Semiconductors for Television and Video Systems

BA481 to SAA197

DATA HANDBOOK

BOOK IC02a 1992

Philips Semiconductors

PHILIPS

PHILIPS

QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

Semiconductors for Television and Video Systems

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QUALITY

Total Quality Management

Philips Semiconductors are a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is:

quality assurance

based on ISO 9000 standards, customer standards such as Ford Q1 and IBM MDQ, and the CECC system of conformity. Our factories are certified to ISO 9000 and CECC by external inspectorates

partnerships with customers

PPM co-operations, design-in agreements, and ship-to-stock, just-in-time and self-qualification programmes

partnerships with suppliers

ship-to-stock, statistical process control and ISO 9000 audits

quality improvement programme

continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

Advanced quality planning

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

Product conformance

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- incoming material management through partnerships with suppliers
- in-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control
- acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications
- periodic inspections to monitor and measure the conformance of products.

Product reliability

With the increasing complexity of OEM (original equipment manufacturer) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies have resulted in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

Customer responses

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

PRO ELECTRON TYPE NUMBERING SYSTEM FOR DISCRETE SEMICONDUCTORS

Basic type number

This type designation code applies to discrete semiconductor devices (not integrated circuits), multiples of such devices, semiconductor chips and Darlington transistors.

FIRST LETTER

The first letter gives information about the material for the active part of the device.

A germanium or other material with a band gap of 0.6 to 1 eV

B silicon or other material with a band gap of 1 to 1.3 eV

C gallium arsenide (GaAs) or other material with a band gap of 1.3 eV or more

R compound materials, e.g. cadmium sulphide.

SECOND LETTER

The second letter indicates the function for which the device is primarily designed. The same letter can be used for multi-chip devices with similar elements.
In the following list low power types are defined by $R_{th\ j\text{-}mb} > 15$ K/W and power types by $R_{th\ j\text{-}mb} \leq 15$ K/W.

A diode; signal, low power

B diode; variable capacitance

C transistor; low power, audio frequency

D transistor; power, audio frequency

E diode; tunnel

F transistor; low power, high frequency

G multiple of dissimilar devices/miscellaneous devices; e.g. oscillators. Also with special third letter, see under '*Serial number*'

H diode; magnetic sensitive

L transistor; power, high frequency

N photocoupler

P radiation detector; e.g. high sensitivity photo-transistor; with special third letter

Q radiation generator; e.g. LED, laser; with special third letter

R control or switching device; e.g. thyristor, low power; with special third letter

S transistor; low power, switching

T control and switching device; e.g. thyristor, power; with special third letter

U transistor; power, switching

W surface acoustic wave device

X diode; multiplier, e.g. varactor, step recovery

Y diode; rectifying, booster

Z diode; voltage reference or regulator, transient suppressor diode; with special third letter.

SERIAL NUMBER/SPECIAL THIRD LETTER

The number comprises three figures running from 100 to 999 for devices primarily intended for consumer equipment, or one letter (Z, Y, X, etc.) and two figures running from 10 to 99 for devices primarily intended for industrial or professional equipment.(1) The letter has no fixed meaning, except in the following cases:

A for triacs, after second letter 'R' or 'T'

F for emitters and receivers in fibre-optic communication, after second letter 'G', 'P' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

L for lasers in non-fibre-optic applications, after second letter 'G' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

O for opto-triacs, after second letter 'R'

T for 3-state bicolour LEDs, after second letter 'Q'

W for transient voltage suppressor diodes, after second letter 'Z'.

EXAMPLES OF BASIC TYPE NUMBERS

AA112: germanium, low power signal diode (consumer type)

ACY32: germanium, low power AF transistor (industrial type)

BD232: silicon, power AF transistor (consumer type)

CQY17: GaAs, light-emitting diode (industrial type)

RPY84: CdS, photo-conductive cell (industrial type).

Version letter(s)

One or two letters may be added to the basic type number to indicate minor electrical or mechanical variants of the basic type. The letters never have a fixed meaning, except that the letter 'R' indicates reverse polarity and the letter 'W' indicates a surface mounted device (SMD).

(1) When the supply of these serial numbers is exhausted, the serial number may be expanded to three figures for industrial types and four figures for consumer types.

Suffix

Sub-classification can be used for devices supplied in a wide range of variants, called associated types. The following sub-coding suffixes are in use:

VOLTAGE REFERENCE AND VOLTAGE REGULATOR DIODES

One letter and one number, preceded by a hyphen (-). The letter, if required, indicates the nominal tolerance of the Zener voltage.

A 1%
B 2%
C 5%
D 10%
E 20%

In the case of a 3% tolerance, the letter 'F' is used.

The number denotes the typical operating (Zener) voltage, related to the nominal current rating for the entire range. The letter 'V' is used in place of the decimal point.

Example: BZY74-C6V3 or -C10.

TRANSIENT VOLTAGE SUPPRESSOR DIODES

One number, preceded by a hyphen (-). The number indicates the maximum recommended continuous reversed (stand-off) voltage, V_R. The letter 'V' is used in place of the decimal point.

Example: BZW70-9V1 or –39.

The letter 'B' may be used immediately after the last number, to indicate a bidirectional suppressor diode.

Example: BZW10-15B.

CONVENTIONAL AND CONTROLLED AVALANCHE RECTIFIER DIODES AND THYRISTORS

One number, preceded by a hyphen (-). The number indicates the rated maximum repetitive peak reverse voltage, V_{RRM}, or the rated repetitive peak off-state voltage, V_{DRM}, whichever is the lower. Reversed polarity with respect to the case is indicated by the letter 'R' immediately after the number.

Example: BYT-100 or -100R.

RADIATION DETECTORS

One number, preceded by a hyphen (-). The number indicates the depletion layer in micrometres (μm). The resolution is indicated by a version letter.

Example: BPX10-2A.

ARRAY OF RADIATION DETECTORS AND GENERATORS

One number, preceded by a hyphen (-). The number indicates the number of basic devices assembled into the array.

Examples: BPW50-6, BPW50-9, BPW50-12.

HIGH FREQUENCY POWER TRANSISTORS

One number, preceded by a hyphen (-). The number indicates the supply voltage.

Example: BLU80-24.

PRO ELECTRON TYPE NUMBERING SYSTEM FOR INTEGRATED CIRCUITS

Basic type number

This type designation code applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick film and hybrid integrated circuits. The basic type number comprises three letters followed by a serial number.

FIRST AND SECOND LETTERS

Digital family circuits

The first two letters identify the family.(1)

Solitary circuits

The first letter divides solitary circuits into:

S solitary digital circuits
T analog circuits

(1) A logic family is an assembly of digital circuits designed to be interconnected and defined by its base electrical characteristics, such as supply voltage, power consumption, propagation delay, noise immunity.

U mixed analog/digital circuits.

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits.[1]

Microprocessors

The first two letters identify microprocessors and related circuits:

MA microcomputer or central processing unit

MB slice processor (functional slice of microprocessor)

MD related memories

ME other related circuits such as interfaces, clocks, peripheral controllers, etc.

Charge-transfer devices and switched capacitors

The first two letters identify:

NH hybrid circuits

NL logic circuits

NM memories

NS analog signal processing using switched capacitors

NT analog signal processing using charge-transfer devices

NX imaging devices

NY other related circuits

THIRD LETTER

The third letter indicates the operating ambient temperature range:

A temperature range not specified below

B 0 to + 70 °C

C –55 to +125 °C

D –25 to + 70 °C

E –25 to + 85 °C

F –40 to + 85 °C

G –55 to + 85 °C.

If a device has another temperature range, the letter 'A' or a letter indicating a narrower temperature may be used, for example, the range of 0 to +75 °C can be indicated by 'A' or 'B'. Should two devices with the same basic type number both have temperature ranges other than those specified, one would use the letter 'A' and the other the letter 'X'.

Serial number

This may be a four-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

Version letter

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. The version letter has no fixed meaning except for 'Z' which means customized wiring. The following letters are recommended for package variants:

C cylindrical

D ceramic dual in-line (CERDIL, CERDIP)

F flat pack (two leads)

G flat pack (four leads)

H quad flat pack (QFP)

L chip on tape (foil)

P plastic dual in-line (DIL)

Q quad in-line (QUIL)

T mini pack (SOL, SO, VSO)

U uncased chip

Two-letter suffix

A two-letter suffix may be used instead of a single package version letter to give more information. To avoid confusion with serial numbers that end with a letter, a hyphen should precede the suffix.

FIRST LETTER (GENERAL SHAPE)

C cylindrical

D dual in-line (DIL)

E power DIL (with external heatsink)

F flat pack (leads on two sides)

(1) The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added, for example, SH for bubble memories.

G flat pack (leads on four sides)
H quad flat pack (QFP)
K diamond (TO-3 family)
M multiple in-line (except dual, triple and quad)
Q quad in-line (QUIL)
R power QUIL (with external heatsink)
S single in-line (SIL)
T triple in-line
W leaded chip carrier (LCC)
X leadless chip carrier (LLCC)
Y pin grid array (PGA)

SECOND LETTER (MATERIAL)

C metal-ceramic
G glass-ceramic
M metal
P plastic

Examples

PCF1105WP: digital IC; PC family; operating temperature range –40 to +85 °C; serial number 1105; plastic leaded chip carrier.

GMB74LS00A-DC: digital IC; GM family; operating temperature range 0 to +70 °C; company number 74LS00A; ceramic DIL package.

TDA1000P: analog IC; operating temperature range non-standard; serial number 1000; plastic DIL package.

SAC2000: solitary digital circuit; operating temperature range –55 to +125 °C; serial number 2000.

MICROCONTROLLER TYPE NUMBERING

8051 and 90C derivatives

P N X C L DDD F T P /RRR

P = Philips

N = 8 for 8051
9 for 90C

X = 0 for ROM-less
3 for ROM
5 for bondout
7 for EPROM
9 for FEE

C = CMOS

L = low power, low voltage option
E = low electro-magnetic emission

DDD = derivative indication

/RRR = ROM code identification

Package types
A = PLCC
B = QFP
F = ceramic DIL with window
L = CLCC with window
N = ceramic PGA
P = DIL
Q = ceramic flat pack
T = SOL, SO, VSO
Z = piggyback

Temperature range
A = other than specified below
B = 0 to + 70 °C
C = –55 to +125 °C
D = –25 to + 70 °C
E = –25 to + 85 °C
F = –40 to + 85 °C
G = –55 to + 85 °C
H = –40 to +125 °C

Frequency range
A = other than specified below
B = 3.5 to 12 MHz
C = 1.2 to 12 MHz
D = 0.5 to 12 MHz
E = 3.5 to 16 MHz
F = 1.2 to 16 MHz
G = 1.2 to 20 MHz
H = DC to 20 MHz
I = 1.2 to 24 MHz
J = DC to 24 MHz

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage

variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Electrostatic charges

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

Work station

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- persons at a work bench should be earthed via a wrist strap and a resistor
- all mains-powered electrical equipment should be connected via an earth leakage switch
- equipment cases should be earthed
- relative humidity should be maintained between 50 and 65%
- an ionizer should be used to neutralize objects with immobile static charges.

Receipt and storage

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

Assembly

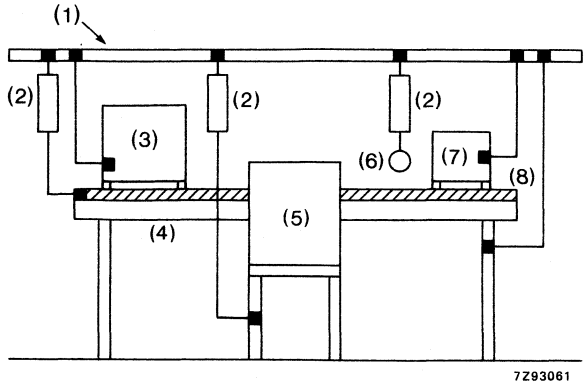
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair.
(6) Wrist strap.
(7) Electrical equipment.
(8) Conductive surface/antistatic sheet.

Fig.1 Protected work station.

DEVICE DATA

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

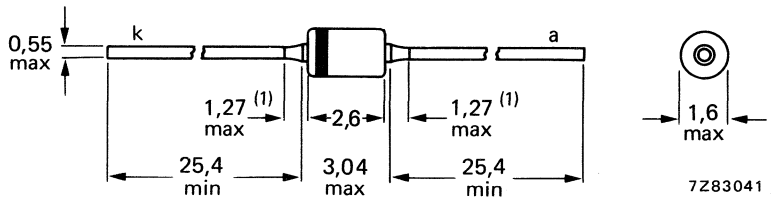
U.H.F. MIXER DIODE

Silicon epitaxial Schottky-barrier diode in a DO-34 envelope and intended for mixer applications in u.h.f. tuners, t.v. modulators and r.f. detectors.

QUICK REFERENCE DATA

Continuous reverse voltage	V_R	max.	4 V
Forward current (d.c.)	I_F	max.	30 mA
Noise figure at f = 900 MHz	F	<	8 dB
Junction temperature	T_j	max.	100 °C

Fig. 1 SOD-68 (DO-34).



(1) Lead diameter in this zone uncontrolled. The BA481 is indicated by a grey band on the cathode side.

The diodes are suitable for mounting on a 2 E (5,08 mm) pitch.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

SILICON PLANAR DIODES

Switching diodes in the subminiature DO-34 glass envelope, intended for band switching in v.h.f. television tuners. Special feature of the diodes is their low capacitance.

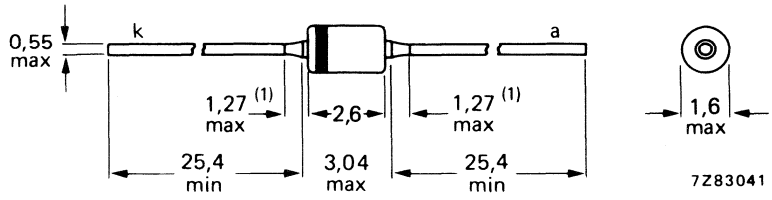
QUICK REFERENCE DATA

Continuous reverse voltage	V_R	max.	35 V			
Forward current (d.c.)	I_F	max.	100 mA			
Junction temperature	T_j	max.	150 °C			
			BA482	BA483	BA484	
Diode capacitance						
V_R = 3 V; f = 1 to 100 MHz	C_d	<	1,2	1,0	1,6	pF
Series resistance at f = 200 MHz						
I_F = 3 mA	r_D	<	0,7	1,2	1,2	Ω
I_F = 10 mA	r_D	typ.	0,4	0,5	0,5	Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-68 (DO-34).



(1) Lead diameter in this zone uncontrolled.
The marking band indicates the cathode.
The diodes are type branded.

Silicon planar diode

BA582

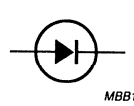
FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

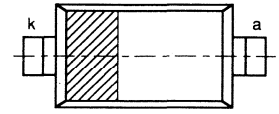
DESCRIPTION

The BA582 is a silicon planar high performance band switching diode, intended for low loss band switching applications in VHF TV tuners. The device has a low diode capacitance and low series resistance and is encapsulated in a microminiature plastic SOD123 envelope.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_R	continuous reverse voltage		35	V
I_F	forward current		100	mA
T_j	junction temperature		150	°C
C_d	diode capacitance	V_R = 3 V; f = 1 to 100 MHz	1.1	pF
r_d	series resistance	I_F = 3 mA; f = 200 MHz	0.7	Ω





Cathode indicated by a blue band

Marking code: P

Fig.1 Simplified outline and symbol.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

BAND-SWITCHING DIODES FOR SURFACE MOUNTING

Switching diodes in a SOD-80 envelope, intended for band switching in v.h.f. television tuners. A special feature of these diodes is their low capacitance.

These SM diodes are leadless diodes in an hermetically sealed micro-miniature glass envelope with tin-plated metal discs at each end. They are suitable for Automatic Placement and as such they can withstand immersion soldering.

The diodes are delivered in "super 8" tape.

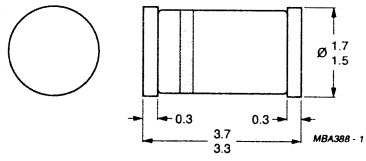
QUICK REFERENCE DATA

			BA682	BA683	
Continuous reverse voltage	V_R	max.	35	35	V
Forward current (d.c.)	I_F	max.	100	100	mA
Junction temperature	T_j	max.	150	150	°C
Diode capacitance V_R = 3 V; f = 1 MHz	C_d	<	1,25	1,2	pF
Series resistance at f = 200 MHz I_F = 3 mA I_F = 10 mA	r_D	< <	0,7 0,5	1,2 0,9	Ω Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-80.



The cathode is indicated by a red band

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

SCHOTTKY BARRIER DIODE

Silicon epitaxial diode in a microminiature plastic envelope. Intended for u.h.f. mixer and fast switching applications in thick and thin-film circuits.

QUICK REFERENCE DATA

Continuous reverse voltage	V_R	max.	4 V
Forward current (d.c.)	I_F	max.	30 mA
Junction temperature	T_j	max.	100 °C
Forward voltage at I_F = 10 mA	V_F	<	600 mV
Diode capacitance at V_R = 0; f = 1 MHz	C_d	<	1,0 pF
Noise figure at f = 900 MHz	F	<	8,0 dB

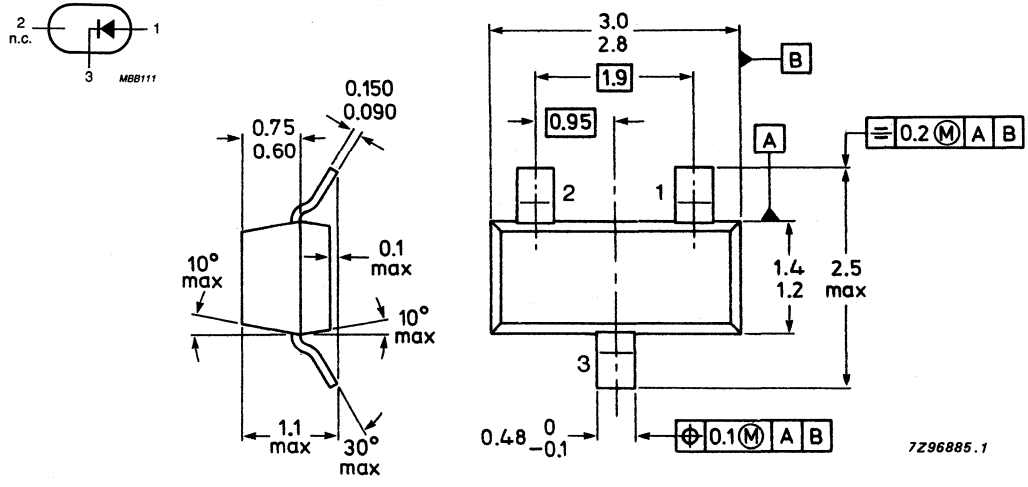
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT-23.

Marking code

BAT17 = A3p



TOP VIEW

Product approved to CECC 50 001-062.

See also *Soldering recommendations.*

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

SILICON PLANAR DIODE

Band switching diode in a microminiature plastic envelope. Intended for thick and thin-film circuits.

QUICK REFERENCE DATA

Continuous reverse voltage	V_R	max.	35 V
Forward current (d.c.)	I_F	max.	100 mA
Junction temperature	T_j	max.	100 °C
Diode capacitance at f = 1 MHz V_R = 20 V	C_d	typ. <	0,8 pF 1,0 pF
Series resistance at f = 200 MHz I_F = 5 mA	r_D	typ. <	0,5 Ω 0,7 Ω

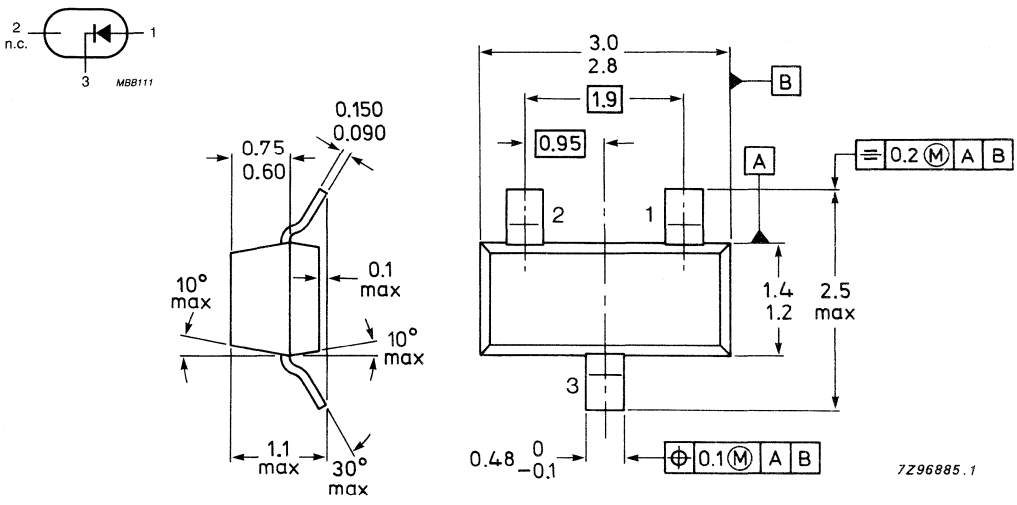
MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-23.

Marking code

BAT18 = A2



TOP VIEW

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

SILICON VARIABLE CAPACITANCE DIODE

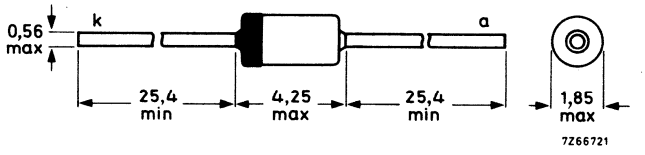
Planar-diffused diode in a DO-35 envelope intended for automatic frequency control in radio and television receivers.

QUICK REFERENCE DATA				
Continuous reverse voltage	V_R	max.	15	V
Junction temperature	T_j	max.	200	°C
Reverse current at V_R = 15 V; T_j = 150 °C	I_R	<	2,0	μA
Diode capacitance at f = 1 MHz V_R = 4 V	C_d	20 to	25	pF
Capacitance ratio at f < 300 MHz	$\frac{C_d\ (V_R = 4\ V)}{C_d\ (V_R = 10\ V)}$	≥	1,3	
Series resistance at V_R = 4 V; f = 200 MHz	r_D	<	1,5	Ω

MECHANICAL DATA

Dimensions in mm

DO-35 (SOD27)



The coloured band indicates the cathode
The diodes are type-branded

VHF variable capacitance diode BB131

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

DESCRIPTION

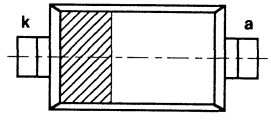
The BB131 is a silicon variable capacitance diode in planar technology, intended for use as a coupling diode in VHF tuners. The device is encapsulated in the ultra-small plastic SMD package, SOD323.

QUICK REFERENCE DATA

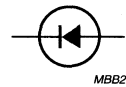
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
I_R	reverse current	V_R = 30 V	–	10	nA
C_d	diode capacitance	V_R = 0.5 V; f = 1 MHz	8	17	pF
		V_R = 28 V; f = 1 MHz	0.7	1.055	pF
$C_{0.5\ V}/C_{28\ V}$	capacitance ratio	f = 1 MHz	12	16	
R_s	series resistance	f = 470 MHz; note 1	–	3	Ω

Note

1. V_R is the value at which C_d = 9 pF.



MSB045



MBB206

Marking code: BB131 = P1.

Fig.1 Simplified outline (SOD323) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
V_{RM}	reverse voltage	peak value	–	30	V
I_F	forward current	DC value	–	20	mA
T_{stg}	storage temperature range		–55	150	°C
T_{amb}	ambient operating temperature range		–55	125	°C

VHF variable capacitance diode BB132

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

DESCRIPTION

The BB132 is a silicon variable capacitance diode in planar technology, with a very high capacitance ratio. It is intended for application in VHF tuners. The device is encapsulated in the ultra-small plastic SMD package, SOD323. A feature of this diode is the excellent matching performance, achieved by the Direct Matching Assembly procedure.

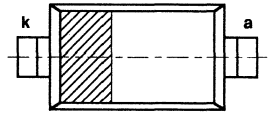
The diodes are delivered on tape in several matched groups, and are also available unmatched upon request.

QUICK REFERENCE DATA

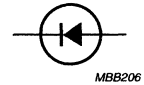
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
I_R	reverse current	V_R = 30 V	–	10	nA
C_d	diode capacitance	V_R = 0.5 V; f = 1 MHz	60	75	pF
		V_R = 28 V; f = 1 MHz	2.3	2.75	pF
$C_{0.5\ V}/C_{28\ V}$	capacitance ratio	f = 1 MHz	24	30	
R_s	series resistance	f = 100 MHz; note 1	–	2	Ω

Note

1. V_R is the value at which C_d = 30 pF.



MSB045



MBB206

Marking code: BB132 = P2.

Fig.1 Simplified outline (SOD323) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
V_{RM}	reverse voltage	peak value	–	30	V
I_F	forward current	DC value	–	20	mA
T_{stg}	storage temperature range		–55	150	°C
T_{amb}	ambient operating temperature range		–55	125	°C

VHF variable capacitance diode BB133

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

DESCRIPTION

The BB133 is a silicon, double-implanted variable capacitance diode in planar technology, intended for use in VHF tuners with a CATV range up to 460 MHz. It has a high linearity and is encapsulated in the ultra-small plastic SMD package, SOD323. A feature of this diode is the excellent matching performance, achieved by the Direct Matching Assembly procedure.

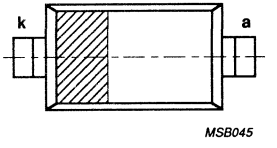
The diodes are delivered on tape in several matched groups, and are also available unmatched upon request.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
I_R	reverse current	V_R = 30 V	–	10	nA
C_d	diode capacitance	V_R = 0.5 V; f = 1 MHz	38	46	pF
		V_R = 28 V; f = 1 MHz	2.2	2.6	pF
$C_{0.5\ V}/C_{28\ V}$	capacitance ratio	f = 1 MHz	14	21	
R_s	series resistance	f = 100 MHz; note 1	–	0.9	Ω

Note

1. V_R is the value at which C_d = 30 pF.



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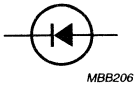


MBB206

Marking code: BB133 = P3.

Fig.1 Simplified outline (SOD323) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
V_{RM}	reverse voltage	peak value	–	30	V
I_F	forward current	DC value	–	20	mA
T_{stg}	storage temperature range		–55	150	°C
T_{amb}	ambient operating temperature range		–55	125	°C

UHF variable capacitance diode BB134

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

DESCRIPTION

The BB134 is a silicon, double-implanted variable capacitance diode in planar technology, intended for use in UHF tuners. It has a high linearity and is encapsulated in the ultra-small plastic SMD package, SOD323. A feature of this diode is the excellent matching performance, achieved by the Direct Matching Assembly procedure.

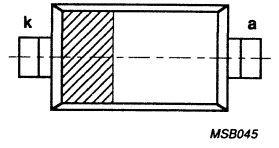
The diodes are delivered on tape in several matched groups. The unmatched type, BB135, has the same specification.

QUICK REFERENCE DATA

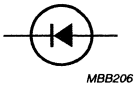
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
I_R	reverse current	V_R = 30 V	–	10	nA
C_d	diode capacitance	V_R = 0.5 V; f = 1 MHz	17.5	21	pF
		V_R = 28 V; f = 1 MHz	1.7	2.1	pF
$C_{0.5\ V}/C_{28\ V}$	capacitance ratio	f = 1 MHz	8.9	12	
R_s	series resistance	f = 470 MHz; note 1	–	0.75	Ω

Note

1. V_R is the value at which C_d = 9 pF.



MSB045



MBB206

Marking code: BB134 = P4.

Fig.1 Simplified outline (SOD323) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
V_{RM}	reverse voltage	peak value	–	30	V
I_F	forward current	DC value	–	20	mA
T_{stg}	storage temperature range		–55	150	°C
T_{amb}	ambient operating temperature range		–55	125	°C

UHF variable capacitance diode BB135

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

DESCRIPTION

The BB135 is a silicon, double-implanted variable capacitance diode in planar technology, intended for use in UHF tuners. It has a high linearity and is encapsulated in the ultra-small plastic SMD package, SOD323.

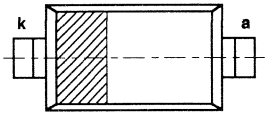
The diodes are delivered on tape (3000 or 10 000 pieces), without gaps.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
I_R	reverse current	V_R = 30 V	–	10	nA
C_d	diode capacitance	V_R = 0.5 V; f = 1 MHz	17.5	21	pF
		V_R = 28 V; f = 1 MHz	1.7	2.1	pF
$C_{0.5\ V}/C_{28\ V}$	capacitance ratio	f = 1 MHz	8.9	12	
R_s	series resistance	f = 470 MHz; note 1	–	0.75	Ω

Note

1. V_R is the value at which C_d = 9 pF.



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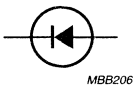


MBB206

Marking code: BB135 = P5.

Fig.1 Simplified outline (SOD323) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
V_{RM}	reverse voltage	peak value	–	30	V
I_F	forward current	DC value	–	20	mA
T_{stg}	storage temperature range		–55	150	°C
T_{amb}	ambient operating temperature range		–55	125	°C

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

UHF VARIABLE CAPACITANCE DIODE

The BB215 is a silicon variable capacitance diode in a hermetically sealed glass envelope (SOD-80) and intended for application in UHF tuners. The leadless SOD-80 encapsulation is intended for surface mounting.
The diode features a capacitance characteristic with a good linearity.

Diodes are supplied in matched sets and the capacitance difference between any two diodes in one set is less than 3% over the voltage range from 0,5 V to 28 V.

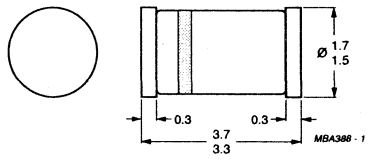
QUICK REFERENCE DATA

Continuous reverse voltage	V_R	max.	30 V
Reverse current V_R = 28 V	I_R	<	10 nA
Diode capacitance at f = 500 kHz V_R = 28 V	C_d		1,8 to 2,2 pF
Capacitance ratio at f = 500 kHz	$\frac{C_d(V_R = 1\ V)}{C_d(V_R = 28\ V)}$	>	7,6
Series resistance at f = 470 MHz V_R is that value at which C_d = 9 pF	r_s	<	0,75 Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-80.



The cathode is indicated by a white band on the body and a second green band indicates the BB215 type.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

UHF VARIABLE CAPACITANCE DIODE

The BB405B is a silicon variable capacitance diode in a hermetically sealed glass envelope and intended for application in UHF tuners.

This miniature diode can be mounted on a 2 E (5,08 mm) pitch.
Diodes are supplied in matched sets and the capacitance difference between any two diodes in one set is less than 3% over the voltage range from 0,5 V to 28 V.

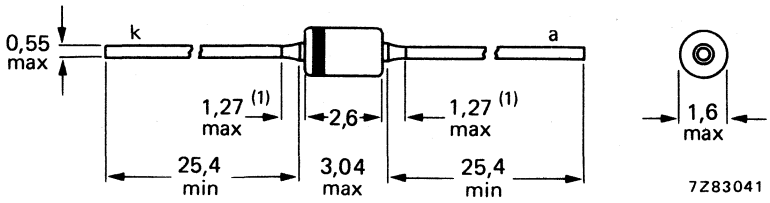
QUICK REFERENCE DATA

Continuous reverse voltage	V_R	max.	30	V
Reverse current V_R = 28 V	I_R	<	10	nA
Diode capacitance at f = 500 kHz V_R = 28 V	C_d		1,8 to 2,2	pF
Capacitance ratio at f = 500 kHz	$\frac{C_d(V_R = 1\ V)}{C_d(V_R = 28\ V)}$	>	7,6	
Series resistance at f = 470 MHz V_R is that value at which C_d = 9 pF	r_s	<	0,75	Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-68 (DO-34).



(1) Lead diameter in this zone uncontrolled.
The cathode is indicated by a white band on a black body.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

VARIABLE CAPACITANCE DIODE

The BB417 is a silicon variable capacitance diode in a hermetically sealed glass DO-34 envelope. The diode is primarily intended for automatic frequency control in television receivers.

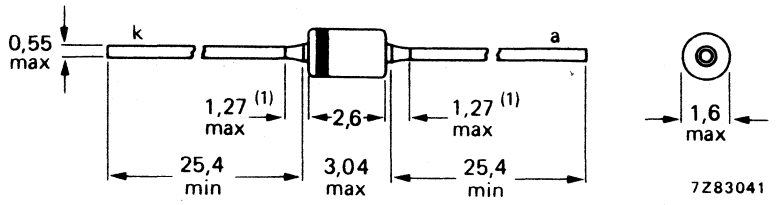
QUICK REFERENCE DATA

Continuous reverse voltage	V_R	max.	20 V
Reverse current at V_R = 20 V	I_R	<	100 nA
Diode capacitance at f = 500 kHz V_R = 15 V	C_d		2,2 to 4,0 pF
Capacitance ratio	$\frac{C_d(V_R = 4\ V)}{C_d(V_R = 15\ V)}$		2,0 to 5,0
Series resistance at f = 470 MHz V_R is that value at which C_d = 9 pF	r_D	<	1,2 Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-68 (DO-34).



(1) Lead diameter in this zone uncontrolled.

Cathode indicated by a white band.

Maximum soldering iron or solder bath temperature 300 °C; maximum soldering time 3 s. Distance from soldering point to seal must be at least 1,5 mm.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

UHF VARIABLE CAPACITANCE DIODE

The BB515 is a silicon variable capacitance diode in a hermetically sealed glass envelope and intended intended for application in UHF tuners

QUICK REFERENCE DATA

Continuous reverse voltage	V_R	max.	30 V
Reverse current at V_R = 30 V	I_R	max.	10 nA
Diode capacitance at f = 1 MHz at V_R = 28 V	C_d		1.85 to 2.25 pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 1\ V)}{C_d\ (V_R = 28\ V)}$		8 to 9.6
Series resistance at f = 470 MHz V_R is that value at which C_d = 9 pF	r_s	typ.	0.5 Ω

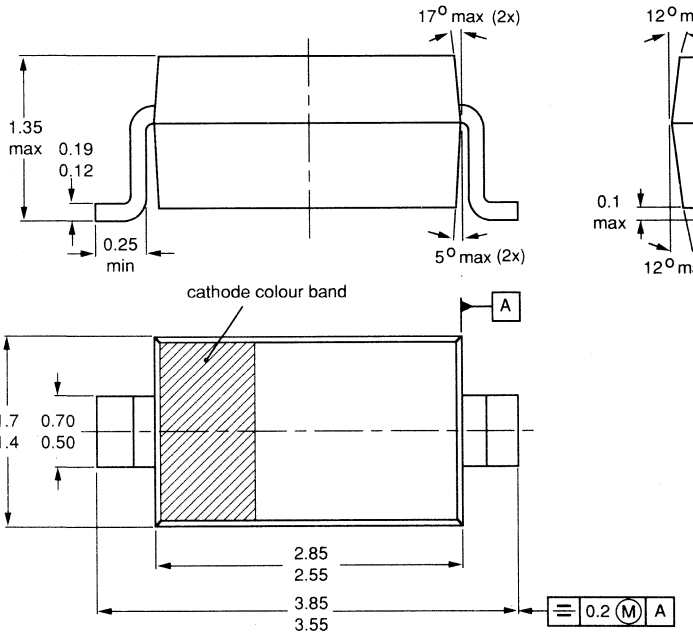
MECHANICAL DATA

Dimensions in mm

Fig.1 SOD123.

Marking code

BB515 = P



Cathode indicated by a white band.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

VHF VARIABLE CAPACITANCE DIODE

The BB619 is a VHF variable capacitance diode in planar technology with a very high capacitance ratio intended for VHF-band B up to 460 MHz in all-band tuners.
The diode is encapsulated in a hermetically sealed SOD123 plastic envelope suitable for surface mounting.

QUICK REFERENCE DATA

Continuous reverse voltage	V_R	max.	30 V
Reverse current at V_R = 30 V	I_R	max.	10 nA
Diode capacitance at f = 1 MHz at V_R = 28 V	C_d		2.4 to 2.9 pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 1\ V)}{C_d\ (V_R = 28\ V)}$	min. typ.	12.5 14
Series resistance at f = 100 MHz; V_R is that value at which C_d = 30 pF	r_s	typ.	0.7 Ω

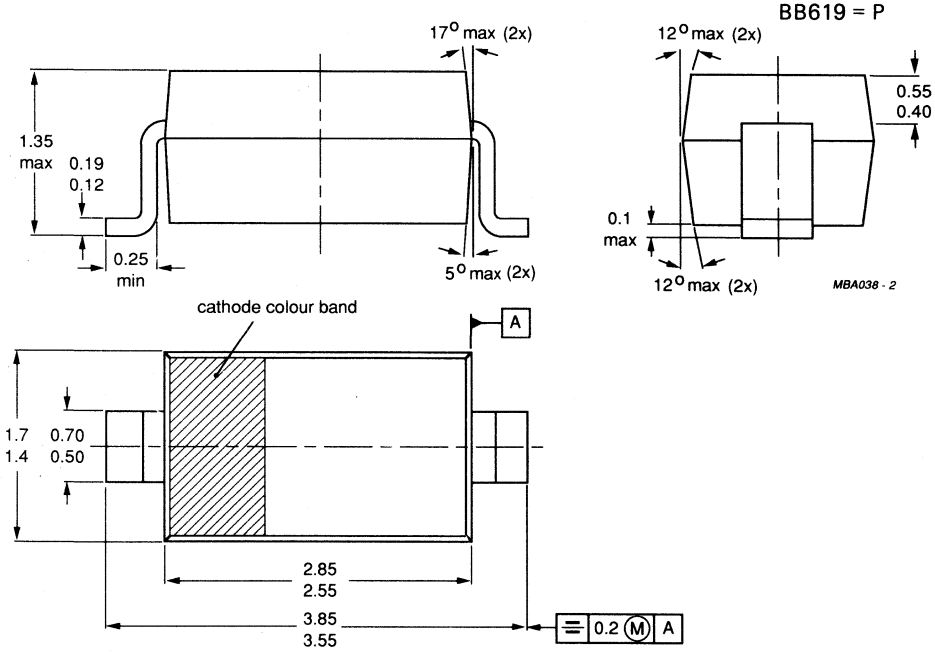
MECHANICAL DATA

Dimensions in mm

Fig.1 SOD123.

Marking code

BB619 = P



Cathode indicated by a yellow band.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

VHF VARIABLE CAPACITANCE DIODE

The BB620 is a VHF variable capacitance diode in planar technology with a very high capacitance ratio intended for VHF-band A up to 160 MHz in all-band tuners.
The diode is encapsulated in a hermetically sealed SOD123 envelope suitable for surface mounting.

QUICK REFERENCE DATA

Continuous reverse voltage	V_R	max.	30 V
Reverse current at V_R = 30 V	I_R	max.	10 nA
Diode capacitance at f = 1 MHz at V_R = 28 V	C_d		2.9 to 3.4 pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 1\ V)}{C_d\ (V_R = 28\ V)}$		19.5 to 25
Series resistance at f = 100 MHz V_R is that value at which C_d = 30 pF	r_s	typ.	1.3 Ω

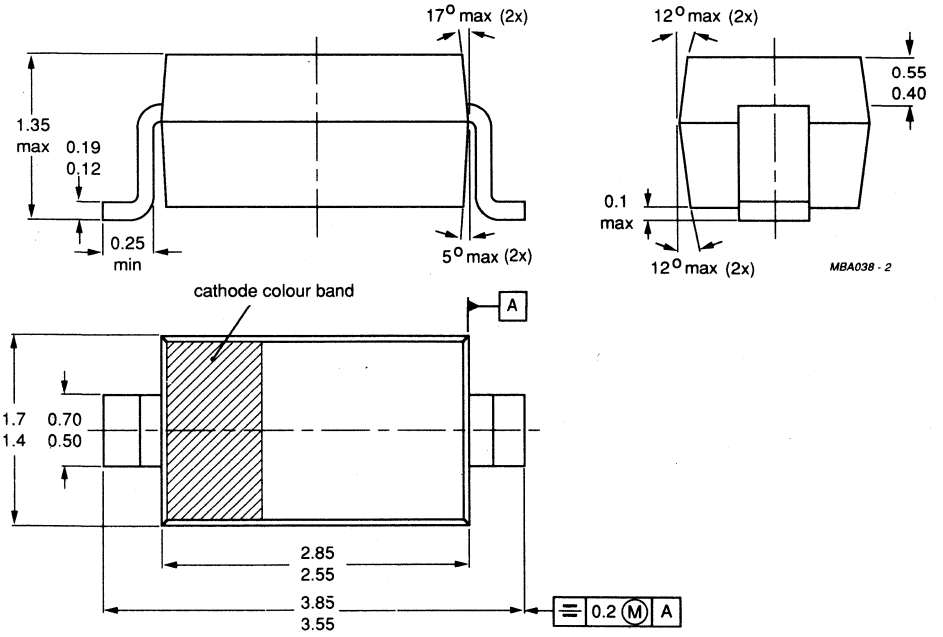
MECHANICAL DATA

Dimensions in mm

Fig.1 SOD123.

Marking code

BB620 = P



Cathode indicated by a red band.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

UHF VARIABLE CAPACITANCE DIODE

The BB811 is a silicon variable capacitance diode in a hermetically sealed SOD123 envelope and intended for application in TV-SAT tuners up to 2 GHz

QUICK REFERENCE DATA

Continuous reverse voltage	V_R	max.	30 V
Reverse current at V_R = 30 V	I_R	max.	20 nA
Diode capacitance at f = 1 MHz at V_R = 28 V	C_d		0.85 to 1.2 pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 1\ V)}{C_d\ (V_R = 28\ V)}$		7.8 to 9.5
Series resistance at f = 100 MHz; V_R is that value at which C_d = 9 pF	r_s	max.	1.45 Ω

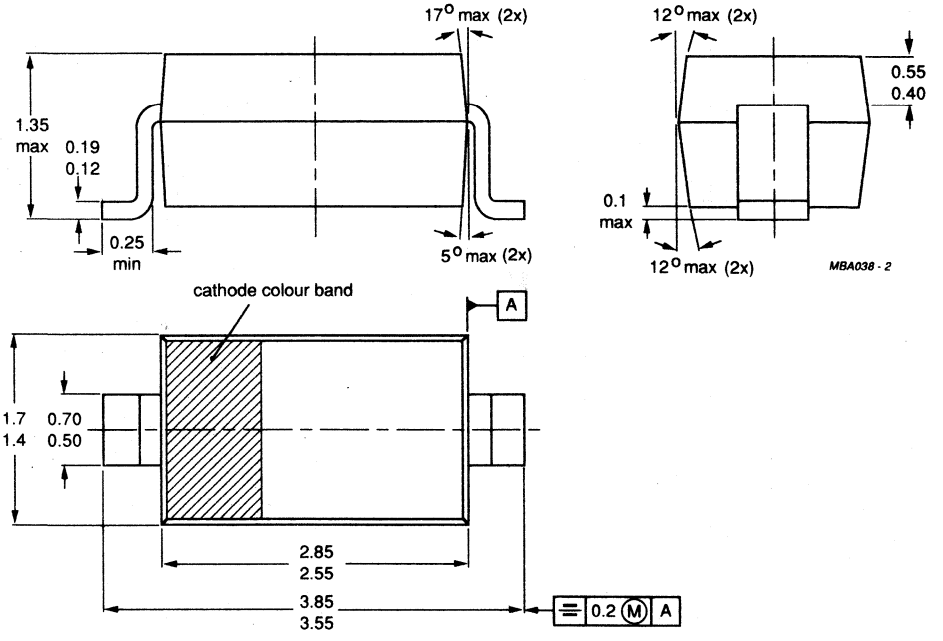
MECHANICAL DATA

Dimensions in mm

Fig.1 SOD123.

Marking code

BB811 = T



Cathode indicated by a white band.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

SILICON PLANAR VARIABLE CAPACITANCE DIODE

The BB909 is a variable capacitance diode in a glass envelope intended for electronic tuning in v.h.f. television tuners for C.A.T.V. applications.

Diodes are supplied in matched sets (minimum 120 pieces and divisible by 12) and the capacitance difference between any two diodes in one set is less than 2,5% over the voltage range from 1 V to 28 V.

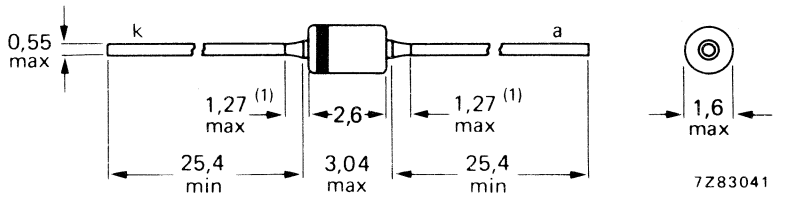
QUICK REFERENCE DATA

Reverse voltage (peak value)	V_{RM}	max.	32	V
Reverse current at V_R = 28 V	I_R	<	10	nA
Diode capacitance at f = 0,5 MHz		BB909A | BB909B		
V_R = 1 V	C_d	> 31 | 33,5		pF
V_R = 28 V	C_d	2,6–3,0 | 2,8–3,2		pF
Capacitance ratio at f = 0,5 MHz	$\frac{C_d\ (V_R = 1\ V)}{C_d\ (V_R = 28\ V)}$	12–15		
Series resistance at f = 100 MHz V_R is that value at which C_d = 30 pF	r_s	typ. <	0,7 0,9	Ω Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 DO-34 (SOD-68).



(1) Lead diameter in this zone uncontrolled.

BB909B : green cathode ring; body black coloured.
BB909A : additional red band.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

VHF VARIABLE CAPACITANCE DIODE

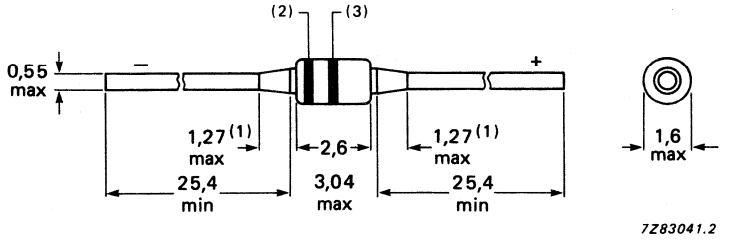
The BB910 is a VHF variable capacitance diode in planar technology with a very high capacitance ratio intended for VHF-band B up to 460 MHz in all-band tuners.
The diode is encapsulated in the whiskerless glass envelope SOD-68.

QUICK REFERENCE DATA

Reverse voltage, peak value	V_{RM}	max.	32 V
Reverse current V_R = 28 V	I_R	<	10 nA
Diode capacitance at f = 1 MHz V_R = 0.5 V V_R = 28 V	C_d	> .	38 pF 2.3 to 2.7 pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 0.5\ V)}{C_d\ (V_R = 28\ V)}$	>	14
Series resistance at f = 100 MHz V_R is that value at which C_d = 40 pF	r_s	<	1.0 Ω

MECHANICAL DATA

Dimensions in mm



(1) Lead diameter in this zone uncontrolled
(2) Cathode type taping (on black body)
(3) Additional ring for type taping.

Fig. 1 SOD-68.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

VHF VARIABLE CAPACITANCE DIODE

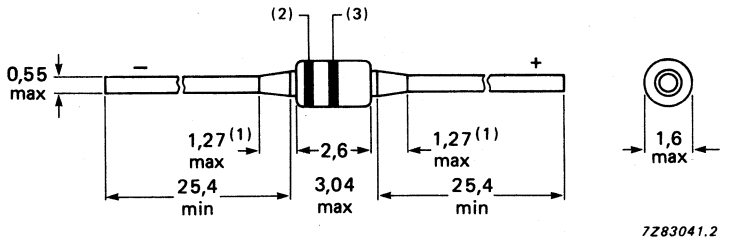
The BB911 is a VHF variable capacitance diode in planar technology with a very high capacitance ratio intended for VHF-band A up to 160 MHz in all-band tuners.
The diode is encapsulated in the whiskerless glass envelope SOD-68.

QUICK REFERENCE DATA

Reverse voltage, peak value	V_{RM}	max.	32 V
Reverse current V_R = 28 V	I_R	<	10 nA
Diode capacitance at f = 1 MHz V_R = 0.5 V V_R = 28 V	C_d	> 	63 pF 2.5 to 3.0 pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 0.5\ V)}{C_d\ (V_R = 28\ V)}$	>	21
Series resistance at f = 100 MHz V_R is that value at which C_d = 40 pF	r_s	<	2.0 Ω

MECHANICAL DATA

Dimensions in mm



(1) Lead diameter in this zone uncontrolled
(2) Cathode type taping (on black body)
(3) Additional ring for type taping.

Fig. 1 SOD-68.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

VARIABLE CAPACITANCE DIODE

Silicon planar variable capacitance diode in a microminiature envelope. It is intended for electronic tuning applications in thick and thin-film circuits.

QUICK REFERENCE DATA

Reverse voltage	V_R	max.	28 V
Reverse current at V_R = 28 V	I_R	<	50 nA
Diode capacitance at f = 1 MHz V_R = 28 V	C_d		1,6 to 2,0 pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 1\ V)}{C_d\ (V_R = 28\ V)}$	typ.	9,7
Series resistance at f = 470 MHz V_R = that value at which C_d = 9 pF	r_D	<	1,2 Ω

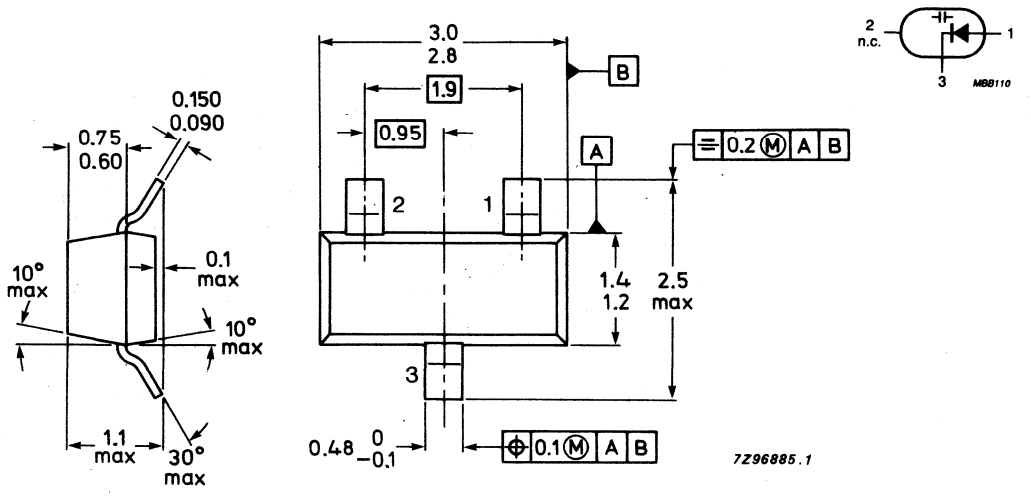
MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-23.

Marking code

BBY31 = $S1_p$



TOP VIEW

See also *Soldering recommendations.*

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

DOUBLE VARIABLE CAPACITANCE DIODE

The BBY39 is a double variable capacitance diode with a common cathode and mounted in a microminiature envelope (SOT-23), suitable for surface mounting. The two diodes in one envelope are matched.

The device is intended for application in electronic tuners in satellite TV systems.

QUICK REFERENCE DATA

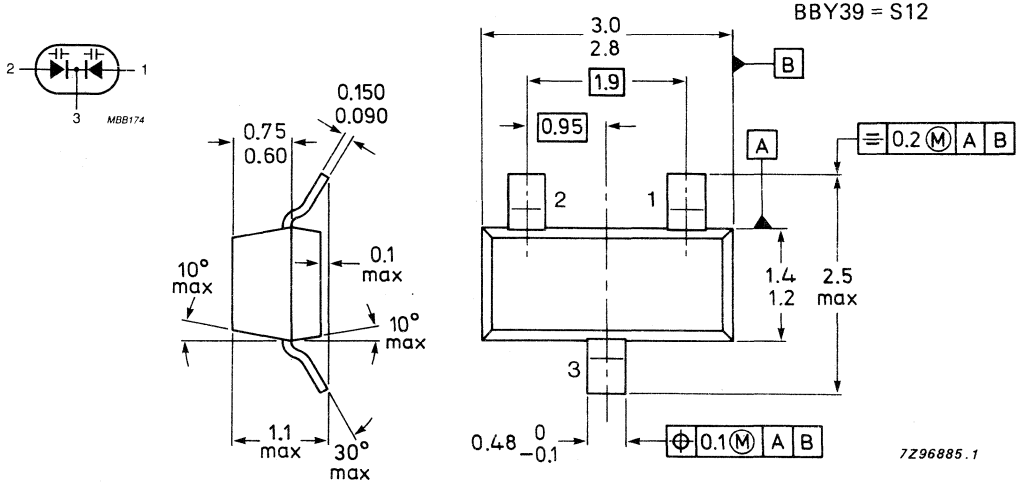
For each diode:			
Continuous reverse voltage	V_R	max.	30 V
Operating junction temperature	T_j	max.	85 °C
Reverse current V_R = 28 V	I_R	<	10 nA
Diode capacitance at f = 1 MHz V_R = 28 V	C_d		1,6 to 2,0 pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 1\ V)}{C_d\ (V_R = 28\ V)}$	>	8,0
Series resistance at f = 470 MHz V_R is that value at which C_d = 9 pF	r_s	<	1,2 Ω

MECHANICAL DATA

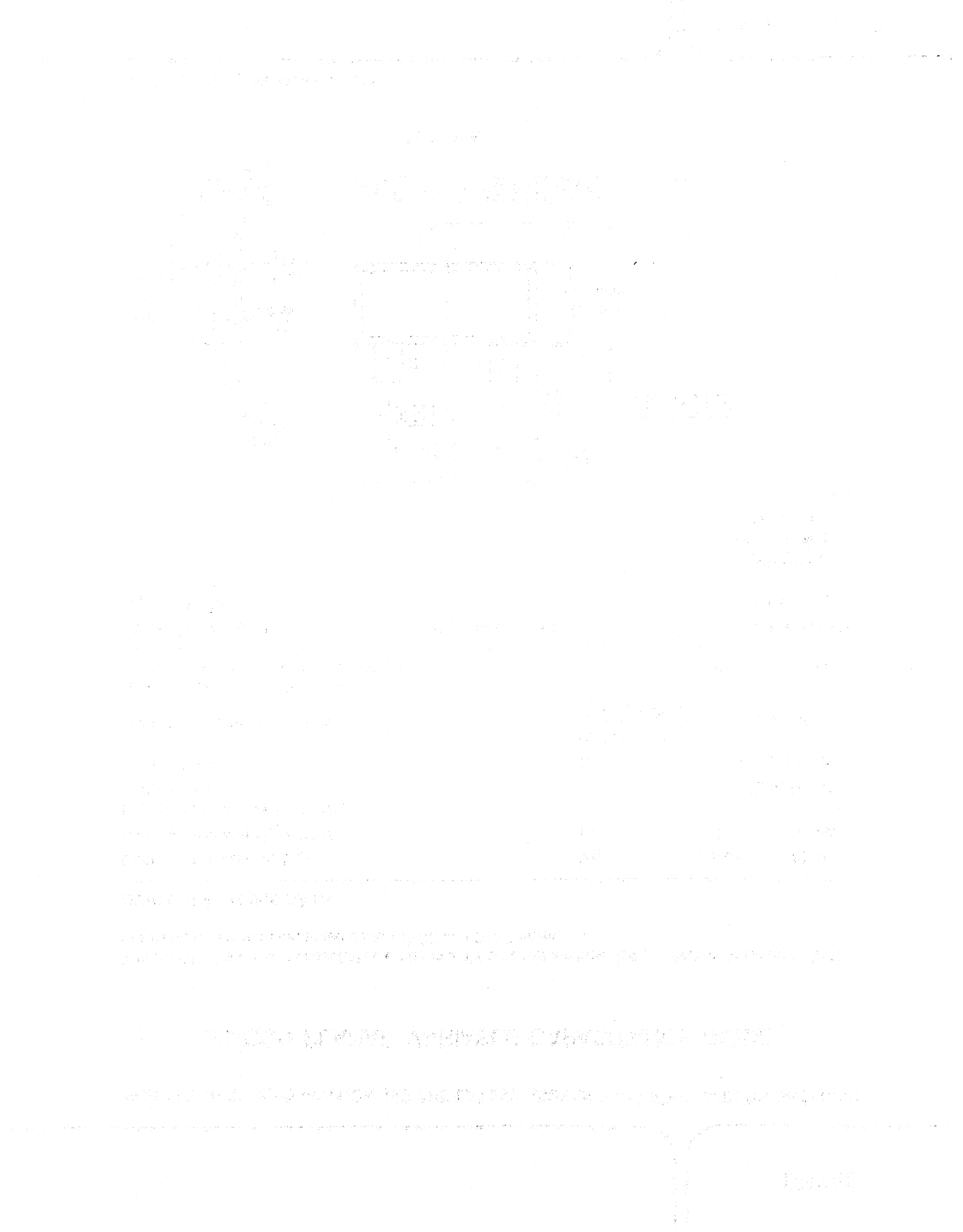
Fig. 1 SOT-23.

Dimensions in mm

Marking code:
BBY39 = S12



TOP VIEW



FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

SILICON PLANAR VARIABLE CAPACITANCE DIODE

The BBY40 is a variable capacitance diode in a plastic envelope intended for electronic tuning in VHF television tuners with extended band I (FCC and OIRT-norm).

QUICK REFERENCE DATA

Continuous reverse voltage	V_R	max.	28 V
Reverse current at V_R = 28 V	I_R	<	10 nA
Diode capacitance at f = 1 MHz			
V_R = 1 V	C_d		39 to 46 pF
V_R = 28 V	C_d		3.8 to 4.8 pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 1\ V)}{C_d\ (V_R = 28\ V)}$		8 to 12
Series resistance at f = 200 MHz V_R is that value at which C_d = 25 pF	r_S	<	0.7 Ω

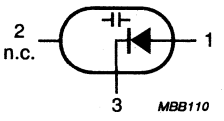
MECHANICAL DATA

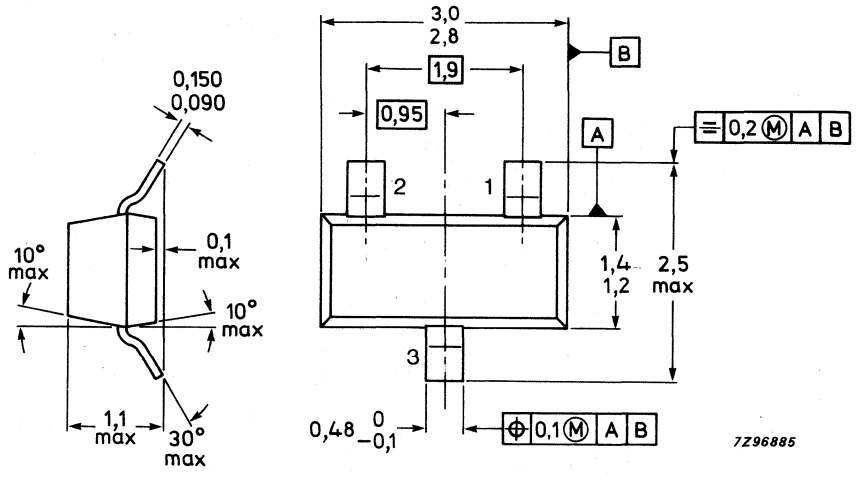
Dimensions in mm

Fig. 1 SOT-23.

Marking code

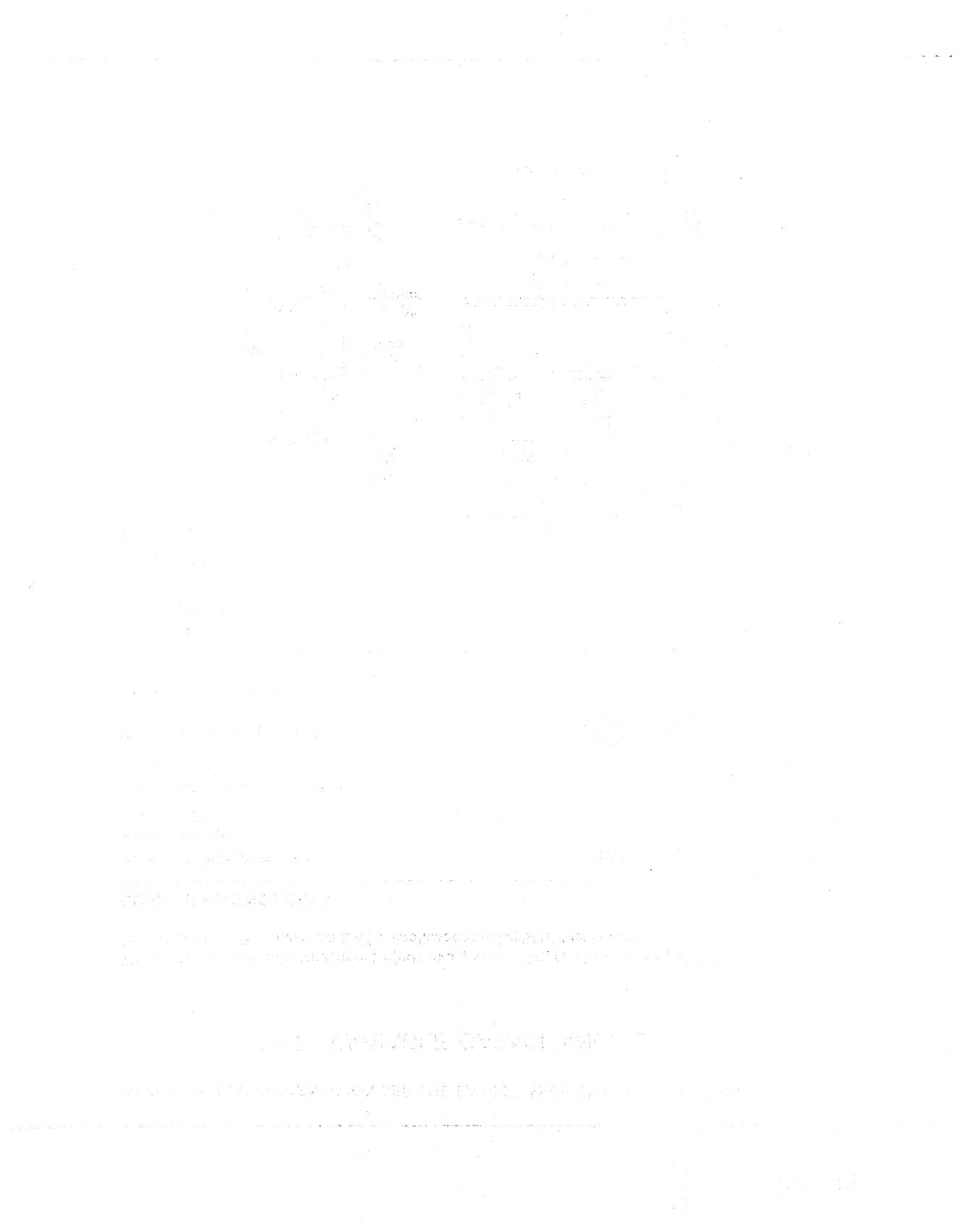
BBY40 = S2





TOP VIEW

See also *Soldering recommendations*.



FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

V.H.F. VARIABLE CAPACITANCE DIODE

The BBY42 is a variable capacitance diode in a microminiature plastic envelope SOT-23. It is intended for use in v.h.f. TV tuners and CATV applications using SMD technology.

QUICK REFERENCE DATA

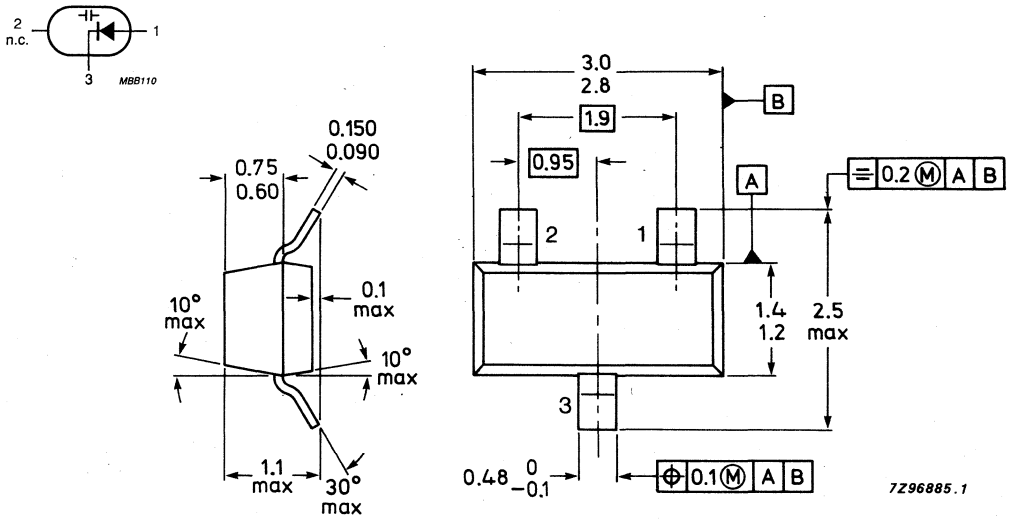
Reverse voltage, peak value	V_{RM}	max. 32 V
Reverse current V_R = 28 V	I_R	max. 10 nA
Diode capacitance at f = 1 MHz V_R = 28 V	C_d	2,4 to 3,0 pF
Capacitance ratio at f = 1 MHz	$\frac{C_d(V_R = 1\ V)}{C_d(V_R = 28\ V)}$	12 to 16
Series resistance at f = 100 MHz V_R is that value at which C_d = 30 pF	r_s	typ. 0,9 Ω max. 1,0 Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-23.

Marking code: S13



TOP VIEW

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC04 OR DATASHEET

SILICON EPITAXIAL TRANSISTORS

N-P-N transistors in plastic TO-92 envelope primarily intended for class-B video output stages in colour television and professional monitor equipment. P-N-P complements are BF421 and BF423.

QUICK REFERENCE DATA

			BF420	BF422	
Collector-base voltage (open emitter)	V_{CBO}	max.	300	250	V
Collector-emitter voltage	V_{CER}	max.	300		V
	V_{CEO}	max.		250	V
Collector current (peak value)	I_{CM}	max.	100		mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	830		mW
Junction temperature	T_j	max.	150		°C
D.C. current gain at T_j = 25 °C I_C = 25 mA; V_{CE} = 20 V	h_{FE}	>	50		
Transition frequency I_C = 10 mA; V_{CE} = 10 V	f_T	>	60		MHz
Feedback capacitance at f = 1 MHz I_C = 0; V_{CE} = 30 V	C_{re}	<	1,6		pF

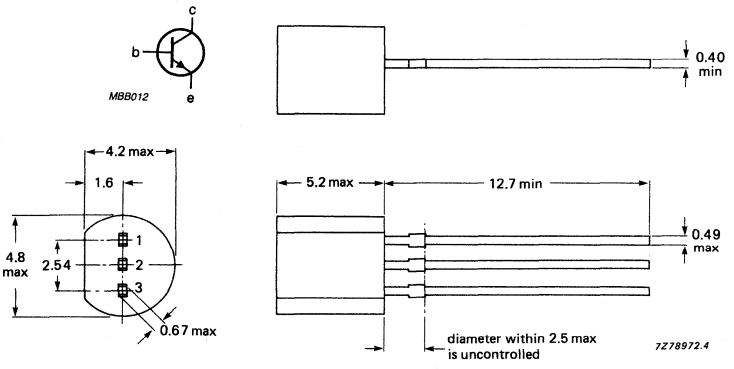
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92.

Pinning

1 = base
2 = collector
3 = emitter



Capability approved to CECC NECC-C-002

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC04 OR DATASHEET

SILICON EPITAXIAL TRANSISTORS

P-N-P transistors in plastic TO-92 envelope primarily intended for class-B video output stages in colour television and professional monitor equipment. N-P-N complements are BF420 and BF422.

QUICK REFERENCE DATA

			BF421	BF423	
Collector-base voltage (open emitter)	$-V_{CBO}$	max.	300	250	V
Collector-emitter voltage (R_{BE} = 2.7 kΩ)	$-V_{CER}$	max.	300		V
(open base)	$-V_{CEO}$	max.		250	V
Collector current (peak value)	$-I_{CM}$	max.	100		mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	830		mW
Junction temperature	T_j	max.	150		°C
D.C. current gain at T_j = 25 °C $-I_C$ = 25 mA; $-V_{CE}$ = 20 V	h_{FE}	>	50		
Transition frequency $-I_C$ = 10 mA; $-V_{CE}$ = 10 V	f_T	>	60		MHz
Feedback capacitance at f = 1 MHz $-I_C$ = 0; $-V_{CE}$ = 30 V	C_{re}	<	1,6		pF

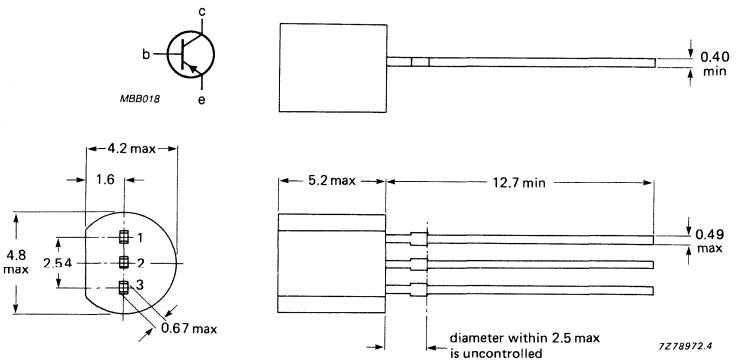
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92.

Pinning:

1 = base
2 = collector
3 = emitter



Capability approved to CECC NECC-C-002

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC06 OR DATASHEET

SILICON PLANAR TRANSISTORS

for video output stages

N-P-N transistors in a SOT-32 plastic envelope intended for video output stages in black-and-white and in colour television receivers.

QUICK REFERENCE DATA

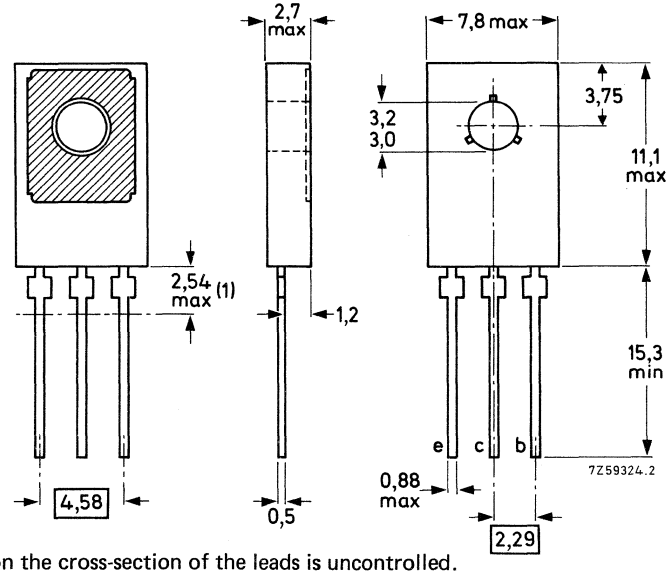
			BF457	BF458	BF459	
Collector-base voltage (open emitter)	V_{CBO}	max.	160	250	300	V
Collector-emitter voltage (open base)	V_{CEO}	max.	160	250	300	V
Collector current (peak value)	I_{CM}	max.		300		mA
Total power dissipation up to T_{mb} = 90 °C	P_{tot}	max.		6		W
Junction temperature	T_j	max.		150		°C
D.C. current gain at T_j = 25 °C I_C = 30 mA; V_{CE} = 10 V	h_{FE}	>		26		
Transition frequency I_C = 15 mA; V_{CE} = 10 V	f_T	typ.		90		MHz
Feedback capacitance at f = 1 MHz I_E = 0; V_{CB} = 30 V	C_{re}	<		3,5		pF

MECHANICAL DATA

Dimensions in mm

Collector connected to metal part of mounting surface

TO-126 (SOT-32)



(1) Within this region the cross-section of the leads is uncontrolled.

See also chapters Mounting instructions and Accessories.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC06 OR DATASHEET

SILICON PLANAR EPITAXIAL TRANSISTORS

N-P-N transistors in plastic envelope intended for class-B video output stages in television receivers and for high-voltage i.f. output stages.
P-N-P complements are BF470 and BF472 respectively.

QUICK REFERENCE DATA

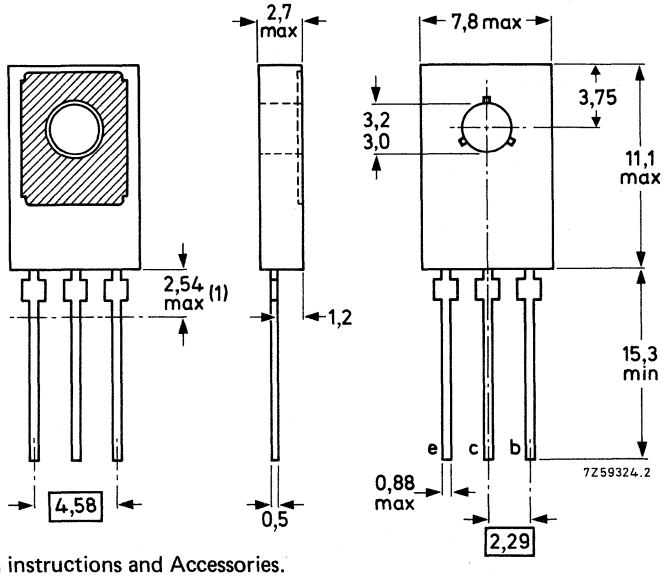
			BF469	BF471	
Collector-base voltage (open emitter)	V_{CBO}	max.	250	300	V
Collector-emitter voltage					
open base	V_{CEO}	max.	250	–	V
R_{BE} = 2,7 kΩ	V_{CER}	max.	–	300	V
Collector current (peak value)	I_{CM}	max.	100		mA
Total power dissipation up to $T_{mb} \leqslant 114$ °C	P_{tot}	max.	1,8		W
Junction temperature	T_j	max.	150		°C
D.C. current gain					
I_C = 25 mA; V_{CE} = 20 V	h_{FE}	>	50		
Transition frequency					
I_C = 10 mA; V_{CE} = 10 V	f_T	>	60		MHz
Feedback capacitance at f = 0,5 MHz					
I_E = 0; V_{CB} = 30 V	C_{re}	<	1,8		pF

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-126 (SOT-32).

Collector connected to mounting base



See also chapters Mounting instructions and Accessories.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC06 OR DATASHEET

SILICON PLANAR EPITAXIAL TRANSISTORS

P-N-P transistors in a plastic envelope intended for class-B video output stages in television receivers and for high-voltage i.f. output stages.
N-P-N complements are BF469 and BF471 respectively.

QUICK REFERENCE DATA

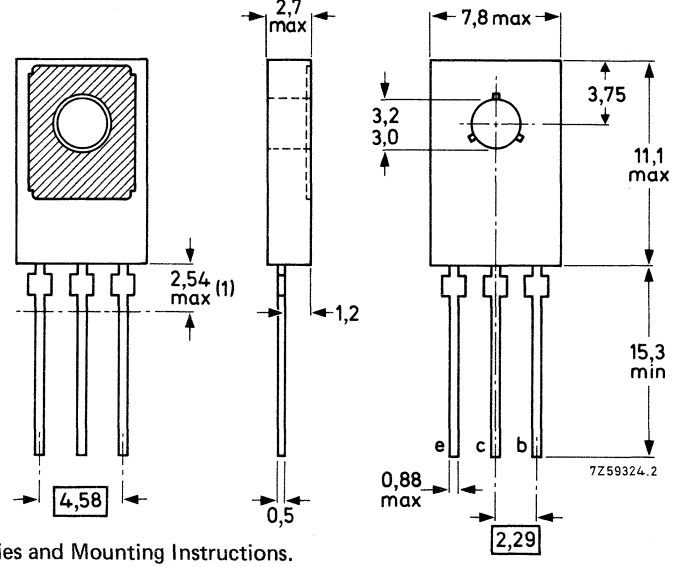
			BF470	BF472	
Collector-base voltage (open emitter)	$-V_{CBO}$	max.	250	300	V
Collector-emitter voltage					
open base	$-V_{CEO}$	max.	250	–	V
R_{BE} = 2,7 kΩ	$-V_{CER}$	max.	–	300	V
Collector current (peak value)	$-I_{CM}$	max.	100		mA
Total power dissipation up to T_{mb} = 114 °C	P_{tot}	max.	1,8		W
Junction temperature	T_j	max.	150		°C
D.C. current gain					
$-I_C$ = 25 mA; $-V_{CE}$ = 20 V	h_{FE}	>	50		
Transition frequency					
$-I_C$ = 10 mA; $-V_{CE}$ = 10 V	f_T	>	60		MHz
Feedback capacitance at f = 0,5 MHz					
I_E = 0; $-V_{CB}$ = 30 V	C_{re}	<	1,8		pF

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-126 (SOT-32).

Collector connected to mounting base.



See also chapters Accessories and Mounting Instructions.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC04 OR DATASHEET

SILICON PLANAR EPITAXIAL TRANSISTORS

N-P-N transistors in TO-92 envelope and intended for use in video output stages in black-and-white and in colour television receivers.

QUICK REFERENCE DATA

			BF483	BF485	BF487	
Collector-base voltage (open emitter)	V_{CBO}	max.	300	350	400	V
Collector-emitter voltage (open base)	V_{CEO}	max.	250	300	350	V
Collector current (peak value)	I_{CM}	max.		100		mA
Total power dissipation (free air)	P_{tot}	max.		830		mW
D.C. current gain I_C = 25 mA; V_{CE} = 20 V	h_{FE}	⩾		50		
Transition frequency $-I_E$ = 10 mA; V_{CB} = 10 V	f_T			70 to 110		MHz
Junction temperature	T_j	max.		150		°C

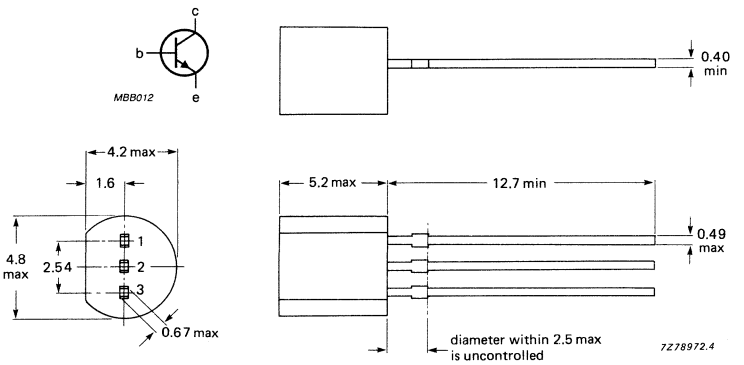
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92.

Pinning:

1 = base
2 = collector
3 = emitter



Capability approved to CECC NECC-C-002

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC04 OR DATASHEET

SILICON PLANAR EPITAXIAL TRANSISTORS

PNP transistors in a TO-92 envelope and intended for use in video output stages of black and white and colour television receivers.

QUICK REFERENCE DATA

			BF484	BF486	BF488	
Collector-base voltage (open emitter)	$-V_{CBO}$	max.	250	300	350	V
Collector-emitter voltage (open base)	$-V_{CEO}$	max.	250	300	350	V
Collector current (peak value)	$-I_{CM}$	max.		100		mA
Total power dissipation (free air)	P_{tot}	max.		830		mW
DC current gain $-I_C$ = 25 mA; $-V_{CE}$ = 20 V	h_{FE}	min.		50		
Transition frequency $-I_C$ = 10 mA; $-V_{CE}$ = 10 V	f_T			70 to 110		MHz
Junction temperature	T_j	max.		150		°C

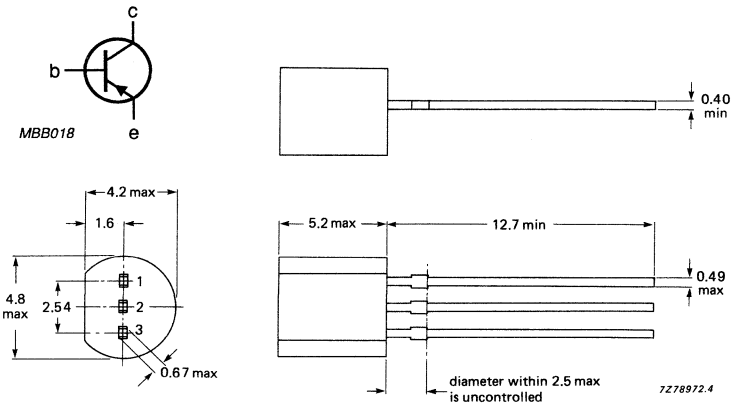
MECHANICAL DATA

Dimensions in mm

Fig.1 TO-92.

Pinning:

1. Base
2. Collector
3. Emitter



Capability approved to CECC NECC-C-002

NPN 1 GHz wideband transistor

BF547

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC10a OR DATASHEET

FEATURES

- Stable oscillator operation
- High current gain
- Good thermal stability.

DESCRIPTION

The BF547 is a low cost NPN transistor in a plastic SOT23 envelope. It is intended for VHF and UHF TV-tuner applications and can be used as a mixer and/or oscillator.

PINNING

PIN	DESCRIPTION
Code: E16	
1	base
2	emitter
3	collector

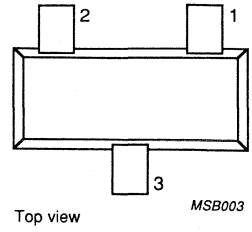


Fig.1 SOT23.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CEO}	collector-emitter voltage	open base	–	20	V
V_{CBO}	collector-base voltage	open emitter	–	30	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_{CM}	peak collector current		–	50	mA
P_{tot}	total power dissipation	up to T_s = 70 °C (note 1)	–	300	mW
T_{stg}	storage temperature range		–55	150	°C
T_j	junction temperature		–	150	°C

Note

1. T_s is the temperature at the soldering point of the collector tab.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC10a OR DATASHEET

SILICON PLANAR EPITAXIAL TRANSISTOR

P-N-P transistor in a microminiature plastic envelope, intended for applications in thick and thin-film circuits such as self-oscillating mixer in u.h.f. tuners in conjunction with bipolar transistors or with MOS fets.

QUICK REFERENCE DATA

Collector-base voltage (open emitter)	$-V_{CBO}$	max.	40 V
Collector-emitter voltage (open base)	$-V_{CEO}$	max.	35 V
Collector current (d.c)	$-I_C$	max.	30 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250 mW
Junction temperature	T_j	max.	150 °C
Transition frequency at f = 100 MHz I_E = 3 mA; $-V_{CB}$ = 10 V	f_T	typ.	900 MHz

MECHANICAL DATA

Dimensions in mm

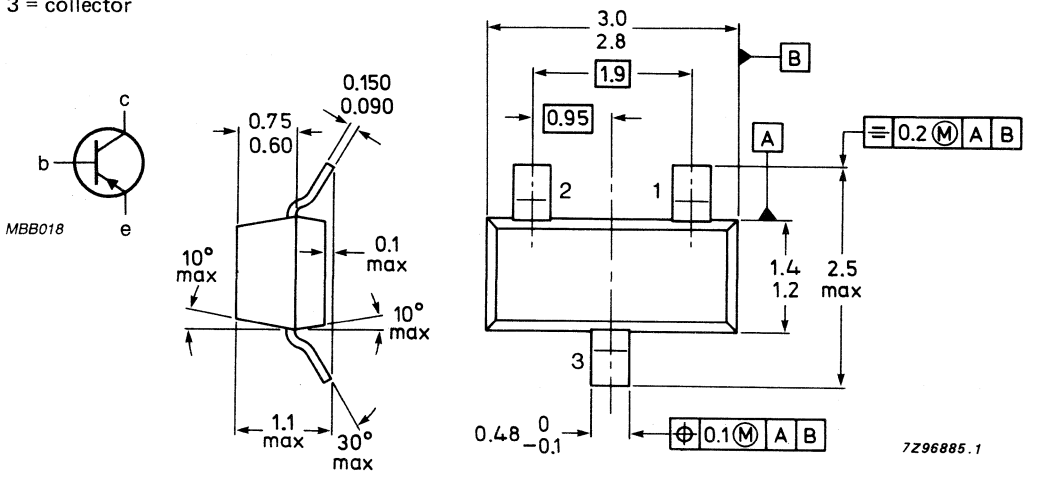
Fig. 1 SOT-23

Pinning:

1 = base
2 = emitter
3 = collector

Marking code

BF569 = LHp



TOP VIEW

See also *Soldering recommendations.*

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC06 OR DATASHEET

SILICON PLANAR EPITAXIAL TRANSISTORS

N-P-N transistors in TO-202 plastic envelope, intended for use in video output stages in black-and-white and in colour television receivers.

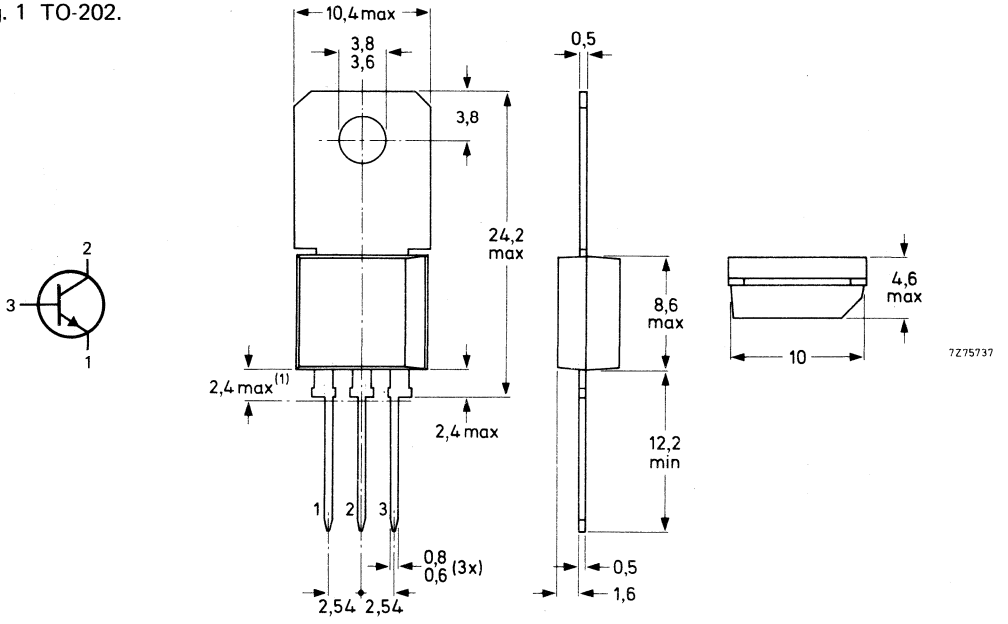
QUICK REFERENCE DATA

			BF583	BF585	BF587	
Collector-base voltage (open emitter)	V_{CBO}	max.	300	350	400	V
Collector-emitter voltage (open base)	V_{CEO}	max.	250	300	350	V
Collector current (peak value)	I_{CM}	max.		100		mA
Total power dissipation (free air)	P_{tot}	max.		1,6		W
D.C. current gain I_C = 25 mA; V_{CE} = 20 V	h_{FE}	min.		50		
Transition frequency $-I_E$ = 10 mA; V_{CB} = 10 V	f_T			70 to 110		MHz
Junction temperature	T_j	max.		150		°C

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-202.



(1) Plastic flash allowed within this zone.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC06 OR DATASHEET

SILICON PLANAR EPITAXIAL TRANSISTORS

PNP transistors in a TO-202 plastic envelope. Intended for use in video output stages of black and white and colour television receivers.

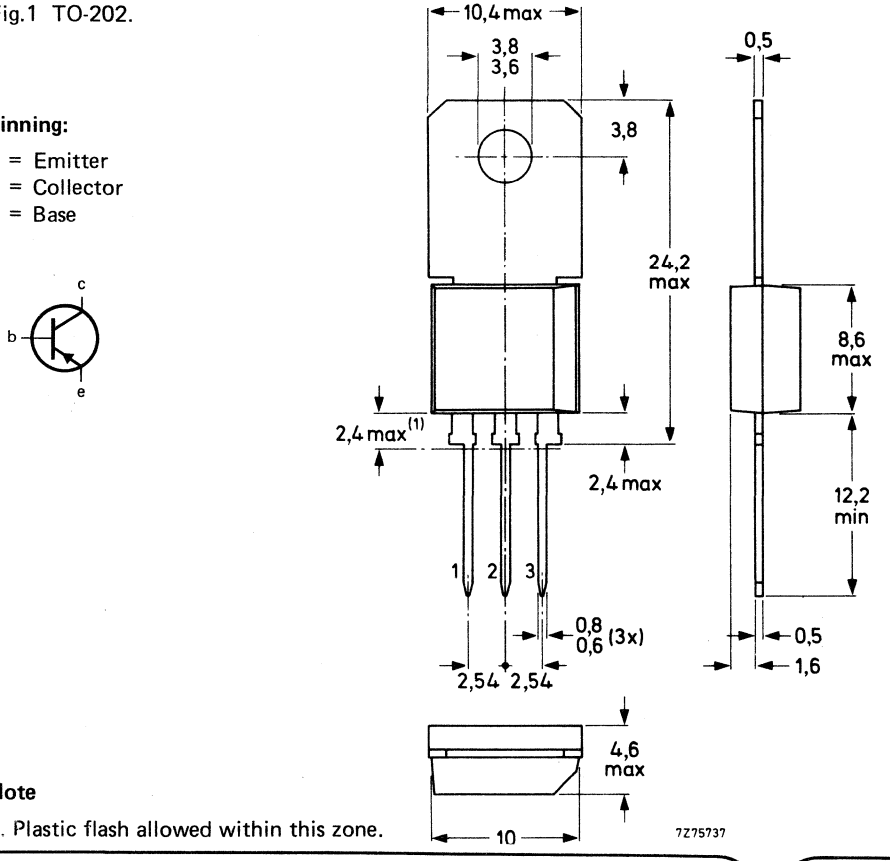
QUICK REFERENCE DATA

			BF584	BF586	BF588	
Collector-base voltage (open emitter)	$-V_{CBO}$	max.	250	300	350	V
Collector-emitter voltage (open base)	$-V_{CEO}$	max.	250	300	350	V
Collector current (peak value)	$-I_{CM}$	max.		100		mA
Total power dissipation (free air)	P_{tot}	max.		1.6		W
DC current gain $-I_C$ = 25 mA; $-V_{CE}$ = 20 V	h_{FE}	min.		50		
Transition frequency $-I_C$ = 10 mA; $-V_{CE}$ = 10 V	f_T			70 to 110		MHz
Junction temperature	T_j	max.		150		°C

MECHANICAL DATA

Dimensions in mm

Fig.1 TO-202.



Pinning:

1 = Emitter
2 = Collector
3 = Base

Note

1. Plastic flash allowed within this zone.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC10a OR DATASHEET

SILICON PLANAR TRANSISTOR

P-N-P transistor, in a microminiature plastic envelope; intended for use as oscillator in v.h.f. tuners with extended frequency range and/or in conjunction with MOS-FETs in thick and thin-film circuits.

QUICK REFERENCE DATA

Collector-base voltage (open emitter)	$-V_{CBO}$	max.	40 V
Collector-emitter voltage (open base)	$-V_{CEO}$	max.	30 V
Collector current (peak value)	$-I_{CM}$	max.	25 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250 mW
Junction temperature	T_j	max.	150 °C
Transition frequency at f = 100 MHz I_E = 5 mA; $-V_{CB}$ = 10 V	f_T	typ.	650 MHz

MECHANICAL DATA

Dimensions in mm

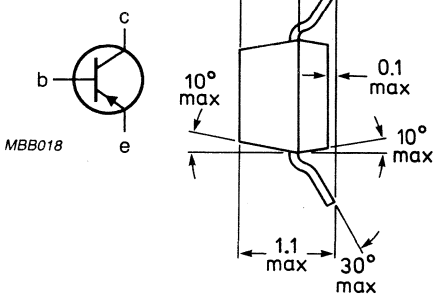
Fig. 1 SOT-23.

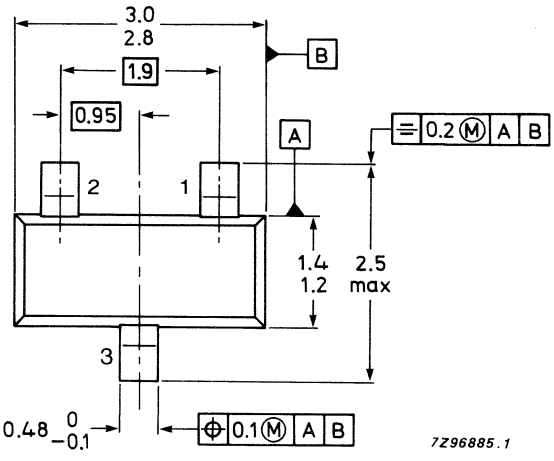
Marking code

BF660 = LEp

Pinning:

1 = base
2 = emitter
3 = collector





TOP VIEW

See also *Soldering recommendations*.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC10a OR DATASHEET

SILICON EPITAXIAL TRANSISTORS

NPN transistors in a microminiature plastic envelope intended for class-B video output stages in colour television receivers, and general purpose high voltage circuits.

PNP complements are BF721 and BF723 respectively.

QUICK REFERENCE DATA

			BF720	BF722	
Collector-base voltage (open emitter)	V_{CBO}	max.	300	250	V
Collector-emitter voltage (open base)	V_{CEO}	max.	–	250	V
Collector-emitter voltage (R_{BE} = 2,7 kΩ)	V_{CER}	max.	300	–	V
Collector current (peak value)	I_{CM}	max.	100		mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1,5		W
Junction temperature	T_j	max.	150		°C
DC current gain I_C = 25 mA; V_{CE} = 20 V	h_{FE}	>	50		
Transition frequency at f = 35 MHz I_C = 10 mA; V_{CE} = 10 V	f_T	>	60		MHz
Feedback capacitance at f = 1 MHz I_C = 0; V_{CE} = 30 V	C_{re}	<	1,6		pF

MECHANICAL DATA

Dimensions in mm

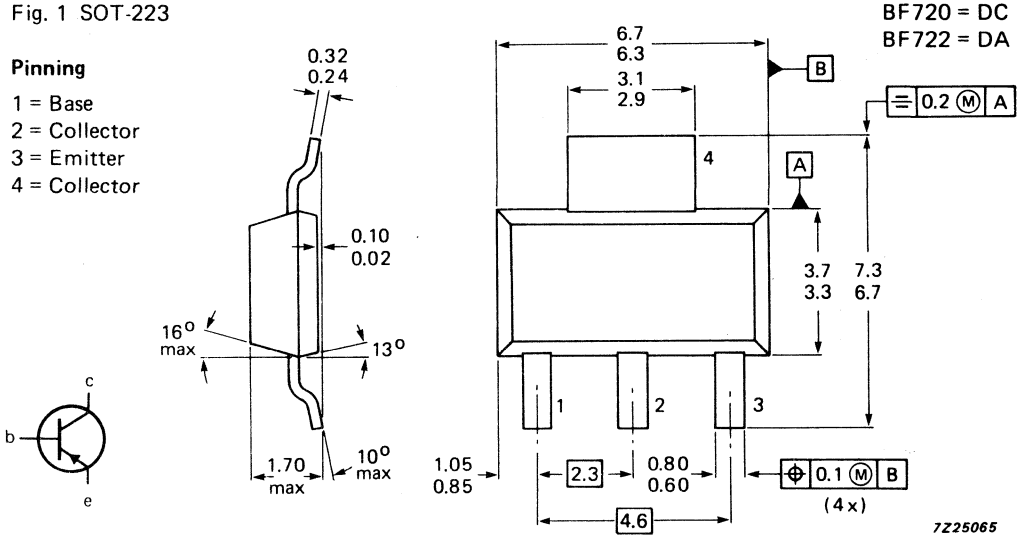
Fig. 1 SOT-223

Pinning

1 = Base
2 = Collector
3 = Emitter
4 = Collector

Marking

BF720 = DC
BF722 = DA



FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC10a OR DATASHEET

SILICON EPITAXIAL TRANSISTORS

PNP transistors in a microminiature plastic envelope intended for application in class-B video output stages in colour television receivers, and general purpose high voltage circuits.

NPN complements are BF720 and BF722 respectively.

QUICK REFERENCE DATA

			BF721	BF723	
Collector-base voltage (open emitter)	$-V_{CBO}$	max.	300	250	V
Collector-emitter voltage (open base)	$-V_{CEO}$	max.	–	250	V
Collector-emitter voltage (R_{BE} = 2,7 kΩ)	$-V_{CER}$	max.	300	–	V
Collector current (peak value)	$-I_{CM}$	max.	100		mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1,5		W
Junction temperature	T_j	max.	150		°C
DC current gain $-I_C$ = 25 mA; $-V_{CE}$ = 20 V	h_{FE}	>	50		
Transition frequency at f = 35 MHz $-I_C$ = 10 mA; $-V_{CE}$ = 10 V	f_T	>	60		MHz
Feedback capacitance at f = 1 MHz I_C = 0; $-V_{CE}$ = 30 V	C_{re}	<	1,6		pF

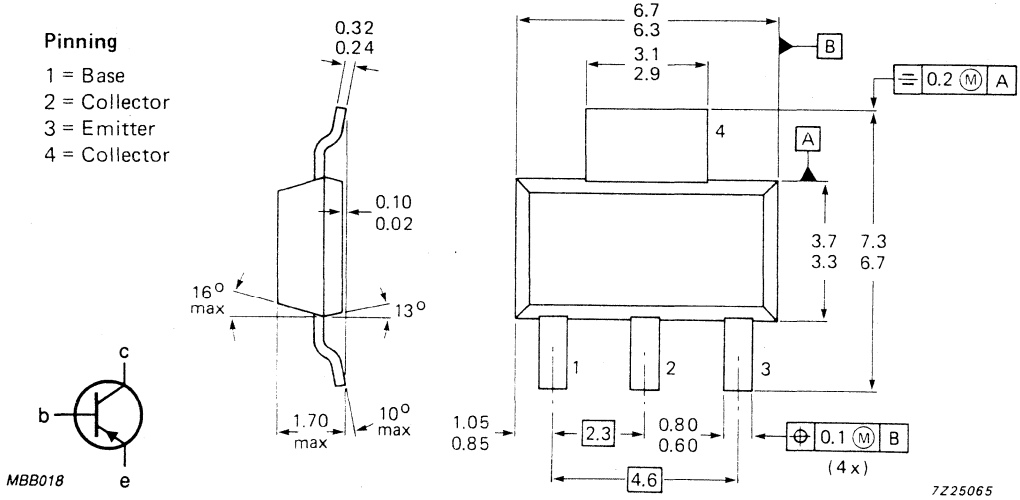
MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-223

Pinning

1 = Base
2 = Collector
3 = Emitter
4 = Collector



Philips Components

Data sheet	
status	Product specification
date of issue	April 1991

BF747
NPN 1 GHz wideband transistor

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC14 OR DATASHEET

FEATURES

- Stable oscillator operation
- High current gain
- Good thermal stability.

DESCRIPTION

The BF747 is a low cost NPN transistor in a plastic SOT23 envelope. It is intended for VHF and UHF TV-tuner applications and can be used as a mixer and/or oscillator.

MECHANICAL DATA

Plastic SOT23.

PIN	DESCRIPTION
1	base
2	emitter
3	collector

Marking code : E15

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CEO}	collector-emitter voltage		-	20	V
V_{CBO}	collector-base voltage		-	30	V
V_{EBO}	emitter-base voltage		-	3	V
I_{CM}	collector current (DC)	peak value	-	50	mA
P_{tot}	total power dissipation	up to T_s = 100°C note 1	-	150	mW
T_{stg}	storage temperature range		–55	+150	°C
T_j	junction temperature		-	+150	°C

Note

1. T_s temperature measured on soldering point of collector tab.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE		
	CODE	PACKING METHOD	PACKING QUANTITY
BF747	SOT23	12 mm reel	3000

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC06 OR DATASHEET

SILICON PLANAR VIDEO OUTPUT TRANSISTORS

N-P-N transistors in TO-202 plastic envelopes intended for video output stages in black-and-white and in colour television receivers.

QUICK REFERENCE DATA

			BF857	BF858	BF859	
Collector-base voltage (open emitter)	V_{CBO}	max.	160	250	300	V
Collector-emitter voltage (open base)	V_{CEO}	max.	160	250	300	V
Collector current (peak value)	I_{CM}	max.		300		mA
Total power dissipation up to T_{mb} = 75 °C	P_{tot}	max.		6		W
Junction temperature	T_j	max.		150		°C
D.C. current gain I_C = 30 mA; V_{CE} = 10 V	h_{FE}	>		26		
Transition frequency at f = 35 MHz I_C = 15 mA; V_{CE} = 10 V	f_T	typ.		90		MHz
Feedback capacitance at f = 1 MHz I_E = 0; V_{CB} = 30 V	C_{re}	<		3		pF

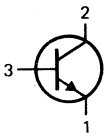
MECHANICAL DATA

Dimensions in mm

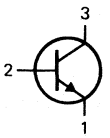
Fig. 1 TO-202.

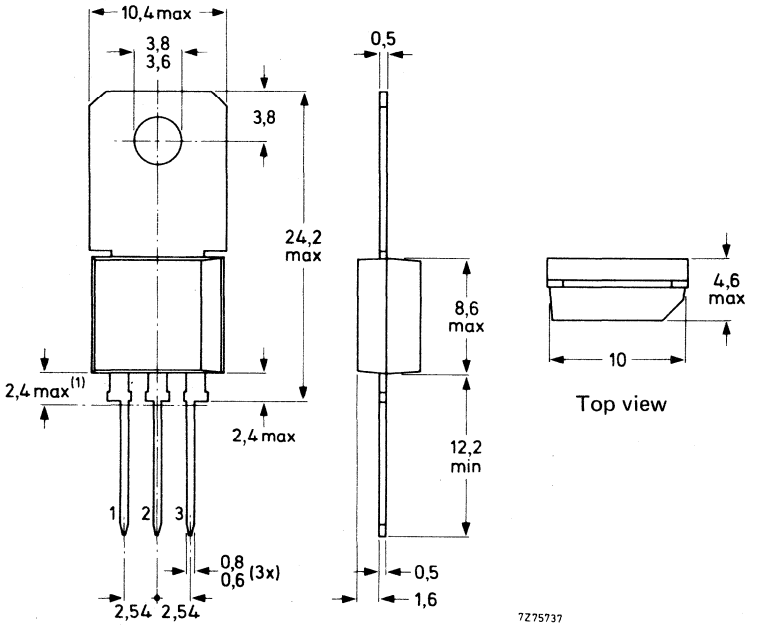
Collector connected to mounting base.

(1) Plastic flash allowed within this zone.



A-version





An A-version is available on request. It has ebc pinning instead of ecb.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC06 OR DATASHEET

SILICON PLANAR VIDEO OUTPUT TRANSISTORS

N-P-N transistors in a TO-202 plastic envelope intended for class-B video output stages in colour television receivers. P-N-P complements are BF870 and BF872.

QUICK REFERENCE DATA

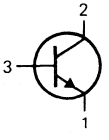
			BF869	BF871	
Collector-base voltage (open emitter)	V_{CBO}	max.	250	300	V
Collector-emitter voltage (open base)	V_{CEO}	max.	250	–	V
Collector-emitter voltage (R_{BE} = 2,7 kΩ)	V_{CER}	max.	–	300	V
Collector current (peak value)	I_{CM}	max.	100		mA
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	5		W
Junction temperature	T_j	max.	150		°C
D.C. current gain I_C = 25 mA; V_{CE} = 20 V; T_j = 25 °C	h_{FE}	>	50		
Transition frequency $-I_E$ = 10 mA; V_{CB} = 10 V	f_T	>	60		MHz
Feedback capacitance at f = 1 MHz I_E = 0; V_{CB} = 30 V	C_{re}	<	2		pF

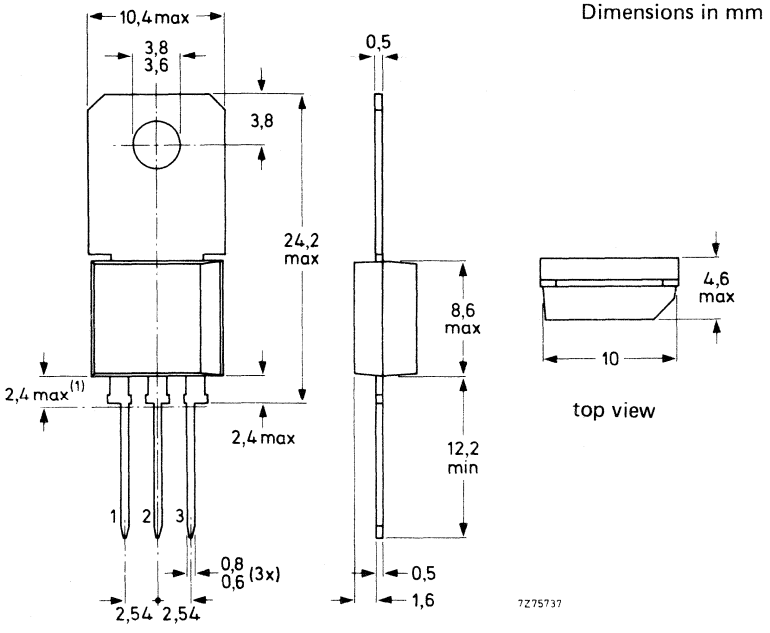
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-202.

Collector connected to mounting base.





(1) Plastic flash allowed within this zone.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC06 OR DATASHEET

SILICON PLANAR VIDEO OUTPUT TRANSISTORS

P-N-P transistors in a TO-202 plastic envelope intended for class-B video output stages in colour television receivers. N-P-N complements are BF869 and BF871.

QUICK REFERENCE DATA

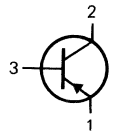
			BF870	BF872	
Collector-base voltage (open emitter)	$-V_{CBO}$	max.	250	300	V
Collector-emitter voltage (open base)	$-V_{CEO}$	max.	250	–	V
Collector-emitter voltage (R_{BE} = 2,7 kΩ)	$-V_{CER}$	max.	–	300	V
Collector current (peak value)	$-I_{CM}$	max.	100		mA
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	5		W
Junction temperature	T_j	max.	150		°C
D.C. current gain $-I_C$ = 25 mA; $-V_{CE}$ = 20 V; T_j = 25 °C	h_{FE}	>	50		
Transition frequency I_E = 10 mA; $-V_{CB}$ = 10 V	f_T	>	60		MHz
Feedback capacitance at f = 1 MHz I_E = 0; $-V_{CB}$ = 30 V	C_{re}	<	2,2		pF

MECHANICAL DATA

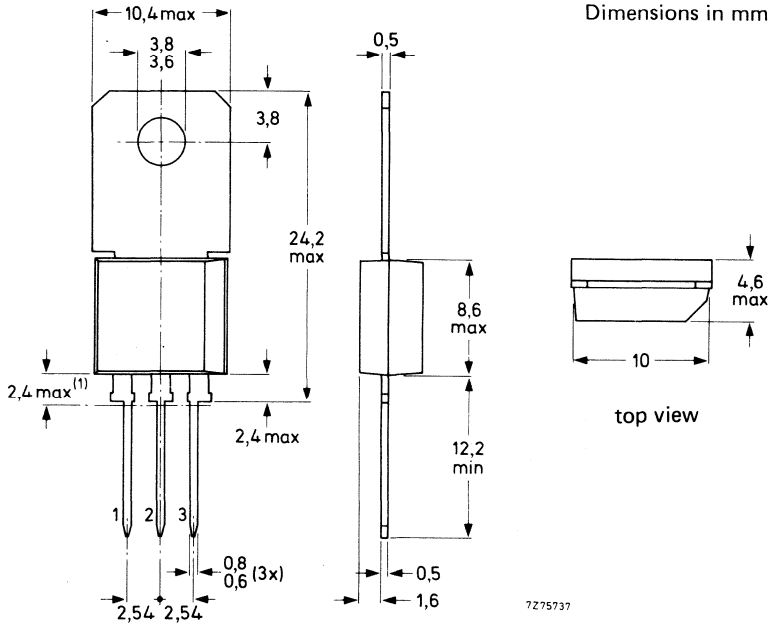
Fig. 1 TO-202.

Collector connected to mounting base.

Dimensions in mm



(1) Plastic flash allowed within this zone.



Dual gate MOS-FETs BF904; BF904R

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC06 OR DATASHEET

FEATURES

- Specially designed for use at 5 V supply voltage
- Short channel transistor with high ratio $|Y_{fs}|:C_{is}$
- Low noise gain-controlled amplifier to 1 GHz
- Superior cross-modulation performance during AGC.

DESCRIPTION

Enhancement type field-effect transistors in plastic microminiature SOT143 and SOT143R envelopes. They are intended for UHF and VHF applications, such as television tuners and professional communications equipment. These transistors consist of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

PINNING

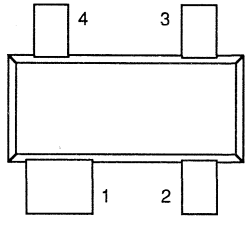
PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

CAUTION

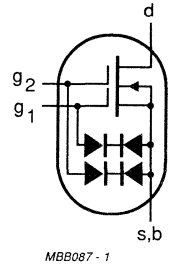
The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage	–	–	7	V
I_D	drain current	–	–	30	mA
P_{tot}	total power dissipation	–	–	200	mW
T_j	junction temperature	–	–	150	°C
$\|Y_{fs}\|$	transfer admittance	22	25	30	mS
C_{ig1-s}	input capacitance at gate 1	–	2.2	2.6	pF
C_{rs}	feedback capacitance	–	25	–	pF
F	noise figure at 800 MHz	–	2	–	dB



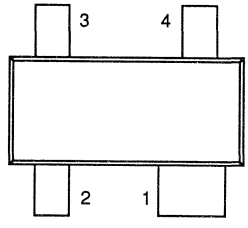
Top view MSB014



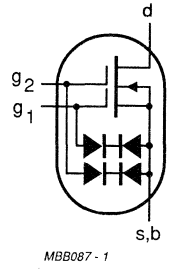
MBB087 - 1

Marking code: MO4.

Fig.1 Simplified outline (SOT143) and symbol.



Top view MSB035



MBB087 - 1

Marking code: MO6.

Fig.2 Simplified outline (SOT143R) and symbol.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for use in u.h.f. applications in television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	20 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	12 mS
Input capacitance at gate 1; f = 1 MHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	1.8 pF
Feedback capacitance at f = 1 MHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	2.8 dB

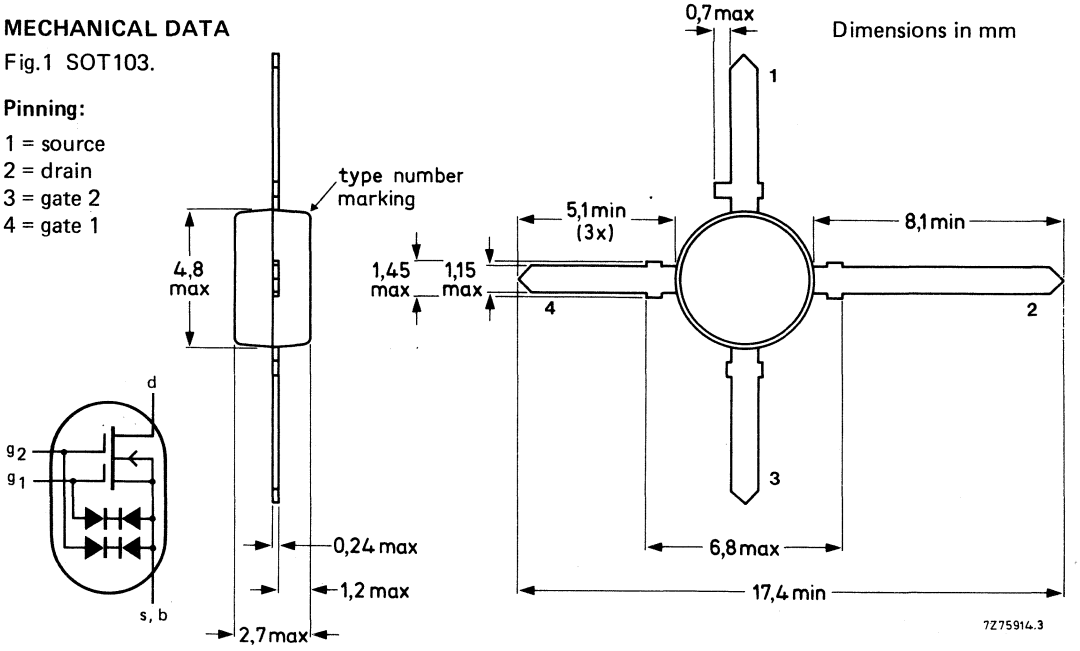
MECHANICAL DATA

Fig.1 SOT103.

Dimensions in mm

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1



FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for VHF applications in television tuners. The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain-current	I_D	max.	30	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	18	mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.5 3.0	pF pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.0	dB

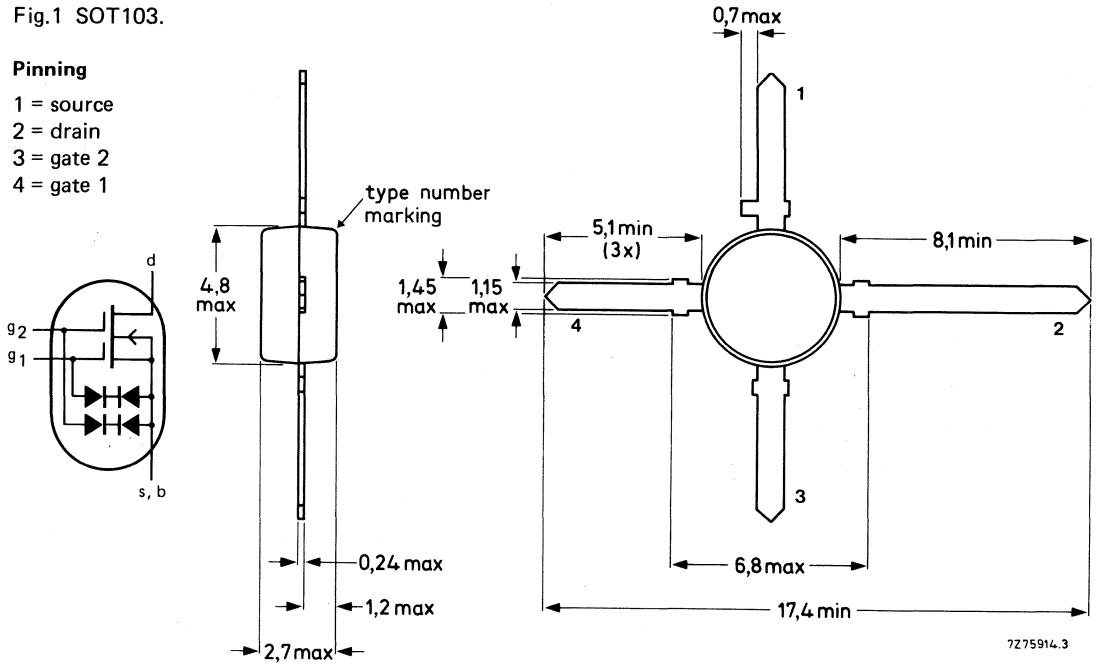
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT103.

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in plastic X-package with source and substrate interconnected, intended for VHF applications, such as VHF television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source and has an integrated drain resistance to suppress oscillation in the frequency range higher than 1 GHz.

This device is especially intended for use in pre-amplifiers in CATV tuners with large tuning ranges up to 500 MHz.

QUICK REFERENCE DATA

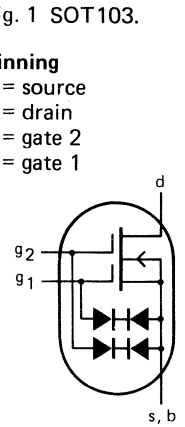
Drain-source voltage	V_{DS}	max.	20 V
Drain-current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	18 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	2,5 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_{Sopt} I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1,0 dB

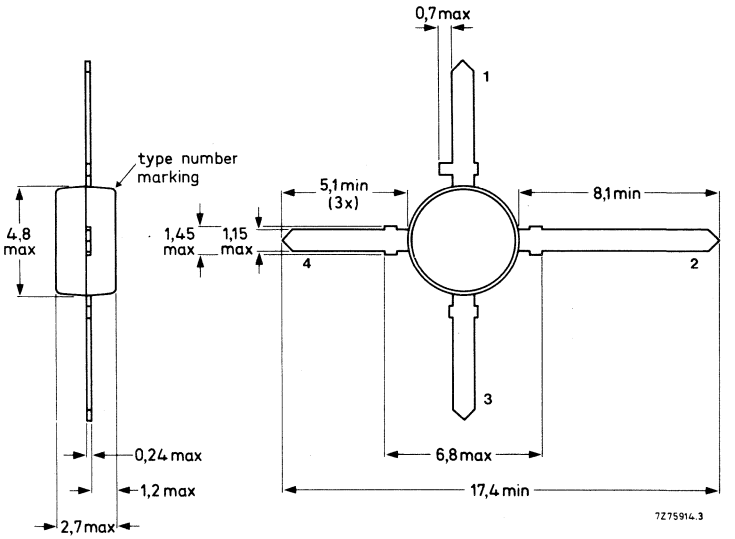
MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT103.

Pinning
1 = source
2 = drain
3 = gate 2
4 = gate 1





FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for u.h.f. applications in television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	18 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.3 pF 2.6 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 3.3 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	1.8 dB

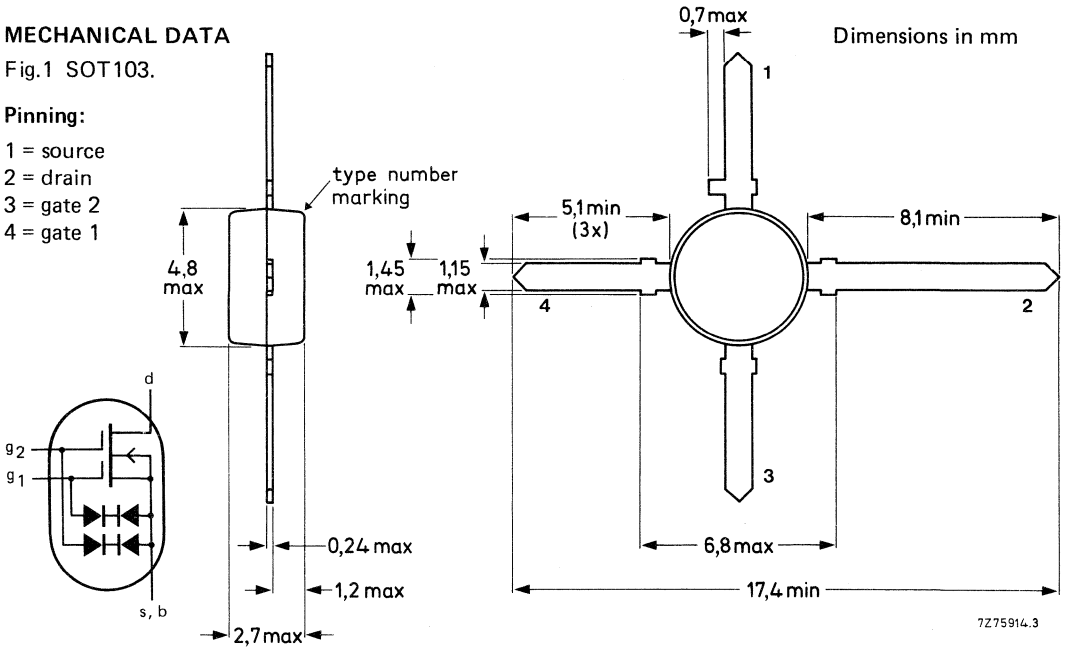
MECHANICAL DATA

Fig.1 SOT103.

Dimensions in mm

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1



FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected. Intended for UHF applications, such as UHF television tuners, with 12 V supply voltage and professional communication equipment.
This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	18	V
Drain current (DC)	I_D	max.	30	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	19	mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ. max.	2.6 3.0	pF pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 5 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	2.0	dB

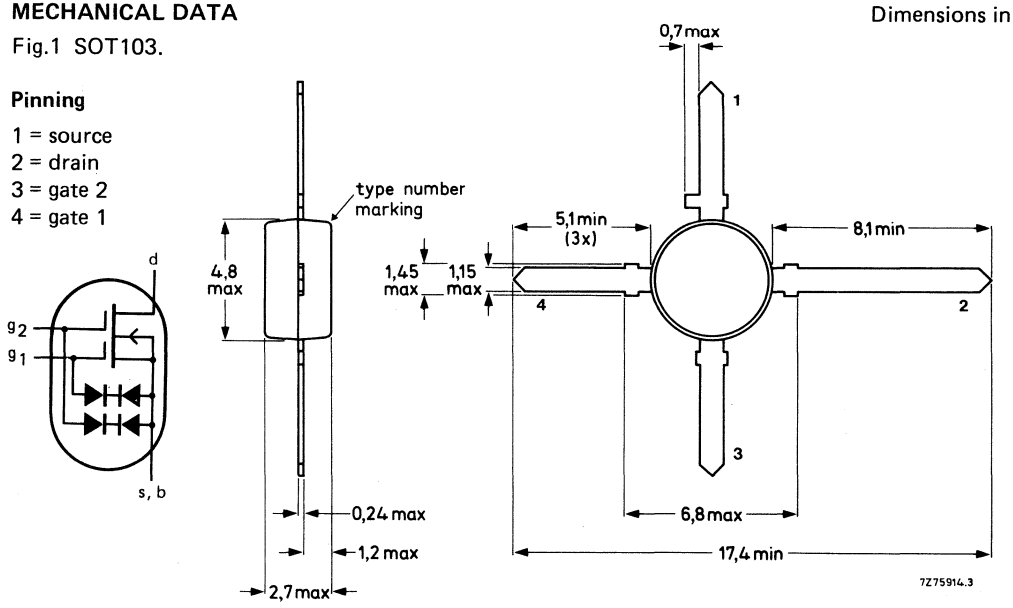
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT103.

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for VHF applications, such as VHF television tuners, FM tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	20 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	14 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	2.1 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	20 fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	0.7 dB

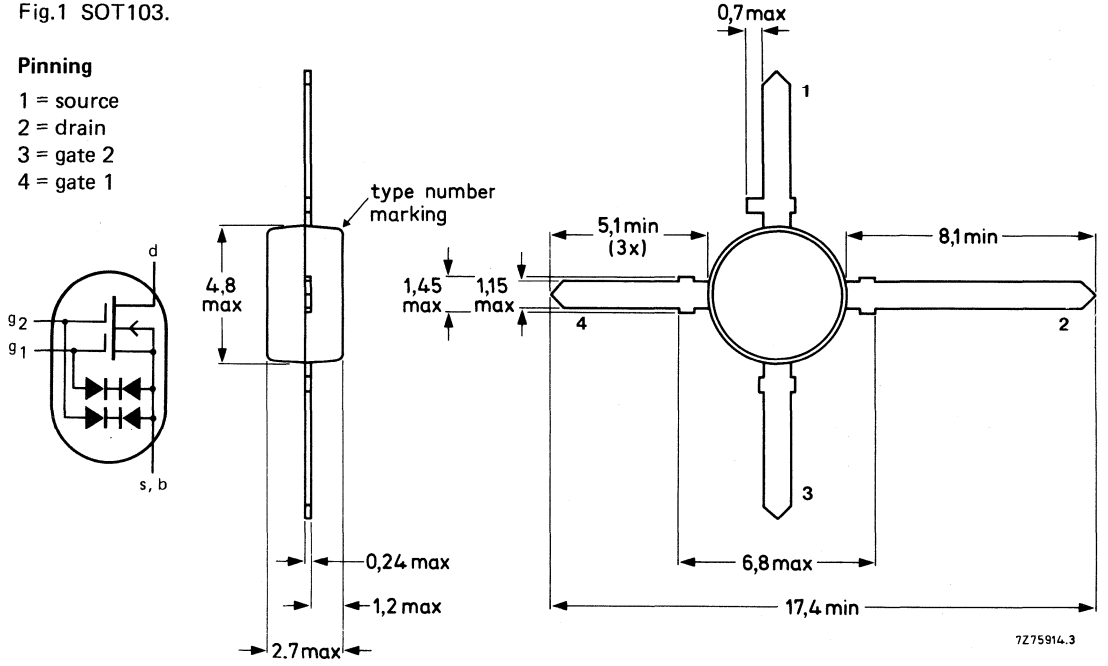
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT103.

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for VHF applications, such as VHF television tuners, FM tuners, with 12 V supply voltage.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	40 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 15 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$\lvert y_{fs} \rvert$	typ.	25 mS
Input capacitance at gate 1; f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{ig1-s}	typ.	4.0 pF
Feedback capacitance at f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{rs}	typ.	30 fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 15 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; f = 200 MHz	F	typ.	1.2 dB

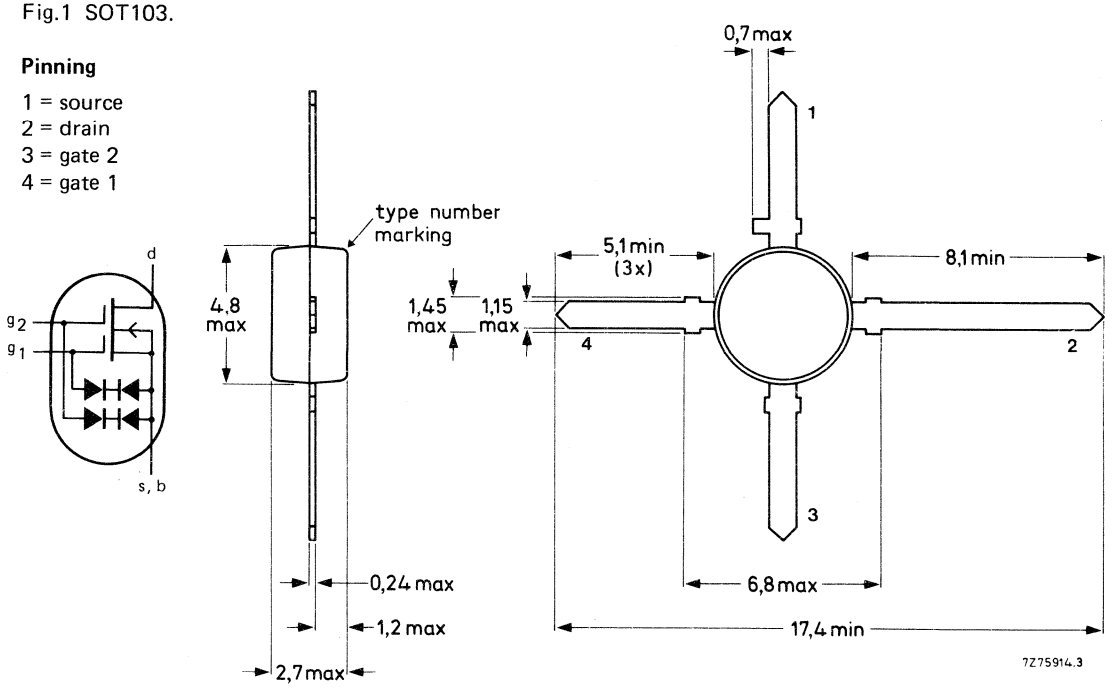
MECHANICAL DATA

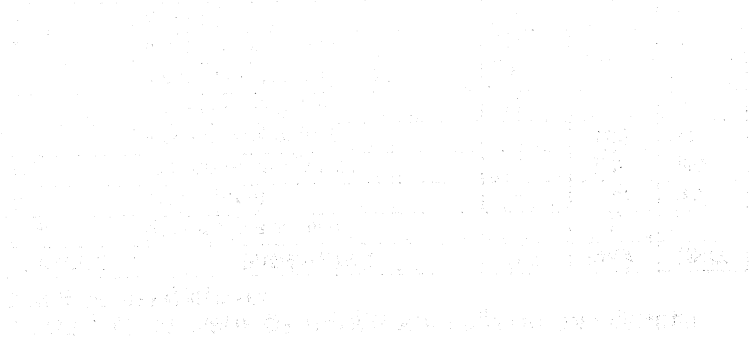
Dimensions in mm

Fig.1 SOT103.

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1





Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

BF988

Silicon n-channel dual gate MOS-FET

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

FEATURES

- Short channel transistor with high ratio $|Y_{fs}|/C_{is}$.
- Low noise gain controlled amplifier to 1 GHz.

DESCRIPTION

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for VHF and UHF applications, such as television tuners, with 12 V supply voltage and professional communication equipment. This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage	-	12	V
I_D	drain current	-	30	mA
P_{tot}	total power dissipation	-	225	mW
T_j	junction temperature	-	150	°C
$\|Y_{fs}\|$	transfer admittance	24	-	mS
C_{ig1-s}	input capacitance at gate 1	2.1	-	pF
C_{rs}	feedback capacitance	25	-	fF
F	noise figure	1	-	dB

Silicon n-channel dual gate MOS-FET BF988

MECHANICAL DATA

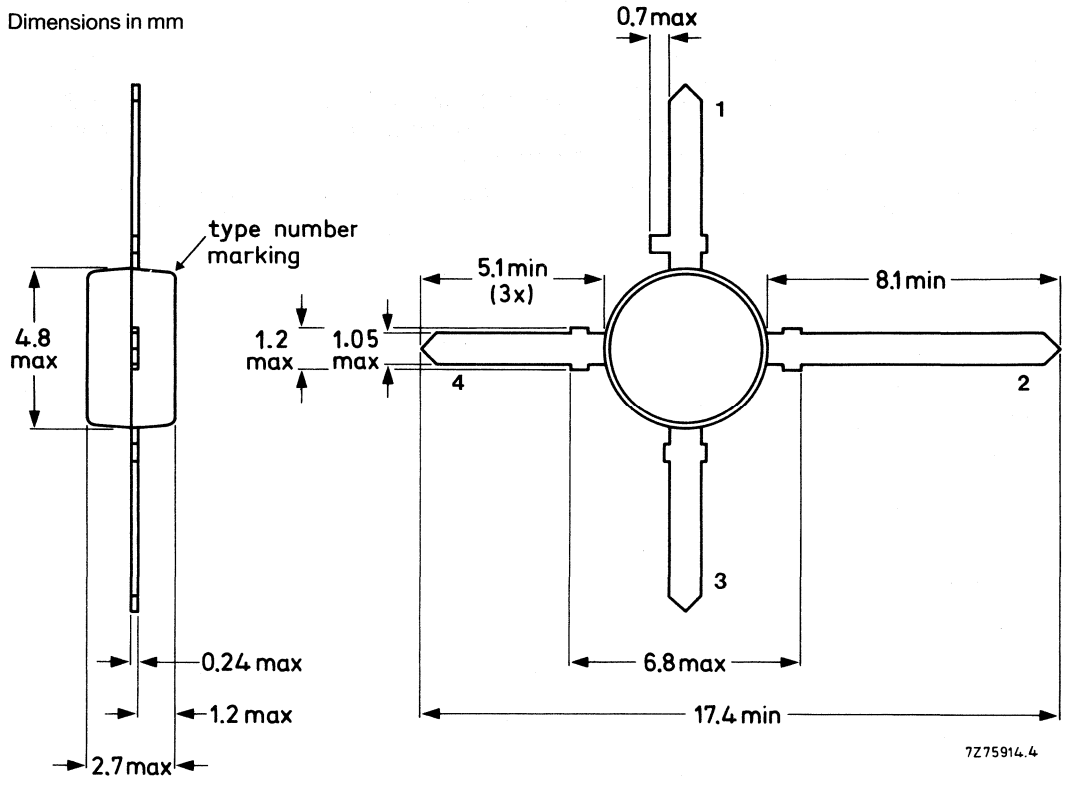


Fig.1 SOT103.

PIN CONFIGURATION

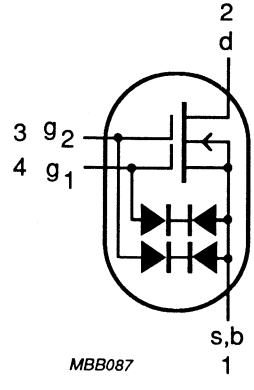


Fig.2 Pin configuration.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in u.h.f. applications in television tuners. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	20 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$\lvert y_{fs} \rvert$	typ.	12 mS
Input capacitance at gate 1; f = 1 MHz I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{ig1-s}	typ.	1.8 pF
Feedback capacitance at f = 1 MHz I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; f = 800 MHz	F	typ.	2.8 dB

MECHANICAL DATA

Fig.1 SOT143.

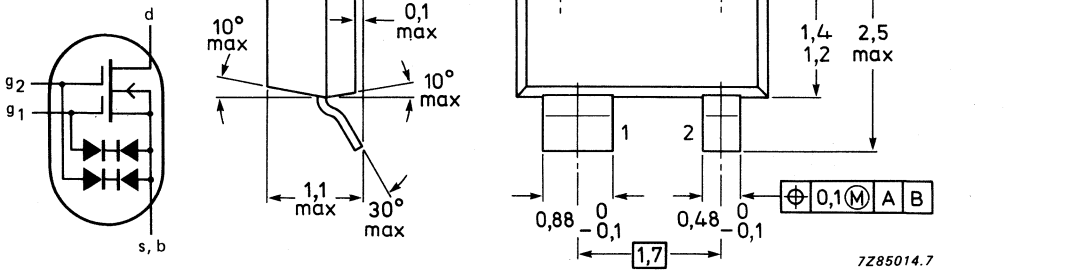
Dimensions in mm

Marking code:

BF989 = MAp

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

See also *Soldering recommendations.*

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected, intended for UHF applications, such as UHF television tuners with 12 V supply voltage and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	18 V
Drain current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	19 mS
Input capacitance at gate; f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.6 pF 3.0 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ. max.	2.0 dB 3.0 dB

MECHANICAL DATA

Fig.1 SOT143.

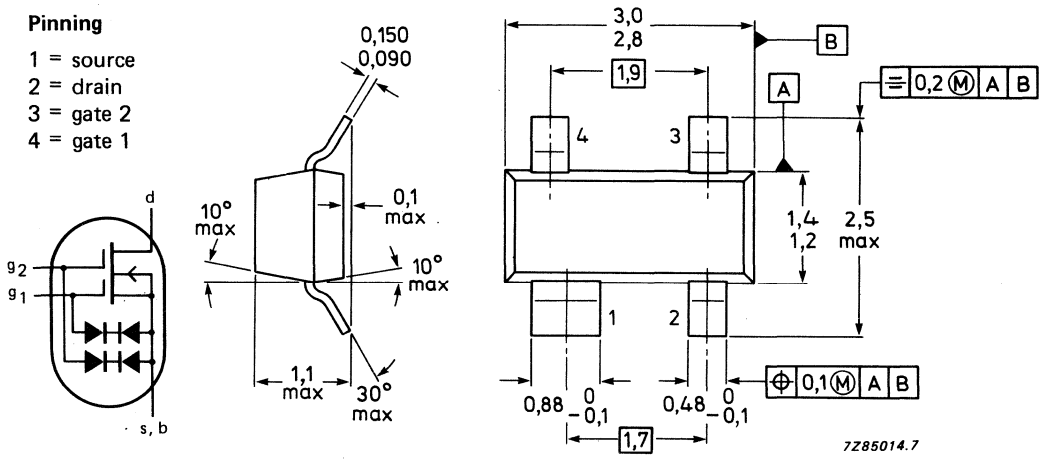
Marking code

BF990A = M87

Dimensions in mm

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

See also *Soldering recommendations.*

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in v.h.f. applications, such as v.h.f. television tuners and f.m. tuners. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	20	mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	14	mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	2,1	pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	20	fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	0,7	dB

MECHANICAL DATA

Fig.1 SOT143.

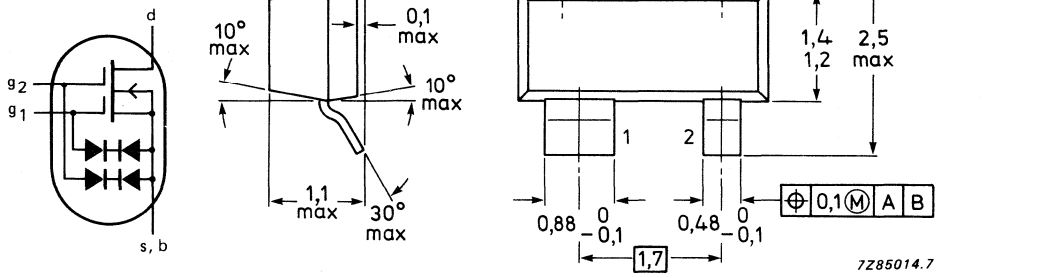
Dimensions in mm

Marking code

BF991 = M91

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

See also *Soldering recommendations.*

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in v.h.f. applications, such as v.h.f. television tuners, FM tuners with a 12 volt supply voltage. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	40 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	25 mS
Input capacitance at gate 1; f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	4 pF
Feedback capacitance at f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	30 fF
Noise figure at G_S = 2 mS I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.2 dB

MECHANICAL DATA

Fig.1 SOT143.

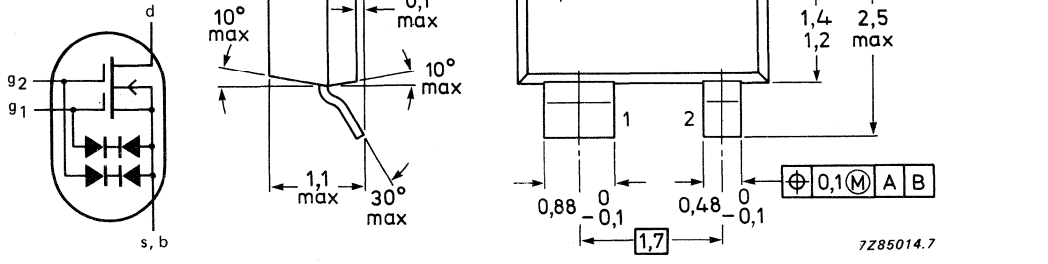
Dimensions in mm

Marking code:

BF992 = M92

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

See also *Soldering recommendations.*

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected and intended for VHF applications in television tuners.
The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	50 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	18 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.5 pF 3.0 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.0 dB

MECHANICAL DATA

Fig.1 SOT143.

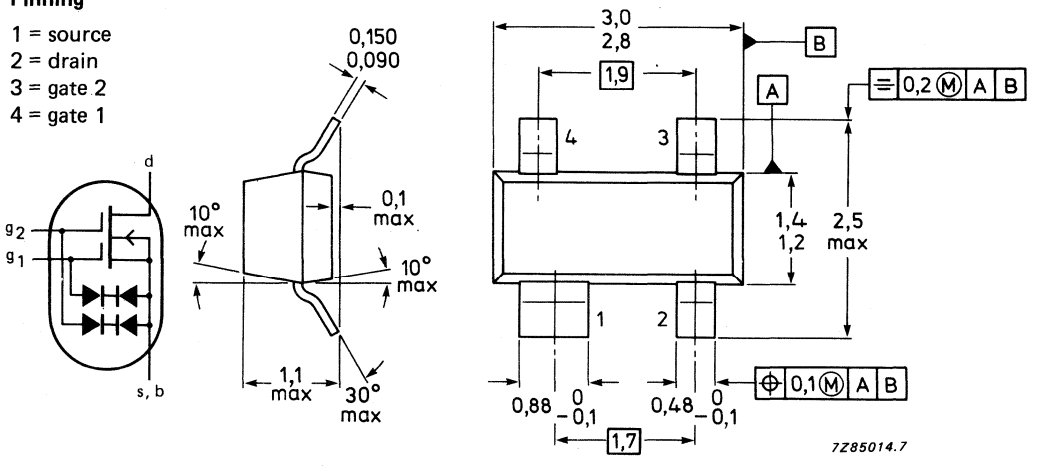
Dimensions in mm

Marking code

BF994S = MGp

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

See also *Soldering recommendations.*

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected and intended for UHF applications in television tuners.
The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates ans source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V	$\lvert y_{fs} \rvert$	typ.	18 mS
Input capacitance at gate 1 : f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V	C_{ig1-s}	typ. max.	2.3 pF 2.6 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V; f = 200 MHz	F	typ.	1.8 dB

MECHANICAL DATA

Dimensions in mm

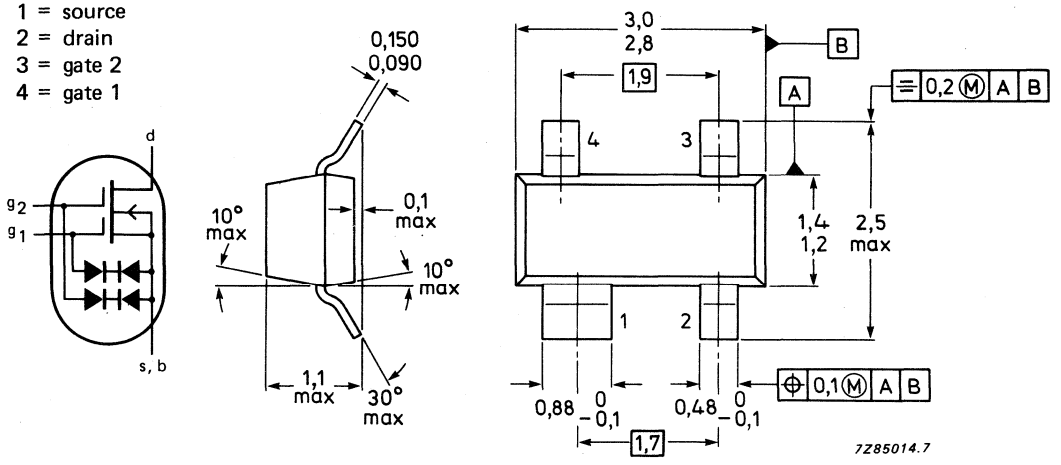
Fig.1 SOT143.

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1

Marking code

BF996S = MHp



TOP VIEW

See also *Soldering recommendations.*

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected, intended for u.h.f. and v.h.f. applications, such as u.h.f./v.h.f. television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source and has an integrated drain resistance to suppress oscillation in the frequency range higher than 1 GHz.

This device is especially intended for use in pre-amplifiers in CATV tuners with a large tuning range up to 500 MHz.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V	$\lvert y_{fs} \rvert$	typ.	18 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V	C_{ig1-s}	typ.	2.5 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V; f = 200 MHz	F	typ.	1.0 dB

MECHANICAL DATA

Fig.1 SOT143.

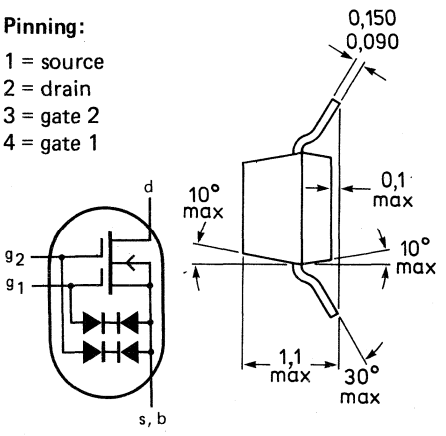
Dimensions in mm

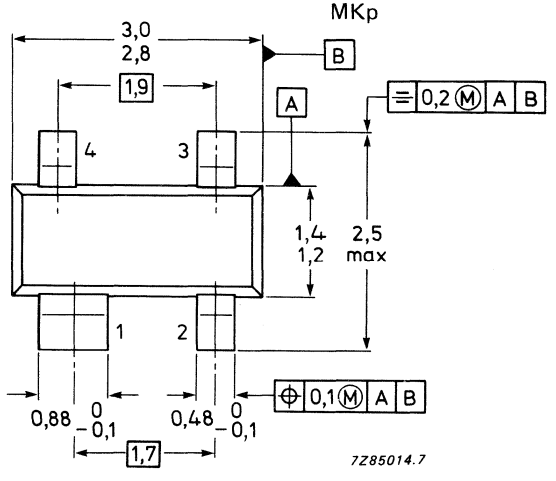
Marking code:

MKp

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1





TOP VIEW

See also *Soldering recommendations.*

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	April 1991

BF998

Silicon n-channel dual gate MOS-FET

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATASHEET

FEATURES

- Short channel transistor with high ratio $|Y_{fs}|/C_{is}$.
- Low noise gain controlled amplifier to 1 GHz.

DESCRIPTION

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected, intended for VHF and UHF applications, such as television tuners, with 12 V supply voltage and professional communication equipment. This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage	-	12	V
I_D	drain current	-	30	mA
P_{tot}	total power dissipation	-	200	mW
T_j	junction temperature	-	150	°C
$\|Y_{fs}\|$	transfer admittance	24	-	mS
C_{ig1-s}	input capacitance at gate 1	2.1	-	pF
C_{rs}	feedback capacitance	25	-	fF
F	noise figure at 800 MHz	1	-	dB

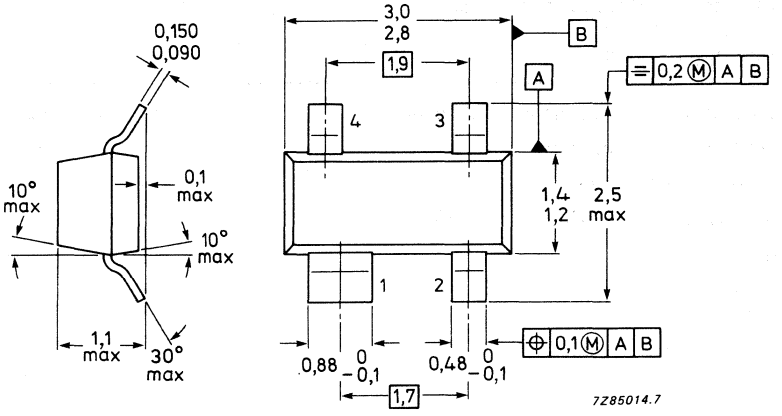
Silicon n-channel dual gate MOS-FET BF998

MECHANICAL DATA

Dimensions in mm

Marking code

BF998 = MOp



TOP VIEW

See also soldering recommendations.

Fig.1 SOT143.

PIN CONFIGURATION

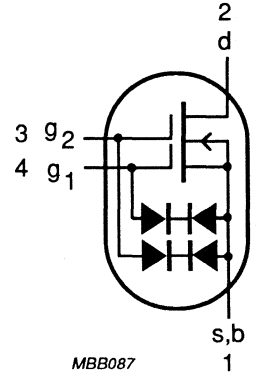


Fig.2 Pin configuration.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC14 OR DATASHEET

N-P-N 4 GHz WIDEBAND TRANSISTOR

N-P-N transistor in a plastic SOT-23 envelope. It is intended for a wide range of v.h.f. and u.h.f. applications in thick and thin-film circuits.

QUICK REFERENCE DATA

Collector-base voltage (open emitter; peak value)	V_{CBOM}	max.	25	V
Collector-emitter voltage (open base)	V_{CEO}	max.	15	V
Collector current (peak value)	I_{CM}	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Junction temperature	T_j	max.	150	°C
DC current gain I_C = 2 mA; V_{CE} = 1 V	h_{FE}	20 to 150		
Transition frequency I_C = 25 mA; V_{CE} = 5 V; f = 500 MHz	f_T	typ.	1.3	GHz
Noise figure I_C = 2 mA; V_{CE} = 5 V; R_S = 50 Ω; f = 500 MHz	F	typ.	4.5	dB

MECHANICAL DATA

Fig. 1 SOT-23.

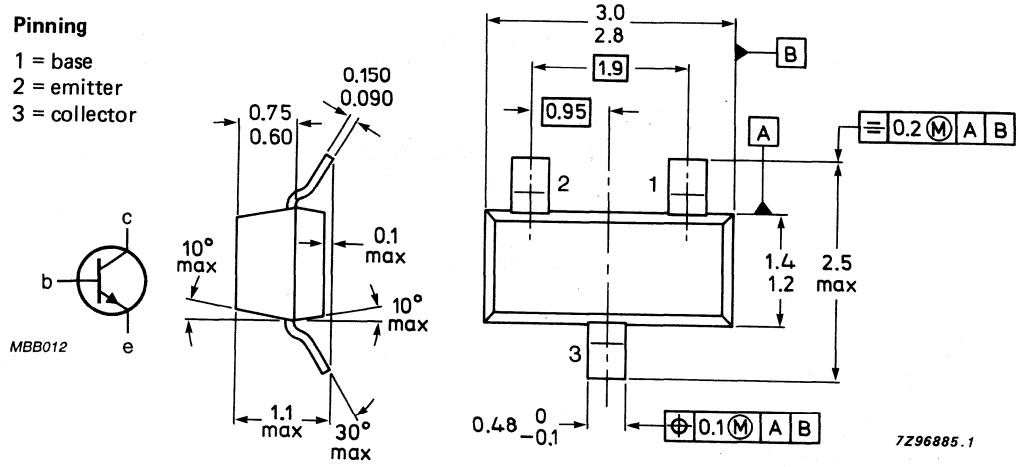
Dimensions in mm

Marking code

BFS17 = $E1_p$

Pinning

1 = base
2 = emitter
3 = collector



TOP VIEW

If required, the R-version (reverse pinning) is available on request.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC14 OR DATASHEET

N-P-N 2 GHz WIDEBAND TRANSISTOR

N-P-N transistor in a plastic SOT-23 envelope. It is intended for a wide range of v.h.f. and u.h.f. applications in thick and thin-film circuits.

The BFS17A is the successor to the BFS17 and offers a higher power gain and an improved noise behaviour.

QUICK REFERENCE DATA

Collector-base voltage (open emitter)	V_{CBO}	max.	25	V
Collector-emitter voltage (open base)	V_{CEO}	max.	15	V
Collector current (DC)	I_C	max.	25	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Junction temperature	T_j	max.	150	°C
D.C. current gain				
I_C = 2 mA; V_{CE} = 1 V	h_{FE}	min.	20	
		max.	150	
Transition frequency at f = 500 MHz				
I_C = 25 mA; V_{CE} = 5 V	f_T	typ.	2.8	GHz
Noise figure				
I_C = 2 mA; V_{CE} = 5 V; f = 800 MHz	F	typ.	2.5	dB
Output voltage at d_{im} = −60 dB				
V_{CE} = 10 V; I_C = 14 mA; Z_L = 75 Ω				
$f_{(p+q-r)}$ = 793.25 MHz	V_o	typ.	150	mV
Maximum unilateral power gain at f = 800 MHz				
V_{CE} = 10 V; I_C = 14 mA	G_{UM}	typ.	13.5	dB

MECHANICAL DATA (see Fig. 1).

If required, the R-version (reverse pinning) is available on request.

MECHANICAL DATA

Fig. 1 SOT-23.

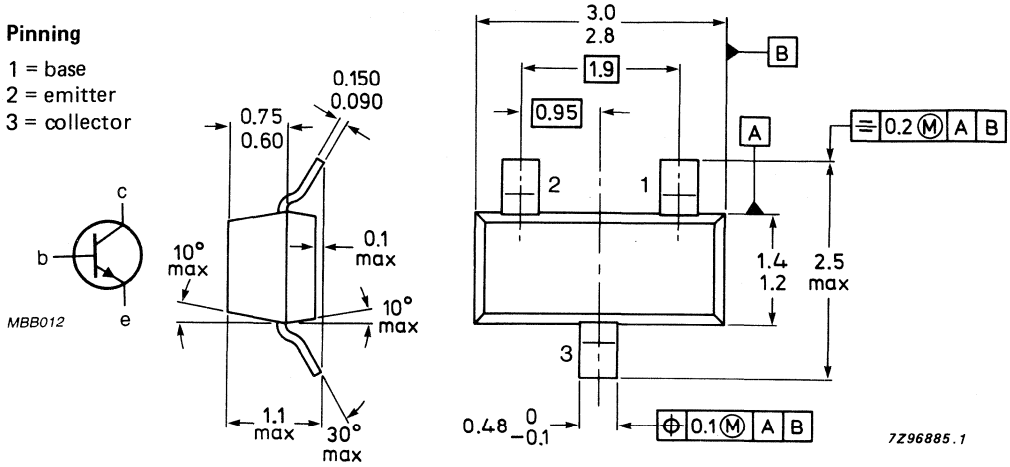
Dimensions in mm

Marking code

BFS17A = E2

Pinning

1 = base
2 = emitter
3 = collector



TOP VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-base voltage (open emitter)	V_{CBO}	max.	25 V
Collector-emitter voltage (open base)	V_{CEO}	max.	15 V
Emitter-base voltage (open collector)	V_{EBO}	max.	2.5 V
Collector current (DC)	I_C	max.	25 mA
Collector current (peak value)	I_{CM}	max.	50 mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	300 mW
Storage temperature	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$	=	430 K/W

* Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

PARALLEL EFFICIENCY DIODE

Double-diffused passivated rectifier diode in an hermetically sealed axial-leaded glass envelope, intended for use as efficiency diode in transistorized horizontal deflection circuits of television receivers. The device features high reverse voltage capability with controlled recovery time.

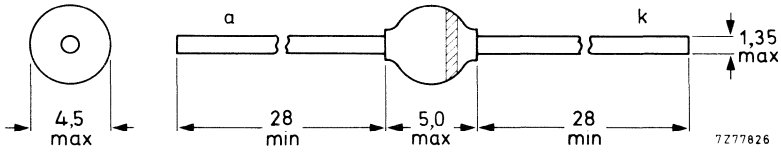
QUICK REFERENCE DATA

Repetitive peak reverse voltage	V_{RRM}	max.	1500 V
Working peak forward current	I_{FWM}	max.	5 A
Repetitive peak forward current	I_{FRM}	max.	10 A
Total reverse recovery time	t_{tot}	<	20 μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-64.



The marking band indicates the cathode.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

32 kHz PARALLEL EFFICIENCY DIODE

Double-diffused glass passivated rectifier diode in an hermetically sealed axial-leaded glass envelope, intended for use as an efficiency diode in transistorized horizontal deflection circuits of television receivers with line frequency up to 32 kHz. The device features high reverse voltage capability with controlled recovery time and fast turn-on.

QUICK REFERENCE DATA

Repetitive peak reverse voltage	V_{RRM}	max.	1400 V
Working peak forward current	I_{FWM}	max.	6 A
Repetitive peak forward current	I_{FRM}	max.	10 A
Total reverse recovery time	t_{tot}	max.	13 μs

MECHANICAL DATA

Dimensions in mm

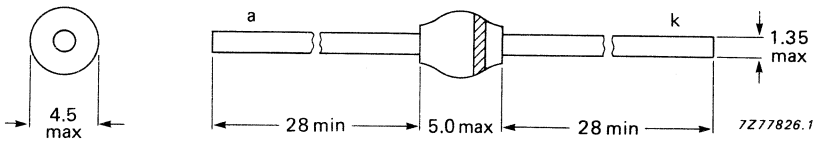


Fig. 1 SOD-64.

The marking band indicates the cathode.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

SILICON E.H.T. AVALANCHE RECTIFIER DIODES *

E.H.T. rectifier diodes in glass envelopes. For use in high-voltage applications such as multipliers, especially in diode-split transformers. The devices feature non-snap-off characteristics and are capable of absorbing avalanche energy e.g. during flashover in a picture tube. Because of the small envelope, the diode should be used in a suitable insulating medium (resin, oil or special arrangements in test-cases).

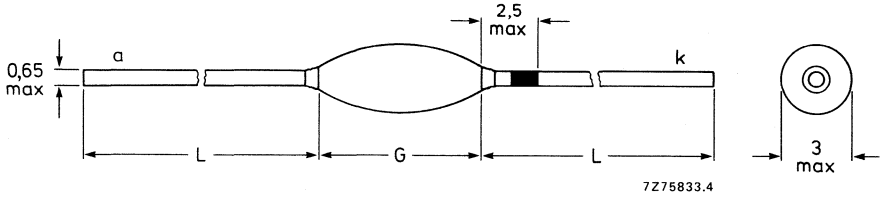
QUICK REFERENCE DATA

			BY609	BY610	
Working reverse voltage	V_{RW}	max.	12	12	kV
Repetitive peak reverse voltage	V_{RRM}	max.	15	17	kV
Average forward current	$I_{F(AV)}$	max.	4		mA
Junction temperature	T_j	max.	120		°C
Reverse recovery charge	Q_s	<	1		nC
Reverse recovery time	t_{rr}	typ.	0,2		μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-61.
L = 29,5 min.
G = 8,9 max.



The cathode of the BY609 is indicated by a yellow band on the lead.
The cathode of the BY610 is indicated by an orange band on the lead.

*See also "Custom made E.H.T. stacks" in section "General".

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

MINIATURE HIGH-VOLTAGE SOFT-RECOVERY RECTIFIER DIODE

Glass-passivated rectifier diode in a miniature hermetically sealed axial-leaded glass envelope. It is intended as a general purpose rectifier for high frequencies and high voltages and owing to its small size this diode is extremely suitable for mounting in miniature assemblies, such as voltage multipliers.

Because of the small envelope, the diode should be well insulated (insulating material: resin, oil or with special arrangements in test cases-SF6 gas).

QUICK REFERENCE DATA

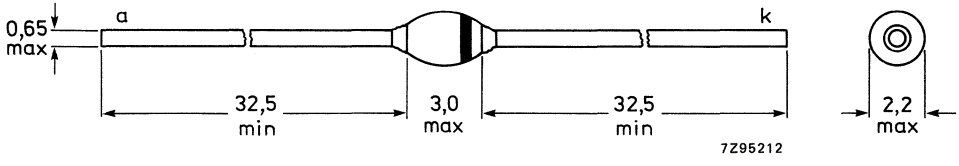
Working reverse voltage	V_{RW}	max.	2000	V
Repetitive peak reverse voltage	V_{RRM}	max.	2200	V
Average forward current	$I_{F(AV)}$	max.	50	mA
Repetitive peak forward current	I_{FRM}	max.	500	mA
Junction temperature	T_j	max.	150	°C
Reverse recovery time	t_{rr}	<	300	ns

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-61H2.

L = 32,5 min.
G = 3,0 max.



The cathode is indicated by a coloured band.

EHT avalanche very fast soft-recovery diodes

BY617

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

FEATURES

- Soft-recovery (non snap-off) characteristics
- Capable of absorbing avalanche energy e.g. during flashover in picture tubes
- Low reverse switching losses.

DESCRIPTION

EHT rectifier diodes in hermetically-sealed, axially-leaded glass envelope and designed for colour TV and monitor applications with frequencies up to 128 kHz. They are suitable for use in high voltage applications such as multipliers and especially in layer-wound diode-split-transformers where controlled avalanche energy capabilities are required.

Because of the small envelope, the diode should be used in a suitable insulating medium (resin, oil or SF6 gas).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{RW}	reverse working voltage	–	7.5	kV
V_{RRM}	repetitive peak reverse voltage	–	9	kV
$I_{F(AV)}$	average forward current	–	4	mA
Q_s	reverse recovery charge	–	0.4	nC
t_{rr}	reverse recovery time	100	–	ns
T_j	junction temperature	–	120	°C

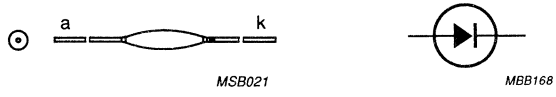


Fig.1 Simplified outline (SOD61) and symbol.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

E.H.T. AVALANCHE VERY FAST SOFT-RECOVERY DIODES *

E.H.T. rectifier diodes in hermetically-sealed, axially-leaded glass envelope and designed for c.t.v. and monitor applications with frequencies up to 128 kHz. They are suitable for use in high-voltage application such as multipliers and especially in diode-split transformers.

Because of the small envelope, the diode should be used in a suitable insulating medium (resin, oil or SF6 gas).

Features:

- Non-snap-off characteristics;
- Capable of absorbing avalanche energy e.g. during flash-over in picture tubes.

QUICK REFERENCE DATA

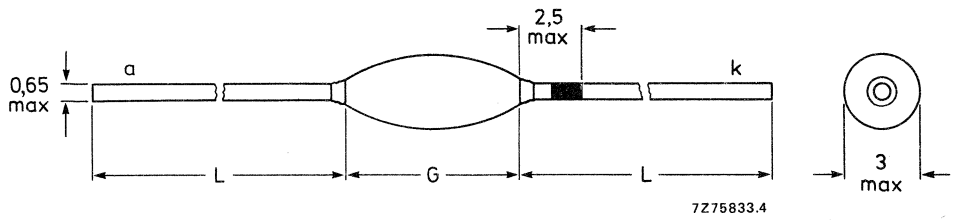
			BY619	BY620	
Working reverse voltage	V_{RW}	max.	12	12	kV
Repetitive peak reverse voltage	V_{RRM}	max.	15	17	kV
Average forward current	$I_{F(AV)}$	max.	4		mA
Junction temperature	T_j	max.	120		°C
Reverse recovery charge	Q_s	<	0,4		nC
Reverse recovery time	t_{rr}	typ.	100		ns

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-61.

L = 28 min.
G = 11 max.



The BY619 cathode is indicated by a curry yellow band on the lead.
The BY620 cathode is indicated by a lilac band on the lead.

*See also "Custom made E.H.T. stacks" in section "General".

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

CONTROLLED AVALANCHE RECTIFIER DIODES

Glass passivated rectifier diode in hermetically sealed axial-leaded ID* envelope capable of absorbing reverse transients, intended for rectifier applications in colour television circuits as well as general purpose applications in telephony equipment.

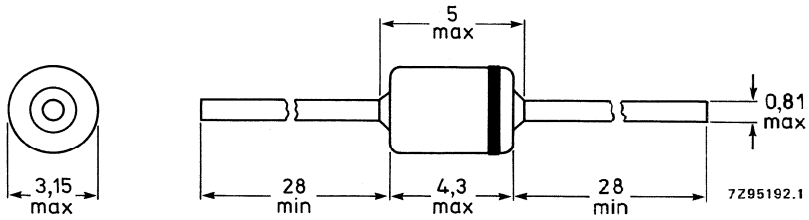
QUICK REFERENCE DATA

Crest working voltage	V_{RWM}	max.	800 V
Repetitive peak reverse voltage	V_{RRM}	max.	1250 V
Average forward current	$I_{F(AV)}$	max.	2 A
Non-repetitive peak forward current	I_{FSM}	max.	50 A
Non-repetitive peak reverse avalanche energy	E_{RSM}	max.	40 mJ
Junction temperature	T_j	max.	175 °C

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-84.



The marking band indicates the cathode.

* Implosion Diode.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

SILICON EHT SOFT-RECOVERY RECTIFIER DIODES

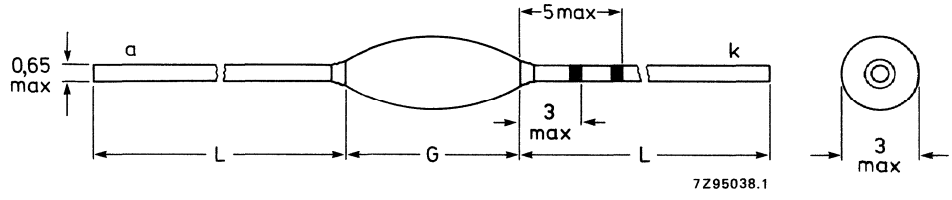
EHT rectifier diodes in glass envelopes intended for use in general purpose high-voltage applications. The devices feature non-snap-off characteristics. Because of the small envelope, the diodes should be used in a suitable insulating medium (resin, oil or special arrangements in test cases).

QUICK REFERENCE DATA

			BY705	BY706	
Working reverse voltage	V_{RW}	max.	4.0	5.0	kV
Repetitive peak reverse voltage	V_{RRM}	max.	5.0	6.0	kV
Average forward current	$I_{F(AV)}$	max.	20		mA
Junction temperature	T_j	max.	120		°C
Reverse recovery charge	Q_s	<	1.0		nC
Reverse recovery time	t_{rr}	typ.	0.2		μs

MECHANICAL DATA

Dimensions in mm



L = 28 min.
G = 5.5 max.

The BY705 cathode is indicated by two brown bands on the lead.
The BY706 cathode is indicated by a brown band on the lead.

Fig. 1 SOD-61.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

SILICON E.H.T. SOFT-RECOVERY RECTIFIER DIODES*

E.H.T. rectifier diodes in glass envelopes intended for use in high-voltage applications such as the high-voltage supply of television receivers and monitors. The devices feature non-snap-off characteristics. Because of the small envelope, the diodes should be used in a suitable insulating medium (resin, oil or special arrangements in test-cases).

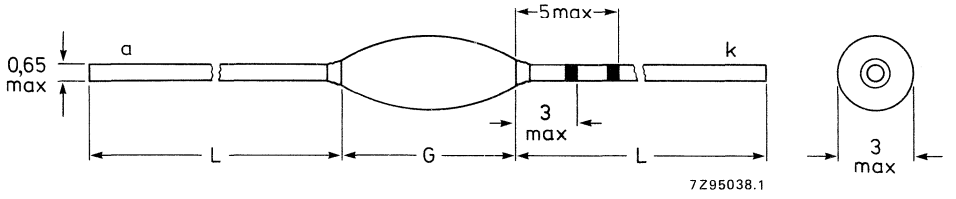
QUICK REFERENCE DATA

			BY707	708	709	
Working reverse voltage	V_{RW}	max.	9	10	12	kV
Repetitive peak reverse voltage	V_{RRM}	max.	10	12	14	kV
Average forward current	$I_{F(AV)}$	max.		4		mA
Junction temperature	T_j	max.		120		°C
Reverse recovery charge	Q_s	<		1		nC
Reverse recovery time	t_{rr}	typ.		0,2		μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-61.
L = 29 min.
G = 9,5 max.



The cathode of the BY707 is indicated by two red bands on the lead.
The cathode of the BY708 is indicated by a red band on the lead.
The cathode of the BY709 is indicated by a red band (inner) and a violet band (outer) on the lead.

*See also "Custom made E.H.T. stacks" in section "General".

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

SILICON E.H.T. SOFT-RECOVERY RECTIFIER DIODES*

E.H.T. rectifier diodes in glass envelopes intended for use in high-voltage applications such as the high-voltage supply of television receivers and monitors. The devices feature non-snap-off characteristics. Because of the small envelope, the diodes should be used in a suitable insulating medium (resin, oil or special arrangements in test cases).

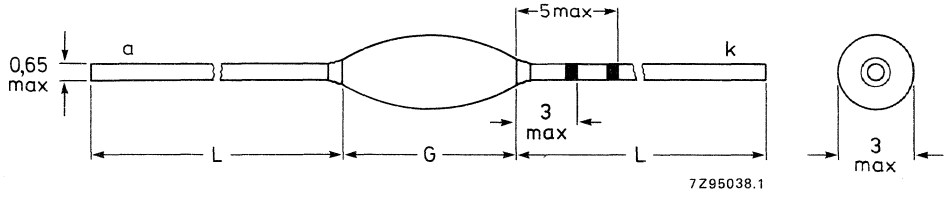
QUICK REFERENCE DATA

			BY710	711	
Working reverse voltage	V_{RW}	max.	14	16	kV
Repetitive peak reverse voltage	V_{RRM}	max.	17	19	kV
Average forward current	$I_{F(AV)}$	max.		3	mA
Junction temperature	T_j	max.		120	°C
Reverse recovery charge	Q_s	<		1	nC
Reverse recovery time	t_{rr}	typ.		0,2	μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-61.
L = 28 min.
G = 11 max.



The cathode of the BY710 is indicated by two green bands on the lead.
The cathode of the BY711 is indicated by a green band on the lead.

*See also "Custom made E.H.T. stacks" in section "General".

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

SILICON E.H.T. SOFT-RECOVERY RECTIFIER DIODES*

E.H.T. rectifier diodes in glass envelopes intended for use in high-voltage applications such as the high-voltage supply of television receivers and monitors. The devices feature non-snap-off characteristics. Because of the small envelope, the diodes should be used in a suitable insulating medium (resin, oil or special arrangements in test-cases).

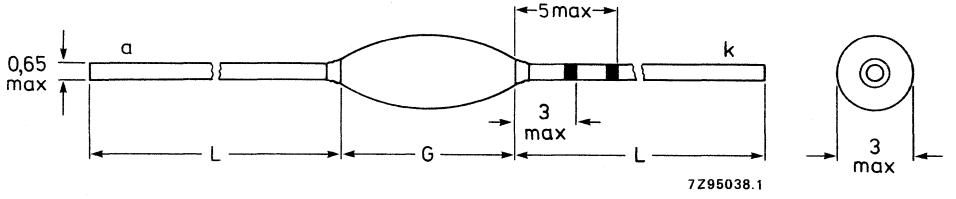
QUICK REFERENCE DATA

			BY712	713	714	
Working reverse voltage	V_{RW}	max.	18	20	24	kV
Repetitive peak reverse voltage	V_{RRM}	max.	22	24	30	kV
Average forward current	$I_{F(AV)}$	max.		3		mA
Junction temperature	T_j	max.		120		°C
Reverse recovery charge	Q_s	<		1		nC
Reverse recovery time	t_{rr}	typ.		0,2		μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-61.
L = 27 min.
G = 12,5 max.



The cathode of the BY712 is indicated by two blue bands on the lead.
The cathode of the BY713 is indicated by a blue band on the lead.
The cathode of the BY714 is indicated by a light blue band on the lead.

*See also "Custom made E.H.T. stacks" in section "General".

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

SILICON VERY FAST EHT SOFT-RECOVERY RECTIFIER DIODES

EHT rectifier diodes in glass envelopes intended for use in general purpose high-speed high-voltage applications. The devices feature non-snap-off characteristics. Because of the small envelope, the diodes should be used in a suitable insulating medium (resin, oil or special arrangements in test cases).

QUICK REFERENCE DATA

			BY715	BY716	
Working reverse voltage	V_{RW}	max.	4.0	5.0	kV
Repetitive peak reverse voltage	V_{RRM}	max.	5.0	6.0	kV
Average forward current	$I_{F(AV)}$	max.	20		mA
Junction temperature	T_j	max.	120		°C
Reverse recovery charge	Q_s	<	0.4		nC
Reverse recovery time	t_{rr}	typ.	100		ns

MECHANICAL DATA

Dimensions in mm

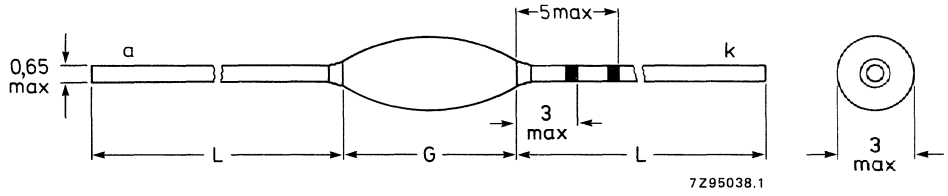


Fig. 1 SOD-61.

L = 28 min.
G = 5.5 max.

The BY715 cathode is indicated by a brown band (inner) and a green band (outer) on the lead.
The BY716 cathode is indicated by a brown band (inner) and a red band (outer) on the lead.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

SILICON VERY FAST EHT SOFT-RECOVERY RECTIFIER DIODES

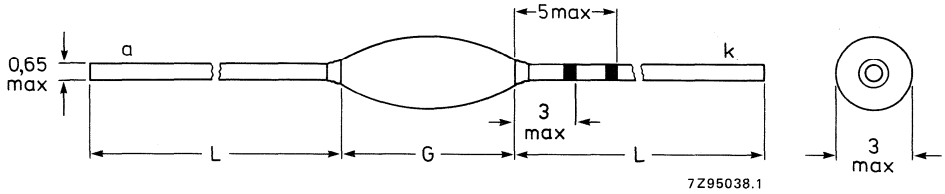
EHT rectifier diodes in glass envelopes intended for use in high-voltage applications e.g. the high-voltage supply of television receivers and monitors, at frequencies in excess of 30 kHz. The devices feature non-snap-off characteristics. Because of the small envelope, the diodes should be used in a suitable insulating medium (resin, oil or special arrangements in test cases).

QUICK REFERENCE DATA

			BY717	718	719	
Working reverse voltage	V_{RW}	max.	9.0	10	12	kV
Repetitive peak reverse voltage	V_{RRM}	max.	10	12	14	kV
Average forward current	$I_{F(AV)}$	max.		4.0		mA
Junction temperature	T_j	max.		120		°C
Reverse recovery charge	Q_s	<		0.4		nC
Reverse recovery time	t_{rr}	typ.		0.1		μs

MECHANICAL DATA

Dimensions in mm



L = 29 min.
G = 9.5 max.

The BY717 cathode is indicated by a red band (inner) and a green band (outer) on the lead.
The BY718 cathode is indicated by a red band (inner) and a blue band (outer) on the lead.
The BY719 cathode is indicated by a red band (inner) and a curry yellow band (outer) on the lead.

* See also "Custom made EHT stacks" in section "General".

Fig. 1 SOD-61.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

SILICON VERY FAST EHT SOFT-RECOVERY RECTIFIER DIODES*

EHT rectifier diodes in glass envelopes intended for use in high voltage applications such as the high voltage supply of television receivers and monitors at frequencies in excess of 30 kHz. The devices feature non-snap-off characteristics.
Because of the small envelope, the diodes should be used in a suitable insulating medium (resin, oil or special arrangements in test cases).

QUICK REFERENCE DATA

			BY720	BY721	
Working reverse voltage	V_{RW}	max.	14.0	16.0	kV
Repetitive peak reverse voltage	V_{RRM}	max.	17.0	19.0	kV
Average forward current	$I_{F(AV)}$	max.	3		mA
Junction temperature	T_j	max.	120		°C
Reverse recovery charge	Q_s	<	0.4		nC
Reverse recovery time	t_{rr}	typ.	100		ns

MECHANICAL DATA

Dimensions in mm

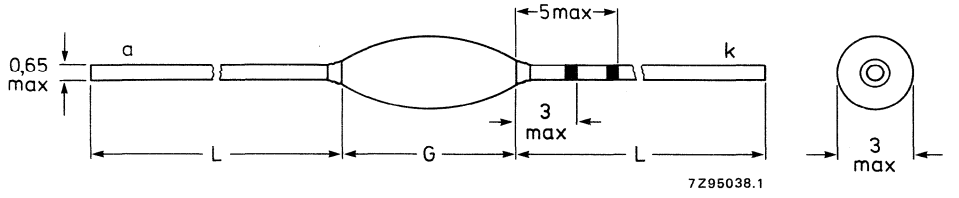


Fig. 1 SOD-61.

L = 28 min.
G = 11 max.

The BY720 cathode is indicated by a green band (inner) and a red band (outer) on the lead.
The BY721 cathode is indicated by a green band (inner) and a blue band (outer) on the lead.

* See also "Custom made EHT stacks" in section "General".

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

SILICON VERY FAST EHT SOFT-RECOVERY RECTIFIER DIODES*

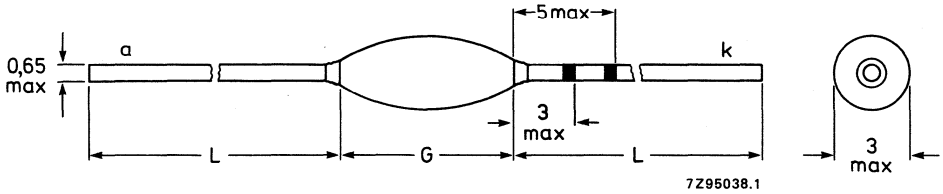
EHT rectifier diodes in glass envelopes intended for use in high-voltage applications e.g. the high-voltage supply of television receivers and monitors, at frequencies in excess of 30 kHz. The devices feature non-snap-off characteristics. Because of the small envelope, the diodes should be used in a suitable insulating medium (resin, oil or special arrangements in test cases).

QUICK REFERENCE DATA

			BY722	723	724	
Working reverse voltage	V_{RW}	max.	18	20	24	kV
Repetitive peak reverse voltage	V_{RRM}	max.	22	24	30	kV
Average forward current	$I_{F(AV)}$	max.		3.0		mA
Junction temperature	T_j	max.		120		°C
Reverse recovery charge	Q_s	max.		0.4		nC
Reverse recovery time	t_{rr}	typ.		0.1		μs

MECHANICAL DATA

Dimensions in mm



L = 27 min.
G = 12.5 max.

Fig. 1 SOD-61.

The BY722 cathode is indicated by a blue band (inner) and a red band (outer) on the lead.
The BY723 cathode is indicated by a blue band (inner) and a green band (outer) on the lead.
The BY724 cathode is indicated by a blue band (inner) and a curry yellow band (outer) on the lead.

* See also "Custom made EHT stacks" in section "General".

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

AVALANCHE FAST SOFT-RECOVERY RECTIFIER DIODES

Rectifier diodes in hermetically sealed axial-leaded ID* envelopes. They are intended for television and industrial applications, such as switched-mode power supplies, scan rectifiers in TV receivers and also for use in inverter and converter applications. The devices feature non-snap-off (soft-recovery) switching characteristics and are capable of absorbing reverse transient energy (e.g. during flashover in a picture tube).

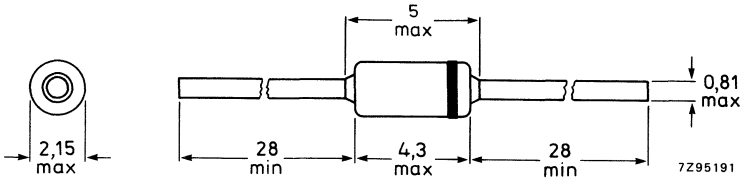
QUICK REFERENCE DATA

			BYD33D	G	J	K	M	
Repetitive peak reverse voltage	V_{RRM}	max.	200	400	600	800	1000	V
Continuous reverse voltage	V_R	max.	200	400	600	600	1000	V
Average forward current	$I_{F(AV)}$	max.		1,3		1,3		A
Non-repetitive peak forward current	I_{FSM}	max.		20		20		A
Non-repetitive peak reverse energy	E_{RSM}	max.		10		7		mJ
Reverse recovery time	t_{rr}	<		250		300		ns

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-81.



The marking band indicates the cathode.

* Implosion Diode.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

AVALANCHE FAST SOFT-RECOVERY RECTIFIER DIODES

Glass passivated rectifier diodes in hermetically sealed axial-leaded glass envelopes. They are intended for television and industrial applications, such as switched-mode power supplies, scan rectifiers in TV receivers, and also for use in inverter and converter applications. The devices feature non-snap-off (soft-recovery) switching characteristics and are capable of absorbing reverse transient energy (e.g. during flashover in the picture tube).

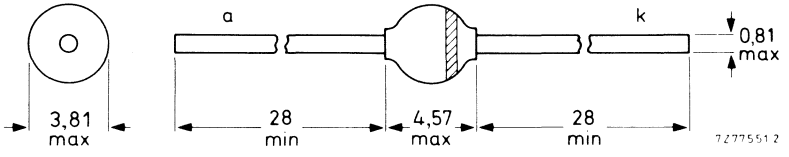
QUICK REFERENCE DATA

			BYV95A	B	C	
Repetitive peak reverse voltage	V_{RRM}	max.	200	400	600	V
Continuous reverse voltage	V_R	max.	200	400	600	V
Average forward current	$I_{F(AV)}$	max.		1,5		A
Non-repetitive peak forward current	I_{FSM}	max.		35		A
Non-repetitive peak reverse energy	E_{RSM}	max.		10		mJ
Reverse recovery time	t_{rr}	<		250		ns

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-57.



The marking band indicates the cathode.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

CONTROLLED AVALANCHE RECTIFIER DIODES

Double-diffused glass passivated rectifier diodes in hermetically sealed axial-leaded glass envelopes, capable of absorbing reverse transients.

They are intended for rectifier applications in colour television circuits as well as general purpose applications in telephony equipment.

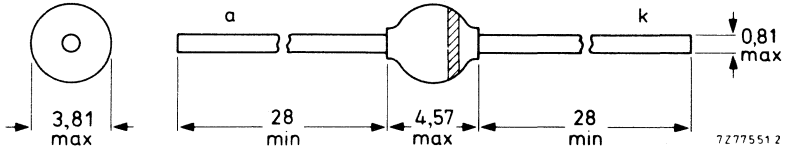
QUICK REFERENCE DATA

			BYW54	BYW55	BYW56	
Crest working reverse voltage	V_{RWM}	max.	600	800	1000	V
Reverse avalanche breakdown voltage	$V_{(BR)R}$	>	650	900	1100	V
		<	1000	1300	1600	V
Average forward current	$I_{F(AV)}$	max.	2	2	2	A
Non-repetitive peak forward current	I_{FSM}	max.		50		A
Non-repetitive peak reverse power dissipation	P_{RSM}	max.		1		kW
Junction temperature	T_j	max.		175		°C

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-57.



The marking band indicates the cathode.

Products approved to CECC 50 008-015.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATASHEET

CONTROLLED AVALANCHE RECTIFIER DIODES

Double-diffused glass passivated rectifier diodes in hermetically sealed axial-leaded glass envelopes, capable of absorbing reverse transients.

They are intended for rectifier applications as well as general purpose applications in television and communication equipment.

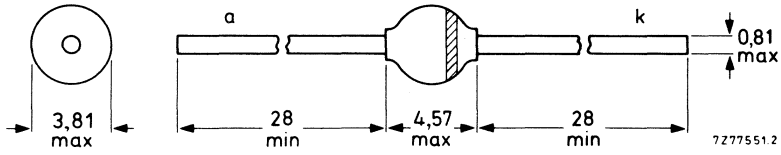
QUICK REFERENCE DATA

			1N5059	5060	5061	5062	
Crest working reverse voltage	V_{RWM}	max.	200	400	600	800	V
Reverse avalanche breakdown voltage	$V_{(BR)R}$	>	225	450	650	900	V
		<	1600	1600	1600	1600	V
Average forward current	$I_{F(AV)}$	max.	2,0				A
Non-repetitive peak forward current	I_{FSM}	max.	50				A
Non-repetitive peak reverse power dissipation	P_{RSM}	max.	1				kW
Junction temperature	T_j	max.	175				°C

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-57.



The marking band indicates the cathode.

Products approved to CECC 50 008-015.

Data sheet	
status	Product specification
date of issue	June 1990

FCB61C65(L/LL)

8 K x 8 Fast CMOS low-power static RAM

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC10 OR DATASHEET

FEATURES

- Operating supply voltage 5 V ± 10%
- Inputs and outputs ESD protected
- Automatic power-down after a completed read access
- Access time: 55 ns and 70 ns
- Low current consumption:
  - active 70 mA max.
  - standby (TTL) 3 mA max.
  - standby (CMOS) 100 µA max. (L-version)
  - standby (CMOS) 1 µA max. (LL-version)
- Suitable for battery back-up operation: (FCB61C65L/LL only)
  - data retention voltage 2 V min.
  - data retention current 50 µA max. (L-version)
  - data retention current 1 µA max. (LL-version)
- Latched data outputs giving stable data between consecutive accesses
- Easy memory expansion
- Common data I/O interface
- All inputs and outputs TTL and CMOS compatible
- All inputs have a Schmitt trigger switching action
- Three-state outputs
- Operating temperature 0 °C to +70 °C

GENERAL DESCRIPTION

The FCB61C65(L/LL) is a 65536-bit fast, low-power, static random access memory organized as 8192 words of 8 bits each.

The chip enable inputs $\overline{CE}1$ and CE2 are available for memory expansion and to control the low-power/ standby mode.

The device operates from a 5 V power supply and has an access time of 55 ns and 70 ns.

The FCB61C65(L/LL) is ideally suited for memory applications where fast access time, low power and ease of use are required.

The FCB61C65(L/LL) is a CMOS device which uses a 6 transistor memory cell.

The IC is fabricated in a CMOS double-metal single-poly process using ion-implanted silicon gate technology.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
FCB61C65 (L/LL)-XXP	28	DIL (600 mil)	plastic	SOT117
FCB61C65 (L/LL)-XXT	28	SOXL (330 mil)	plastic	SOT213

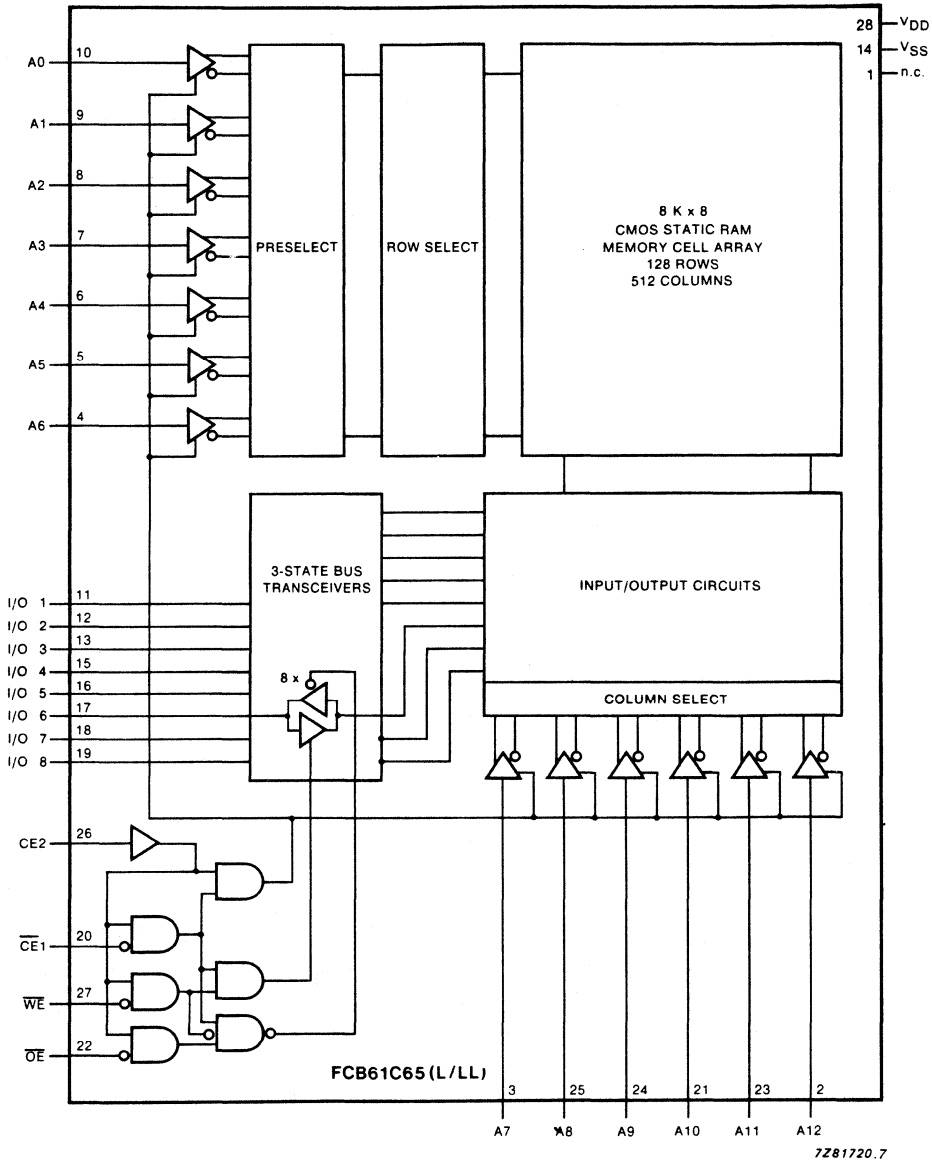


Fig.1 Block diagram.

Data sheet	
status	Product specification
date of issue	August 1990

FCF61C65(L/LL)

8 K x 8 Fast CMOS low-power static RAM for extended temperature range

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC10 OR DATASHEET

FEATURES

- Operating supply voltage 5 V ± 10%
- Inputs and outputs ESD protected
- Automatic power-down after a completed read access
- Access time: 85 ns
- Low current consumption:
  - active 60 mA max.
  - standby (TTL) 3 mA max.
  - standby (CMOS) 200 µA max. (L-version)
  - standby (CMOS) 4 µA max. (LL-version)
- Suitable for battery back-up operation: (FCF61C65L/LL only)
  - data retention voltage 2 V min.
  - data retention current 100 µA max. (L-version)
  - data retention current 4 µA max. (LL-version)
- Latched data outputs giving stable data between consecutive accesses
- Easy memory expansion
- Common data I/O interface
- All input and outputs TTL and CMOS compatible
- All inputs have a Schmitt trigger switching action
- Three-state outputs
- Operating temperature –40 °C to +85 °C

GENERAL DESCRIPTION

The FCF61C65(L/LL) is a 65536-bit, fast, low-power, static random access memory organized as 8192 words of 8 bits each.

The chip enable inputs $\overline{CE}1$ and CE2 are available for memory expansion and to control the lower-power/ standby mode.

The device operates from a 5 V power supply and has an access time of 85 ns.

The FCF61C65(L/LL) is ideally suited for memory applications for the extended temperature range of –40 to +85°C where fast access time, low power and ease of use are required.

The FCF61C65(L/LL) is a full CMOS device using a 6 transistor memory cell.

The IC is fabricated in a CMOS double-metal single-poly process using ion-implanted silicon gate technology.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
FCF61C65 (L/LL)-85T	28	SOXL (330 mil)	plastic	SOT213

8 K x 8 Fast CMOS low-power static RAM for extended temperature range

FCF61C65(L/LL)

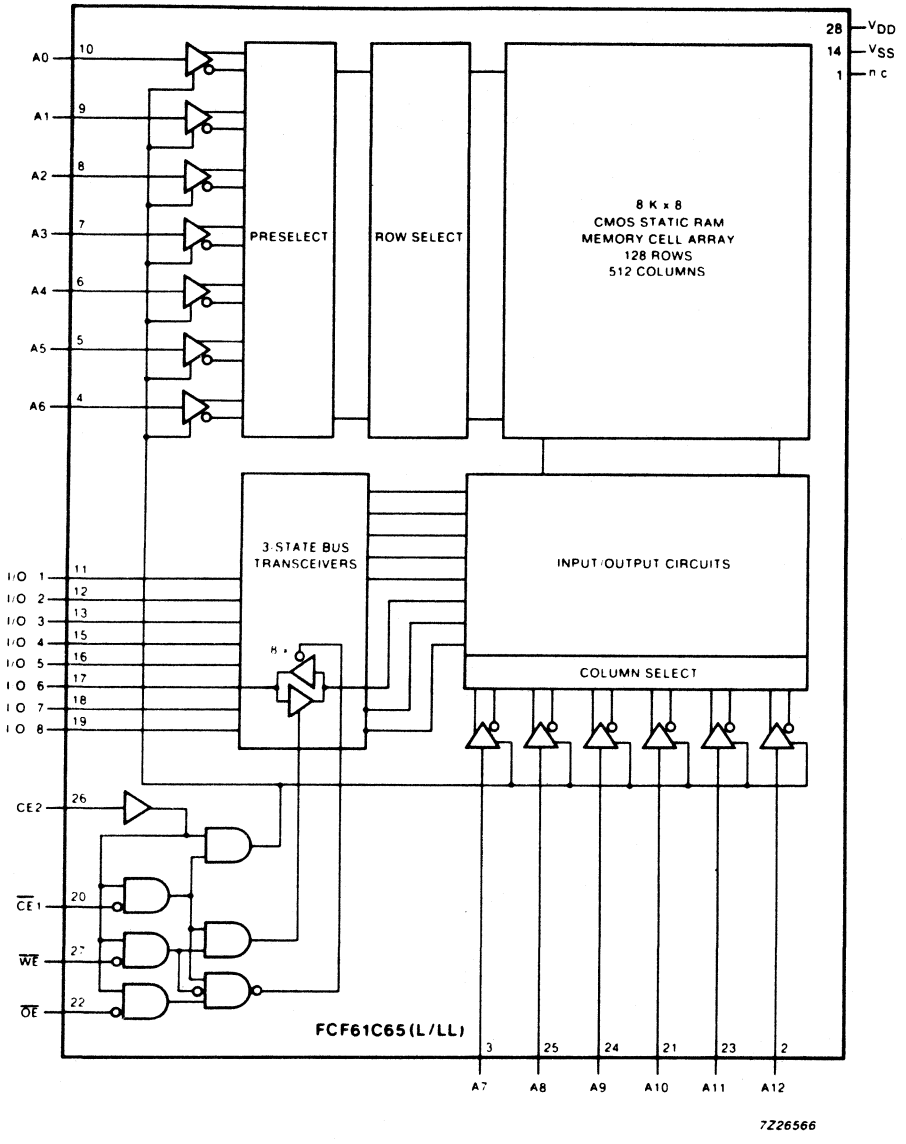


Fig.1 Block diagram.

NE/SA/SE592
Video Amplifier

Product Specification

DESCRIPTION

The NE/SA/SE592 is a monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers. Now available in an 8-pin version with fixed gain of 400 without external components and adjustable gain from 400 to 0 with one external resistor.

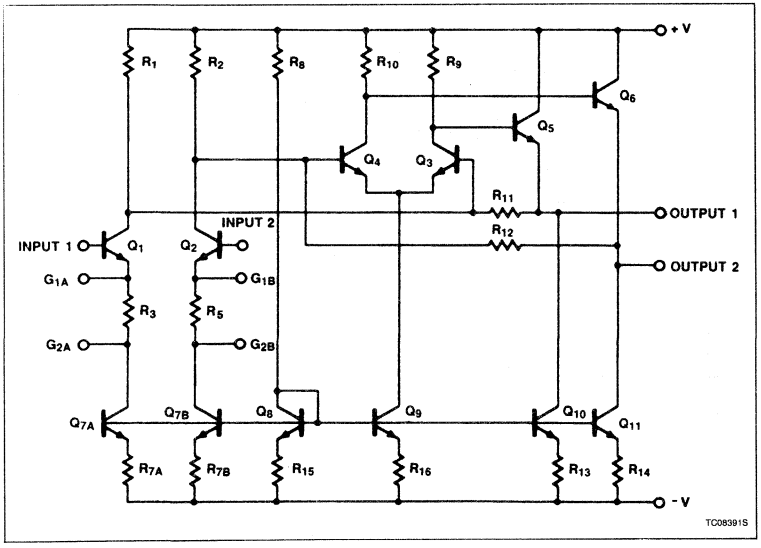
FEATURES

- **120MHz unity gain bandwidth**
- **Adjustable gains from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**
- **MIL-STD processing available**

APPLICATIONS

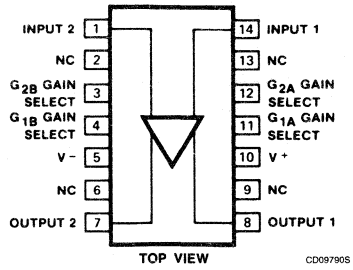
- **Floppy disk head amplifier**
- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memory**
- **Video recorder systems**

EQUIVALENT CIRCUIT

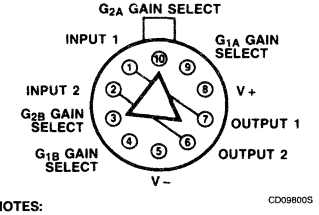


PIN CONFIGURATIONS

D, F, N Packages

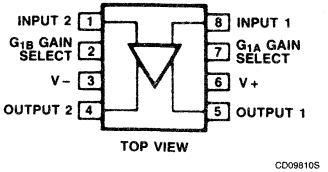


H Package*



NOTES:
Pin 5 connected to case.
*Metal cans (H) not recommended for new designs.

D, F, N, Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE592N14
14-Pin Cerdip	0 to +70°C	NE592F14
14-Pin Cerdip	-55°C to +125°C	SE592F14
14-Pin SO	0 to +70°C	NE592D14
8-Pin Plastic DIP	0 to +70°C	NE592N8
8-Pin Cerdip	-55°C to +125°C	SE592F8
8-Pin Plastic DIP	-40°C to +85°C	SA592N8
8-Pin SO	0 to +70°C	NE592D8
8-Pin SO	-40°C to +85°C	SA592D8
10-Lead Metal Can	0 to +70°C	NE592H
10-Lead Metal Can	-55°C to +125°C	SE592H

NOTE:
N8, N14, D8 and D14 package parts also available in "High" gain version by adding "H" before package designation, i.e., NE592HD8.

ABSOLUTE MAXIMUM RATINGS $T_A = +25°C$, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common-mode input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating ambient temperature range		
	SE592	-40 to +85	°C
	NE592	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
$P_{D\ MAX}$	Maximum power dissipation, $T_A = 25°C$ (still air)[1]		
	F-14 package	1.17	W
	F-8 package	0.79	W
	D-14 package	0.98	W
	D-8 package	0.79	W
	H package	0.83	W
	N-14 package	1.44	W
	N-8 package	1.17	W

NOTE:
1. Derate above 25°C at the following rates:
   F-14 package at 9.3mW/°C
   F-8 package at 6.3mW/°C
   D-14 package at 7.8mW/°C
   D-8 package at 6.3mW/°C
   H package at 6.7mW/°C
   N-14 package at 11.5mW/°C
   N-8 package at 9.3mW/°C

DC ELECTRICAL CHARACTERISTICS

$T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part								
	Gain 1[1]	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	250	400	600	300	400	500	V/V
	Gain 2[2, 4]		80	100	120	90	100	110	V/V
	High gain part		400	500	600				V/V
R_{IN}	Input resistance								
	Gain 1[1]			4.0			4.0		kΩ
	Gain 2[2, 4]		10	30		20	30		kΩ
C_{IN}	Input capacitance[2]	Gain 2[4]		2.0			2.0		pF
I_{OS}	Input offset current			0.4	5.0		0.4	3.0	μA
I_{BIAS}	Input bias current			9.0	30		9.0	20	μA
V_{NOISE}	Input noise voltage	BW 1kHz to 10MHz		12			12		μV_{RMS}
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio								
	Gain 2[4]	$V_{CM} \pm 1V$, $f < 100kHz$	60	86		60	86		dB
	Gain 2[4]	$V_{CM} \pm 1V$, $f = 5MHz$		60			60		dB
PSRR	Supply voltage rejection ratio								
	Gain 2[4]	$\Delta V_S = \pm 0.5V$	50	70		50	70		dB
V_{OS}	Output offset voltage								
	Gain 1	$R_L = \infty$			1.5			1.5	V
	Gain 2[4]	$R_L = \infty$			1.5			1.0	V
	Gain 3[3]	$R_L = \infty$		0.35	0.75		0.35	0.75	V
V_{CM}	Output common-mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OUT}	Output voltage swing differential	$R_L = 2k\Omega$	3.0	4.0		3.0	4.0		V
R_{OUT}	Output resistance			20			20		Ω
I_{CC}	Power supply current	$R_L = \infty$		18	24		18	24	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

DC ELECTRICAL CHARACTERISTICS

$V_{SS} = \pm 6V$, $V_{CM} = 0$, $0°C \leq T_A \leq 70°C$ for NE592; $-40°C \leq T_A \leq 85°C$ for SA592, $-55°C \leq T_A \leq 125°C$ for SE592, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part								
	Gain 1[1]	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	250		600	200		600	V/V
	Gain 2[2, 4]		80		120	80		120	V/V
	High gain part		400	500	600				V/V
R_{IN}	Input resistance								
	Gain 2[2, 4]		8.0			8.0			kΩ
I_{OS}	Input offset current				6.0			5.0	μA
I_{BIAS}	Input bias current				40			40	μA
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio								
	Gain 2[4]	$V_{CM} \pm 1V$, $f < 100kHz$	50			50			dB
PSRR	Supply voltage rejection ratio								
	Gain 2[4]	$\Delta V_S = \pm 0.5V$	50			50			dB
V_{OS}	Output offset voltage								
	Gain 1	$R_L = \infty$			1.5			1.5	V
	Gain 2[4]	$R_L = \infty$			1.5			1.2	V
	Gain 3[3]	$R_L = \infty$			1.0			1.0	V
V_{OUT}	Output voltage swing differential	$R_L = 2k\Omega$	2.8			2.5			V
I_{CC}	Power supply current	$R_L = \infty$			27			27	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

AC ELECTRICAL CHARACTERISTICS

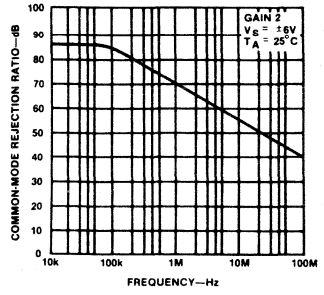
$T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Bandwidth								
	Gain 1[1]			40			40		MHz
	Gain 2[2, 4]			90			90		MHz
t_R	Rise time								
	Gain 1[1]	$V_{OUT} = 1V_{P-P}$		10.5			10.5		ns
	Gain 2[2, 4]			4.5	12		4.5	10	ns
t_{PD}	Propagation delay								
	Gain 1[1]	$V_{OUT} = 1V_{P-P}$		7.5			7.5		ns
	Gain 2[2, 4]			6.0	10		6.0	10	ns

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

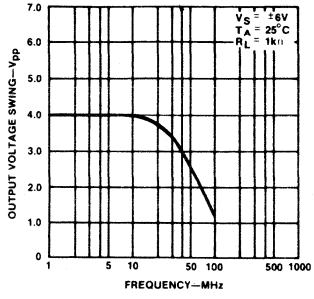
TYPICAL PERFORMANCE CHARACTERISTICS

Common-Mode Rejection Ratio as a Function of Frequency



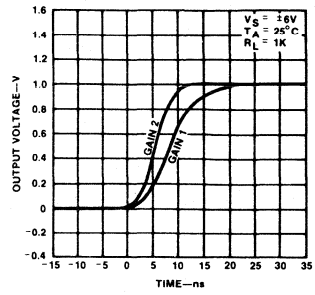
OP04421S

Output Voltage Swing as a Function of Frequency



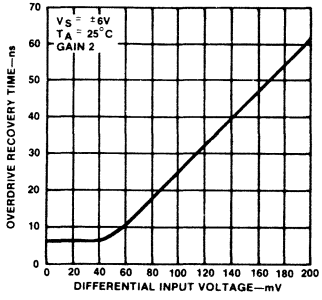
OP04430S

Pulse Response



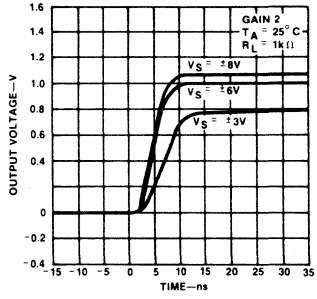
OP04440S

Differential Overdrive Recovery Time



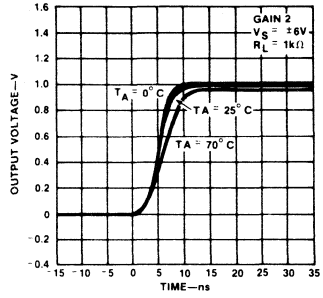
OP04450S

Pulse Response as a Function of Supply Voltage



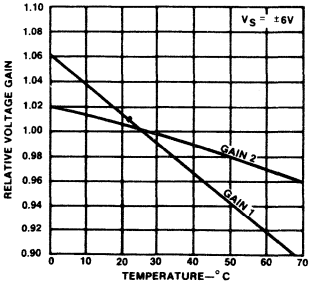
OP04460S

Pulse Response as a Function of Temperature



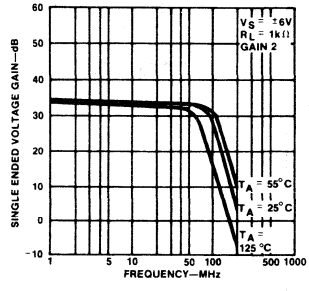
OP04470S

Voltage Gain as a Function of Temperature



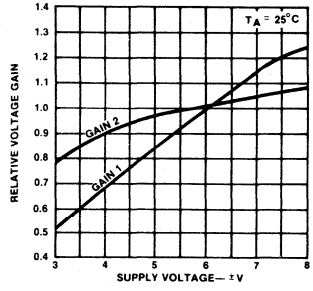
OP04480S

Gain vs Frequency as a Function of Temperature



OP04490S

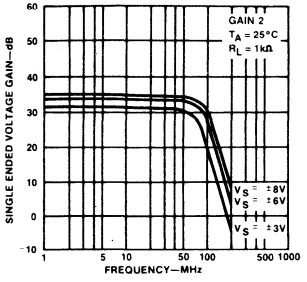
Voltage Gain as a Function of Supply Voltage



OP04500S

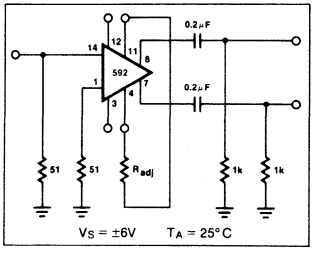
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Gain vs Frequency as a Function of Supply Voltage



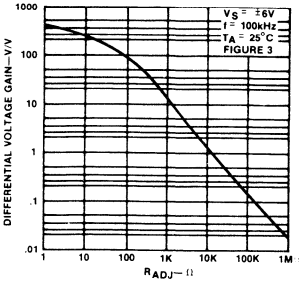
OP04510S

Voltage Gain Adjust Circuit



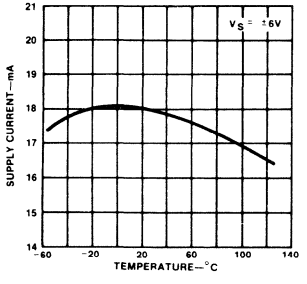
OP04521S

Voltage Gain as a Function of RADJ (Figure 3)



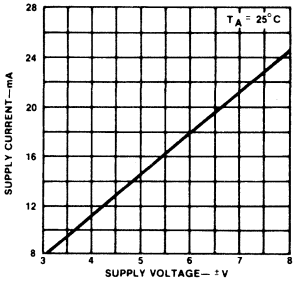
OP04530S

Supply Current as a Function of Temperature



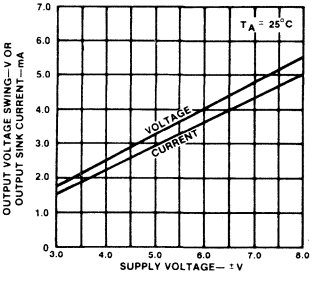
OP04540S

Supply Current as a Function of Supply Voltage



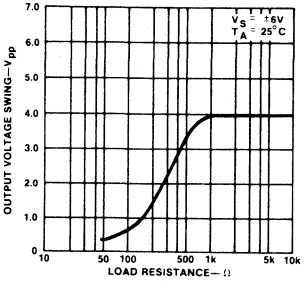
OP04550S

Output Voltage and Current Swing as a Function of Supply Voltage



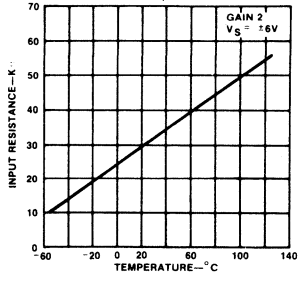
OP04560S

Output Voltage Swing as a Function of Load Resistance



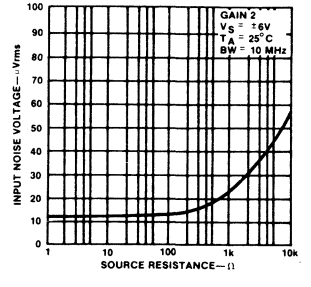
OP04570S

Input Resistance as a Function of Temperature



OP04580S

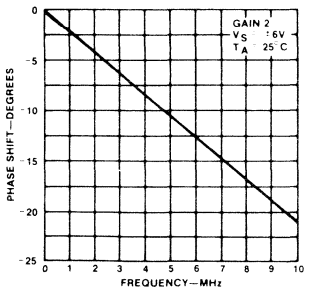
Input Noise Voltage as a Function of Source Resistance



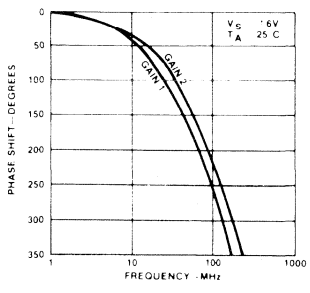
OP04590S

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

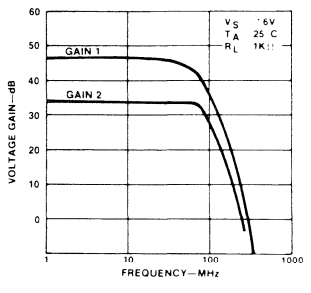
Phase Shift as a Function of Frequency



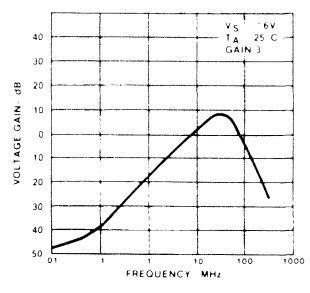
Phase Shift as a Function of Frequency



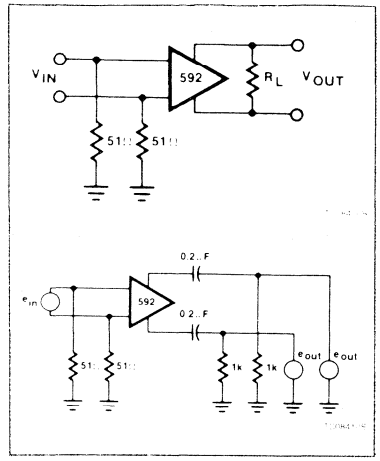
Voltage Gain as a Function of Frequency



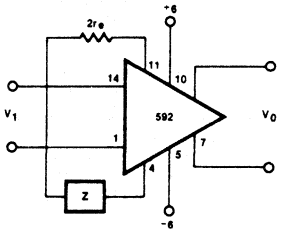
Voltage Gain as a Function of Frequency (All Gain Select Pins Open)



TEST CIRCUITS $T_A = 25°C$, unless otherwise specified.



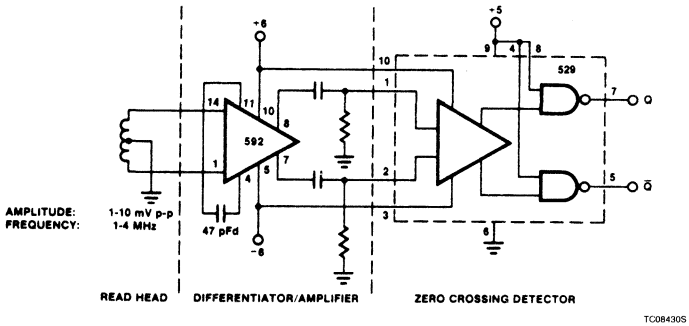
TYPICAL APPLICATIONS



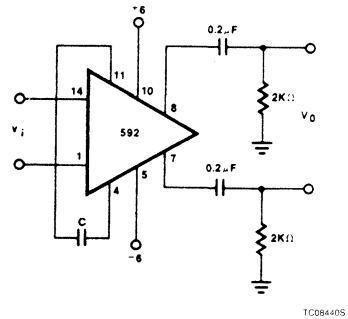
NOTE:

$$\frac{V_0(s)}{V_1(s)} \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e} \cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

Basic Configuration



Disc/Tape Phase-Modulated Readback Systems

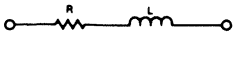
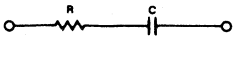
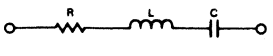
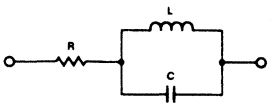


NOTE:
For frequency $F_1 << 1/2\pi(32)C$

$$V_0 \cong 1.4 \times 10^4 C \frac{dVi}{dT}$$

Differentiation with High Common-Mode Noise Rejection

FILTER NETWORKS

Z NETWORK	FILTER TYPE	V_0 (s) TRANSFER V_1 (s) FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\, s + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

TC08422S

NOTES:
In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω.
$S = j\omega$
$\omega = 2\pi f$

Wide-band high-frequency amplifier — NE/SA5204A

DESCRIPTION

The NE/SA5204A family of wideband amplifiers replaces the NE/SA5204 family. The 'A' parts are fabricated on a rugged 2μm bipolar process featuring excellent statistical process control. Electrical performance is nomically identical to the original parts.

The NE/SA5204A is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 200MHz. The -3dB bandwidth is greater than 350MHz. This performance makes the amplifier ideal for cable TV applications. The NE/SA5204A operates with a single supply of 6V, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

The NE/SA5204A is a relaxed version of the NE5205. Minimum guaranteed bandwidth is relaxed to 350MHz and the "S" parameter Min/Max limits are specified as typicals only.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA5204A solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The standing wave ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output over the entire DC to 350MHz operating range.

Since the part is a small, monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

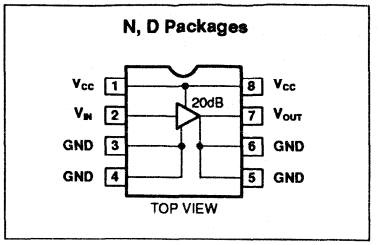
No external components are needed other than AC-coupling capacitors because the NE/SA5204A is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm, respectively, at 100MHz.

The part is well matched for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters, and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio, and data/video transmission in fiber optics, as well as broadband LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA5204As in series as required, without any degradation in amplifier stability.

FEATURES

- Bandwidth (min.)
  200 MHz, ±0.5dB
  350 MHz, -3dB
- 20dB insertion gain
- 4.8dB (6dB) noise figure ZO=75Ω (ZO=50Ω)
- No external components required
- Input and output impedances matched to 50/75Ω systems
- Surface-mount package available
- Cascadable
- 2000V ESD protection

PIN CONFIGURATION



APPLICATIONS

- Antenna amplifiers
- Amplified splitters
- Signal generators
- Frequency counters
- Oscilloscopes
- Signal analyzers
- Broadband LANs
- Networks
- Modems
- Mobile radio
- Security systems
- Telecommunications

ORDERING INFORMATION

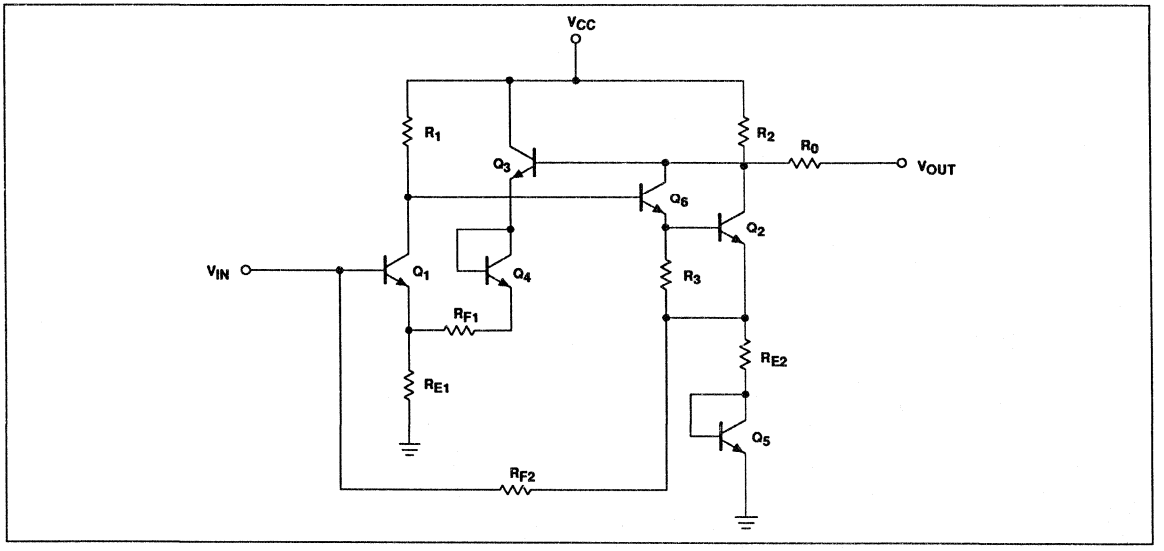
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C –40 to +85°C	NE5204AN SA5204AN
8-Pin Plastic SO package	0 to +70°C –40 to +85°C	NE5204AD SA5204AD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{IN}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range		
	NE grade	0 to +70	°C
	SA grade	–40 to +85	°C
P_{DMAX}	Maximum power dissipation[1, 2] T_A=25°C(still–air)		
	N package	1160	mW
	D package	780	mW
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	–55 to +150	°C
T_{SOLD}	Lead temperature (soldering 60s)	300	°C

NOTES:
1. Derate above 25°C, at the following rates
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. See "Power Dissipation Considerations" section.

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS

V_{CC}=6V, Z_S=Z_L=Z_O=50Ω and T_A=25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage range	Over temperature	5		8	V
I_{CC}	Supply current	Over temperature	19	25	33	mA
S21	Insertion gain	f=100MHz, over temperature	16	19	22	dB
S11	Input return loss	f=100MHz		25		dB
		DC –550MHz		12		dB
S22	Output return loss	f=100MHz		27		dB
		DC –550MHz		12		dB
S12	Isolation	f=100MHz		–25		dB
		DC –550MHz		–18		dB
BW	Bandwidth	±0.5dB	200	350		MHz
BW	Bandwidth	–3dB	350	550		MHz
	Noise figure (75Ω)	f=100MHz		4.8		dB
	Noise figure (50Ω)	f=100MHz		6.0		dB
	Saturated output power	f=100MHz		+7.0		dBm
	1dB gain compression	f=100MHz		+4.0		dBm
	Third–order intermodulation intercept (output)	f=100MHz		+17		dBm
	Second–order intermodulation intercept (output)	f=100MHz		+24		dBm
t_R	Rise time			500		ps
t_P	Propagation delay			500		ps

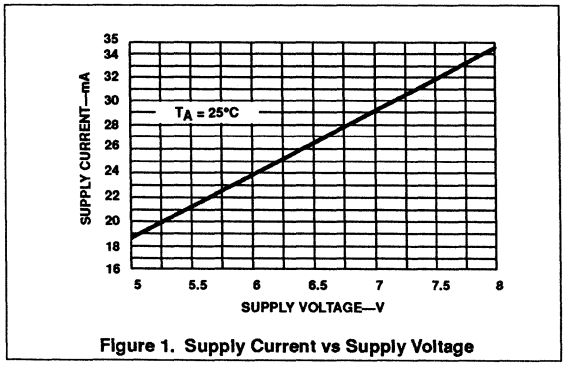


Figure 1. Supply Current vs Supply Voltage

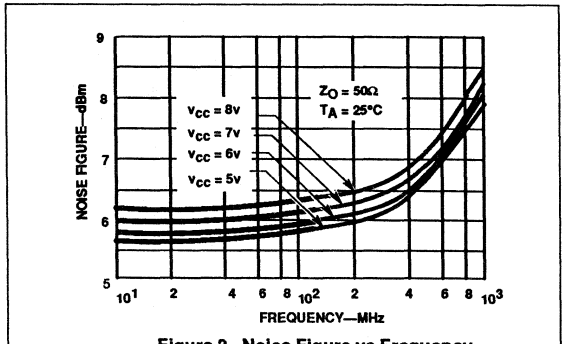


Figure 2. Noise Figure vs Frequency

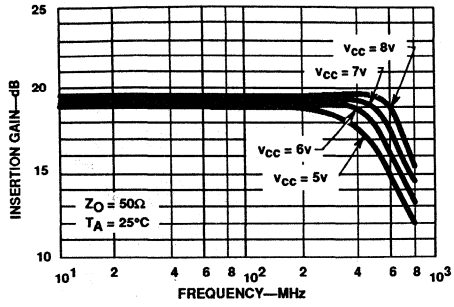


Figure 3. Insertion Gain vs Frequency (S_{21})

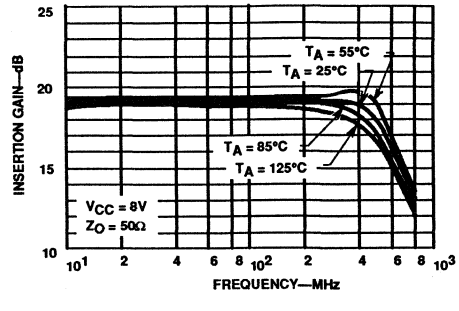


Figure 4. Insertion Gain vs Frequency (S_{21})

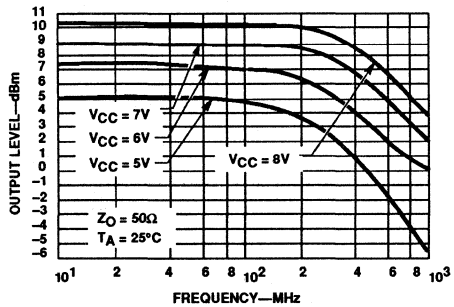


Figure 5. Saturated Output Power vs Frequency

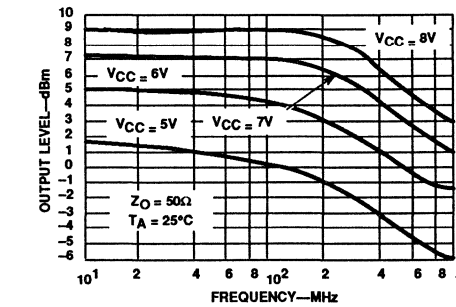


Figure 6. 1dB Gain Compression vs Frequency

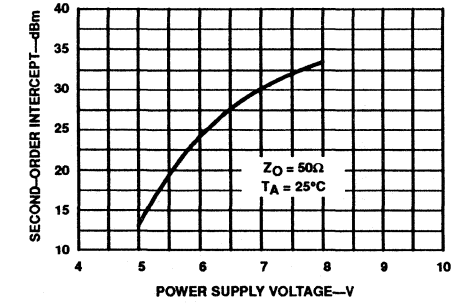


Figure 7. Second-Order Output Intercept vs Supply Voltage

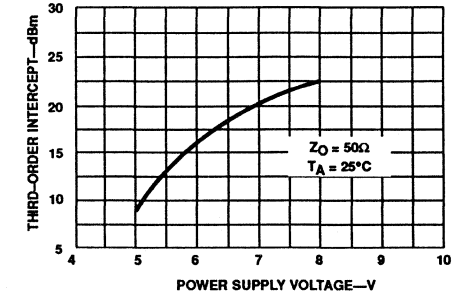


Figure 8. Third-Order Intercept vs Supply Voltage

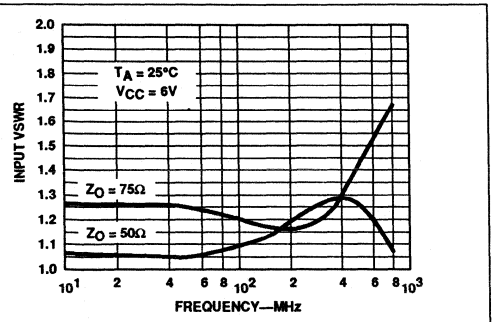


Figure 9. Input VSWR vs Frequency

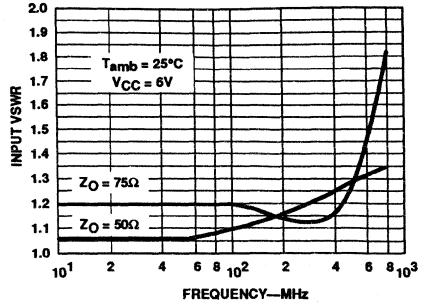


Figure 10. Output VSWR vs Frequency

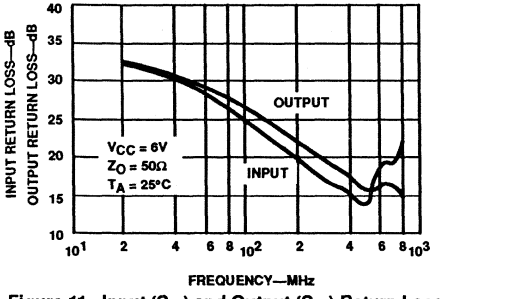


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

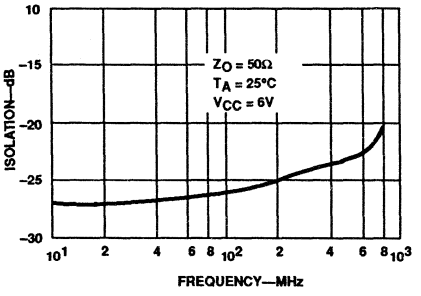


Figure 12. Isolation vs Frequency (S_{12})

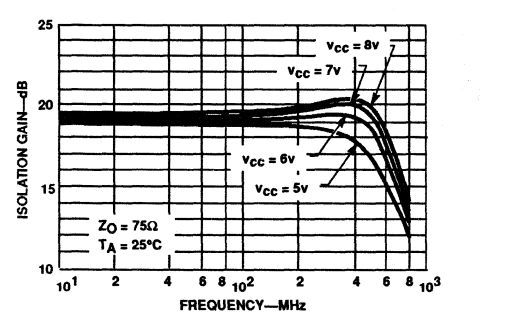


Figure 13. Insertion Gain vs Frequency (S_{21})

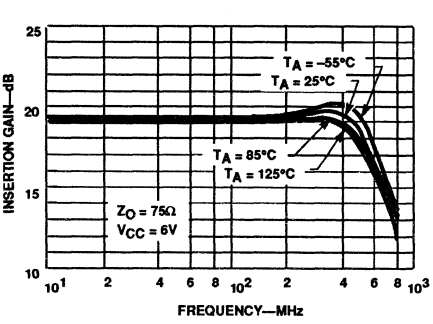


Figure 14. Insertion Gain vs Frequency (S_{21})

Wide-band high-frequency amplifier | NE/SA5204A

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1}) \;/\; R_{E1} \qquad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wide-band terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible, while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10Log\left\{1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2qI_{C1}}\right]}{R_O}\right\} dB \quad (2)$$

where I_{C1}=5.5mA, R_{E1}=12Ω, r_b=130Ω, KT/q=26mV at 25°C and R_0=50 for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN}=V_{BE1}+(I_{C1}+I_{C3})\,R_{E1} \quad (3)$$

where R_{E1}=12Ω, V_{BE}=0.8V, I_{C1}=5mA and I_{C3}=7mA (currents rated at V_{CC}=6V).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4, which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt-feedback loading on the output. The value of R_{F1}=140Ω is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT}=V_{CC}-(I_{C2}+I_{C6})R2, \quad (4)$$

where V_{CC}=6V, R_2=225Ω, I_{C2}=8mA and I_{C6}=5mA.

From here, it can be seen that the output voltage is approximately 3.1V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (32mA max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat-sinking benefits can be realized by mounting the SO and N package bodies against the PC board plane.

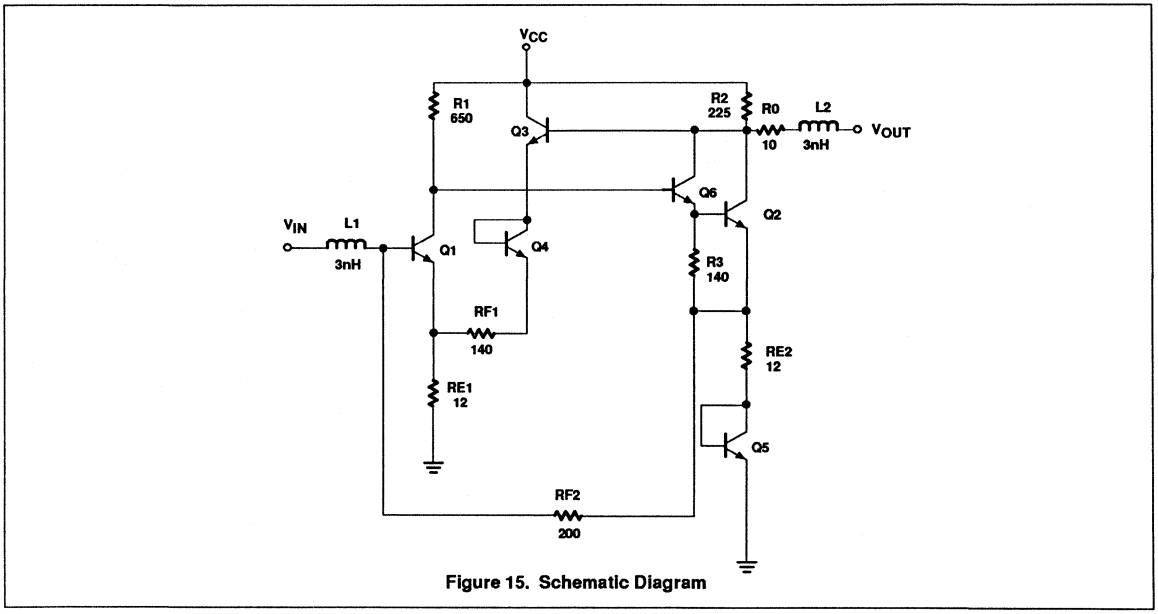


Figure 15. Schematic Diagram

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5204A to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the package). The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible, and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC-coupled. This is because at V_{CC}=6V, the input is approximately at 1V while the output is at 3.1V. The output must be decoupled into a low-impedance system, or the DC bias on the output of the amplifier will be loaded down, causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high-frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

SCATTERING PARAMETERS

The primary specifications for the NE5204A are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source,

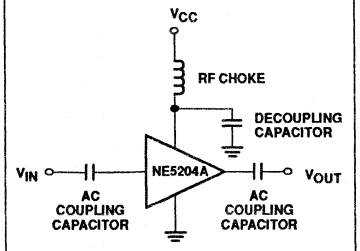


Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling

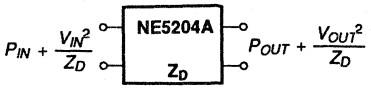
amplifier, and load as well as transmission losses. The parameters for a two-port network are defined in Figure 17.

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 18.

Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5204A to other high-frequency amplifiers.

The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

Z_D=Z_{IN}=Z_{OUT} for the NE/SA/SE5204A



$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

P_I=V_I ^{2}

P_I=Insertion Power Gain

V_I=Insertion Voltage Gain

Measured value for the NE/SA/SE5204A = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

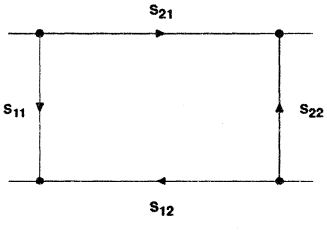
$P_{I(dB)}$ =10 Log $|S_{21}|^2$ = 20dB

$V_{I(dB)}$ = 20 Log S_{21} = 20dB

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)}$ = 20dB

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 19. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:



a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} = \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OSOLATION

$$S_{12} = \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

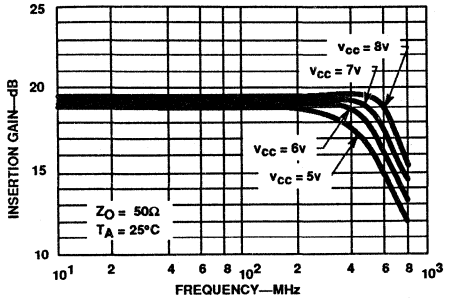
$$S_{21} = \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

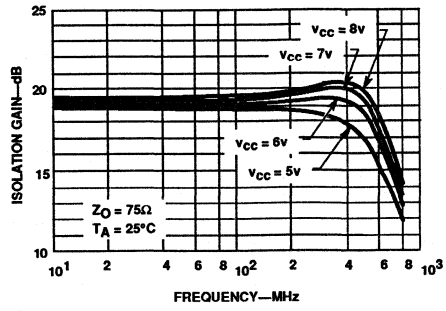
$$S_{22} = \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

b.

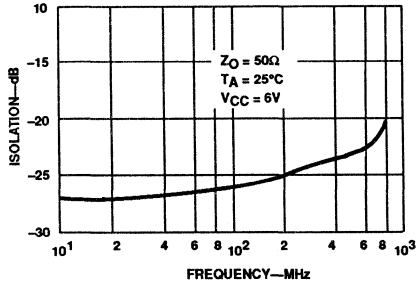
Figure 17.



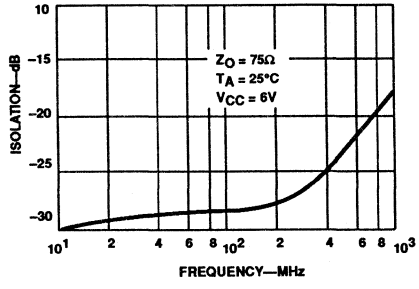
a. Insertion Gain vs Frequency (S_{21})



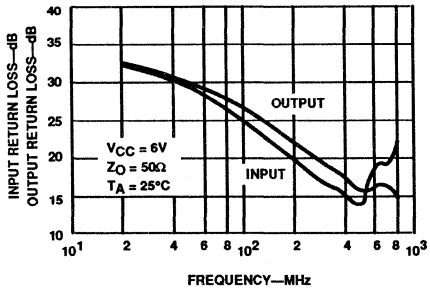
b. Insertion Gain vs Frequency (S_{21})



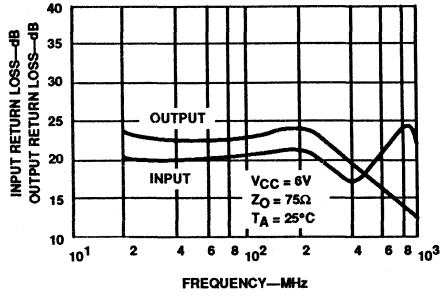
c. Isolation vs Frequency (S_{12})



d. S_{12} Isolation vs Frequency



e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency



f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 18.

INPUT RETURN LOSS=S_{11}dB
S_{11}dB=20 Log | S_{11} |

OUTPUT RETURN LOSS=S_{22}dB
S_{22}dB=20 Log | S_{22} |

INPUT VSWR=≤1.5

OUTPUT VSWR=≤1.5

1DB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily

overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 20, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

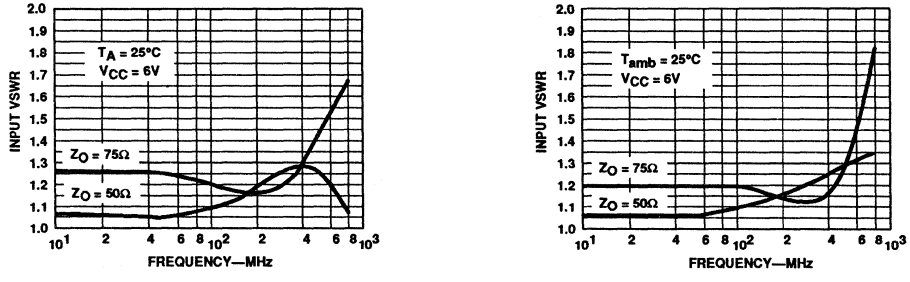
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

$$IP_2 = P_{OUT} + IMR_2$$

$$IP_3 = P_{OUT} + IMR_3/2$$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA5204A we have chosen an output level of –10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.



a. Input VSWR vs Frequency **b. Output VSWR vs Frequency**

Figure 19. Input/Output VSWR vs Frequency

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to High-Frequency Amplifiers by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.

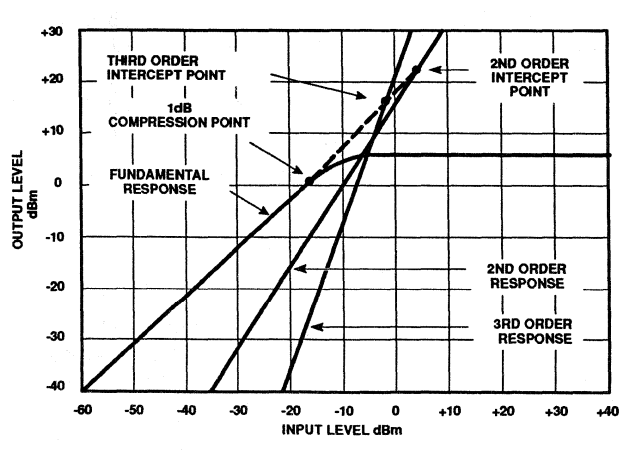


Figure 20.

Wide-band high-frequency amplifier — NE/SA/SE5205A

DESCRIPTION

The NE/SA/SE5205A family of wideband amplifiers replace the NE/SA/SE5205 family. The 'A' parts are fabricated on a rugged 2µm bipolar process featuring excellent statistical process control. Electrical performance is nominally identical to the original parts.

The NE/SA/SE5205A is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 450MHz, and the -3dB bandwidth is greater than 600MHz in the EC package. This performance makes the amplifier ideal for cable TV applications. For lower frequency applications, the part is also available in industrial standard dual in-line and small outline packages. The NE/SA/SE5205A operates with a single supply of 6V, and only draws 24mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high-power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA/SE5205A solves these problems by incorporating a wide-band amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The Standing Wave Ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output from DC to the -3dB bandwidth limit.

Since the part is a small monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

No external components are needed other than AC coupling capacitors because the NE/SA/SE5205A is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz.

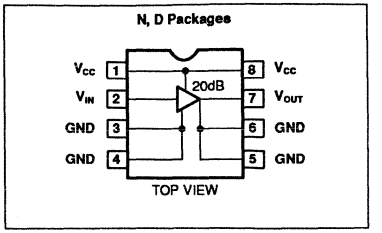
The device is ideally suited for 75Ω cable television applications such as decoder boxes, satellite receiver/decoders, and front-end amplifiers for TV receivers. It is also useful for amplified splitters and antenna amplifiers.

The part is matched well for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio and data/video transmission in fiber optics, as well as broad-band LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA/SE5205As in series as required, without any degradation in amplifier stability.

FEATURES

- 600MHz bandwidth
- 20dB insertion gain
- 4.8dB (6dB) noise figure ZO=75Ω (ZO=50Ω)
- No external components required
- Input and output impedances matched to 50/75Ω systems
- Surface mount package available
- MIL-STD processing available
- 2000V ESD protection

PIN CONFIGURATIONS



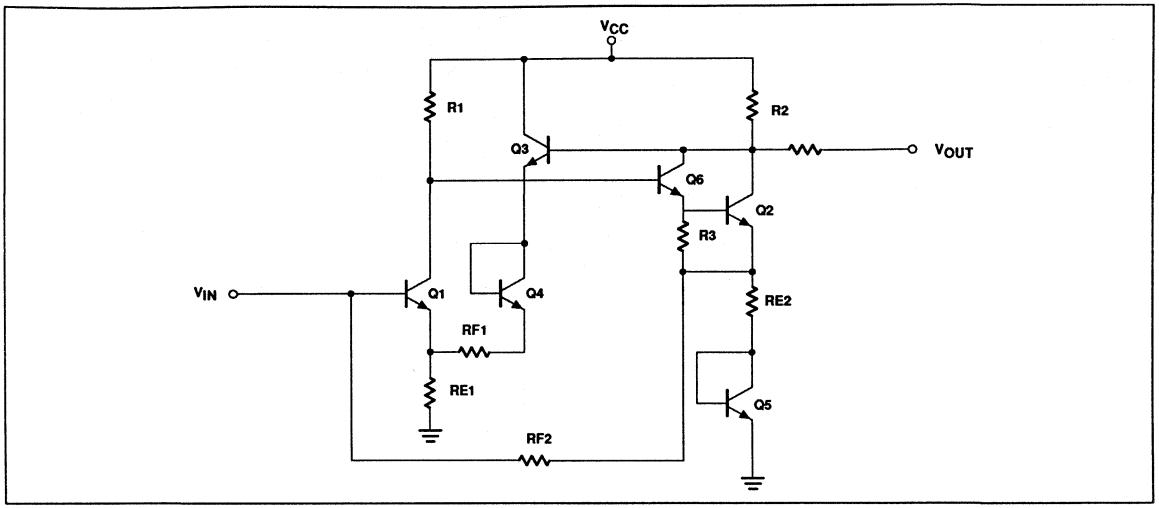
APPLICATIONS

- 75Ω cable TV decoder boxes
- Antenna amplifiers
- Amplified splitters
- Signal generators
- Frequency counters
- Oscilloscopes
- Signal analyzers
- Broad-band LANs
- Fiber-optics
- Modems
- Mobile radio
- Security systems
- Telecommunications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE5205AD
8-Pin Plastic DIP	0 to +70°C	NE5205AN
8-Pin Plastic SO	-40 to +85°C	SA5205AD
8-Pin Plastic DIP	-40 to +85°C	SA5205AN
8-Pin Plastic DIP	-55 to +125°C	SE5205AN

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{AC}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range		
	NE grade	0 to +70	°C
	SA grade	-40 to +85	°C
	SE grade	-55 to +125	°C
P_{DMAX}	Maximum power dissipation, T_A=25°C (still-air)[1, 2]		
	N package	1160	mW
	D package	780	mW

NOTES:
1. Derate above 25°C, at the following rates:
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. See "Power Dissipation Considerations" section.

DC ELECTRICAL CHARACTERISTICS

V_{CC}=6V, Z_S=Z_L=Z_O=50Ω and T_A=25°C in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5205A			NE/SA5205A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Operating supply voltage range		5		6.5	5		8	V
		Over temperature	5		6.5	5		8	V
I_{CC}	Supply current		20	25	32	20	25	32	mA
		Over temperature	19	25	33	19	25	33	mA
S21	Insertion gain	f=100MHz	17	19	21	17	19	21	dB
		Over temperature	16.5		21.5	16.5		21.5	
S11	Input return loss	f=100MHz D, N		25			25		dB
		DC - f_{MAX} D, N	12			12			dB
S22	Output return loss	f=100MHz D, N		27			27		dB
		DC - f_{MAX}	12			12			dB
S12	Isolation	f=100MHz		-25			-25		dB
		DC - f_{MAX}	-18			-18			dB
t_R	Rise time			500			500		ps
t_P	Propagation delay			500			500		ps
BW	Bandwidth	±0.5dB D, N		300			450		MHz
f_{MAX}	Bandwidth	-3dB D, N				550			MHz
	Noise figure (75Ω)	f=100MHz		4.8			4.8		dB
	Noise figure (50Ω)	f=100MHz		6.0			6.0		dB
	Saturated output power	f=100MHz		+7.0			+7.0		dBm
	1dB gain compression	f=100MHz		+4.0			+4.0		dBm
	Third-order intermodulation intercept (output)	f=100MHz		+17			+17		dBm
	Second-order intermodulation intercept (output)	f=100MHz		+24			+24		dBm

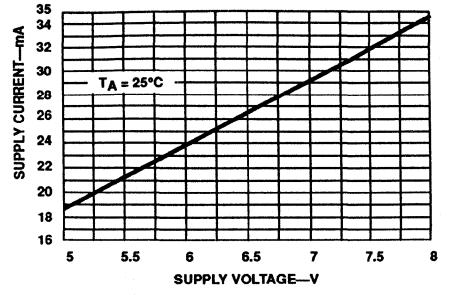


Figure 1. Supply Current vs Supply Voltage

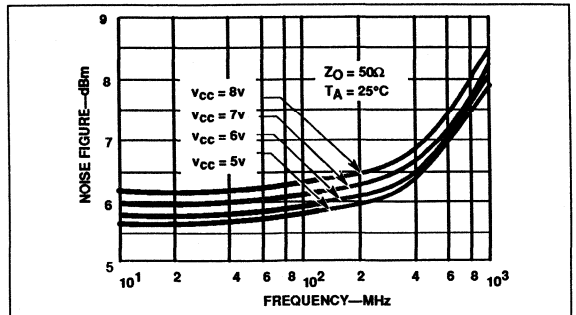


Figure 2. Noise Figure vs Frequency

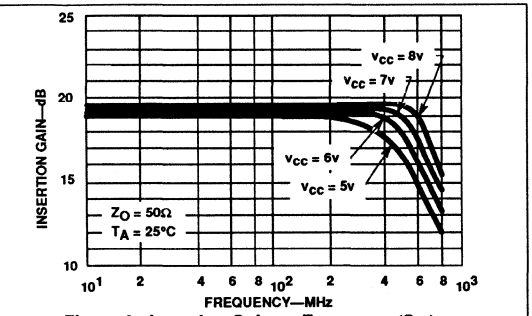


Figure 3. Insertion Gain vs Frequency (S_{21})

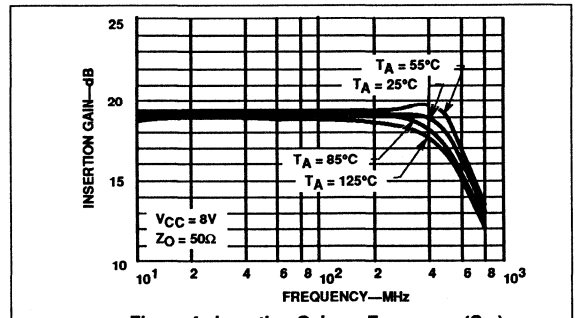


Figure 4. Insertion Gain vs Frequency (S_{21})

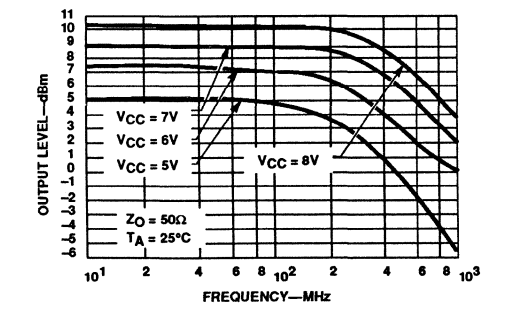


Figure 5. Saturated Output Power vs Frequency

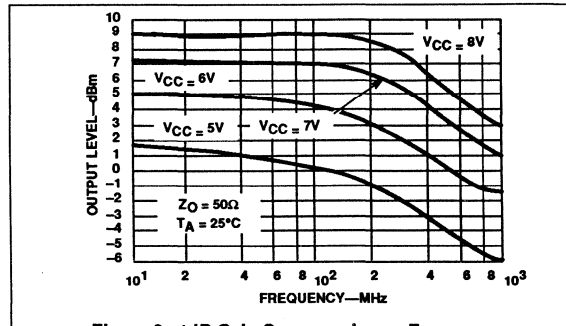


Figure 6. 1dB Gain Compression vs Frequency

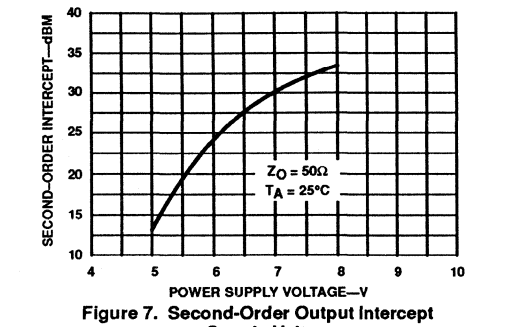


Figure 7. Second-Order Output Intercept vs Supply Voltage

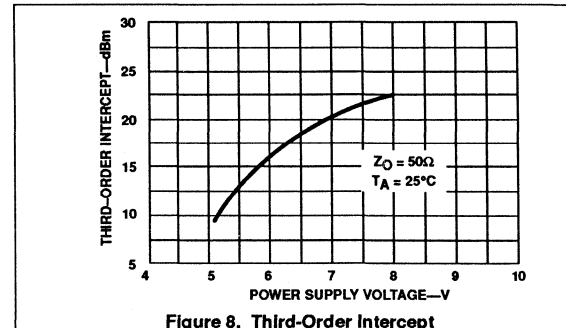


Figure 8. Third-Order Intercept vs Supply Voltage

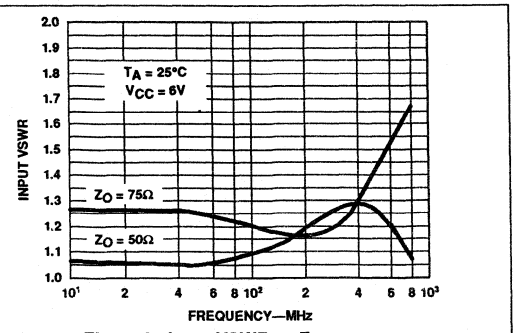


Figure 9. Input VSWR vs Frequency

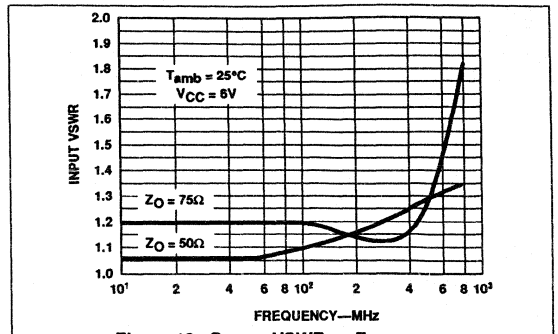


Figure 10. Output VSWR vs Frequency

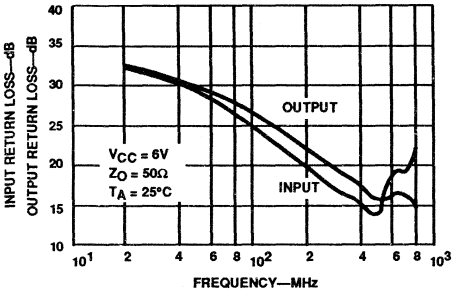


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

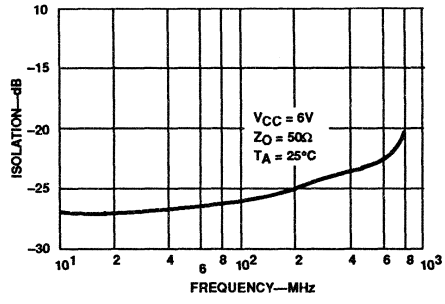


Figure 12. Isolation vs Frequency (S_{12})

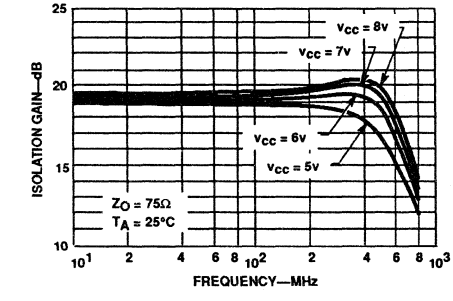


Figure 13. Insertion Gain vs Frequency (S_{21})

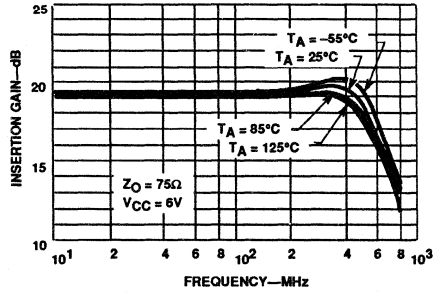


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = \frac{(R_{F1} + R_{E1})}{R_{E1}} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wideband terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10\log\left[1 + \left[\frac{r_b + R_{E1} + \frac{KT}{2qI_{C1}}}{R_O}\right]\right] dB \quad (2)$$

where I_{C1}=5.5mA, R_{E1}=12Ω, r_b=130Ω, KT/q=26mV at 25°C and R_0=50 for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN}=V_{BE1}+(I_{C1}+I_{C3})\ R_{E1}$$

where R_{E1}=12Ω, V_{BE}=0.8V, I_{C1}=5mA and I_{C3}=7mA (currents rated at V_{CC}=6V).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4 which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt feedback loading on the output. The value of R_{F1}=140Ω is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT}=V_{CC}-(I_{C2}+I_{C6})R2,(4)$$

where V_{CC}=6V, R_2=225Ω, I_{C2}=8mA and I_{C6}=5mA.

From here it can be seen that the output voltage is approximately 3.1V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

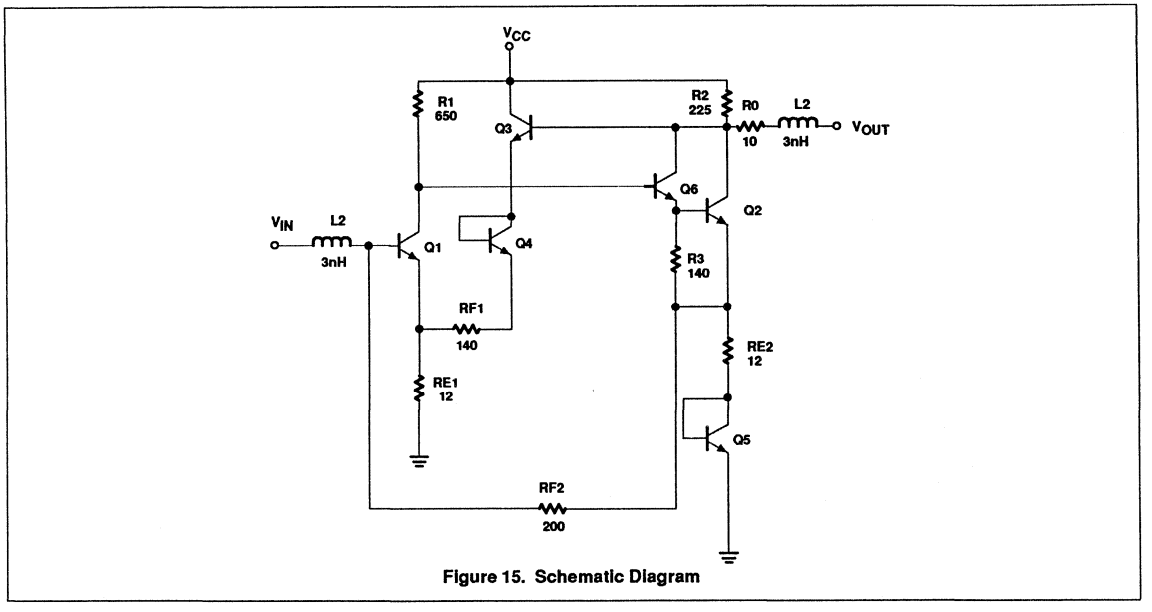


Figure 15. Schematic Diagram

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (32mA Max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat sinking benefits can be realized by mounting the D package body against the PC board plane.

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5205A to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the SO package). The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and

output should be AC coupled. This is because at V_{CC}=6V, the input is approximately at 1V while the output is at 3.1V. The output must be decoupled into a low impedance system or the DC bias on the output of the amplifier will be loaded down causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

SCATTERING PARAMETERS

The primary specifications for the NE/SA/SE5205A are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier and load as well as transmission losses. The parameters for a two-port network are defined in Figure 17.

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 18.

Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5205A to other high-frequency amplifiers.

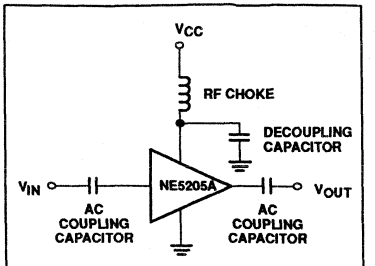


Figure 1. Circuit Schematic for Coupling and Power Supply Decoupling

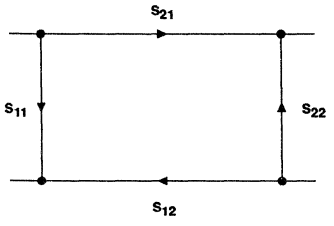


Figure 17a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} = \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OSOLATION

$$S_{12} = \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

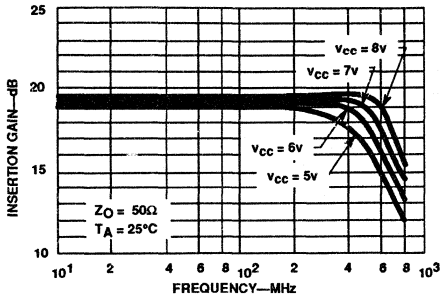
$$S_{21} = \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

$$S_{22} = \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

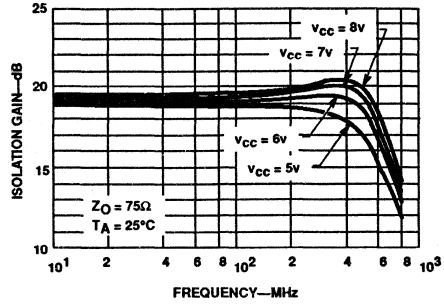
Figure 17b.

50Ω System

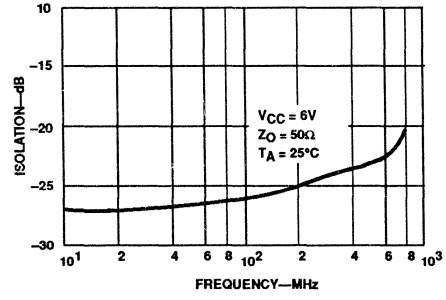


a. Insertion Gain vs Frequency (S_{21})

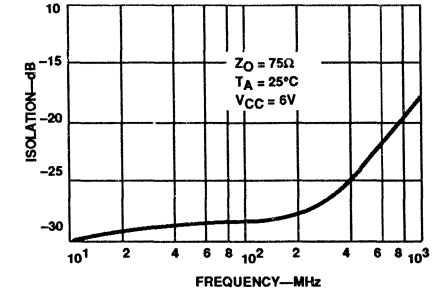
75Ω System



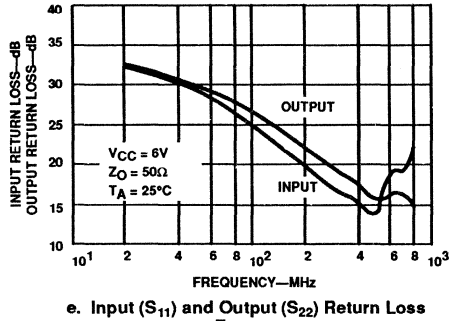
b. Insertion Gain vs Frequency (S_{21})



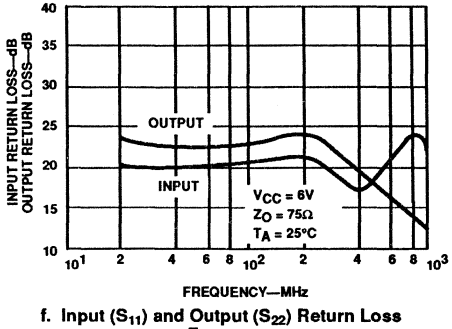
c. Isolation vs Frequency (S_{12})



d. S_{12} Isolation vs Frequency



e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

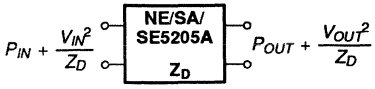


f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 18.

The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D=Z_{IN}=Z_{OUT}$ for the NE/SA/SE5205A



$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$P_I=V_I{}^2$

P_I=Insertion Power Gain

V_I=Insertion Voltage Gain

Measured value for the
NE/SA/SE5205A = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:
$P_{I(dB)}$ =10 Log $|S_{21}|^2$ = 20dB
$V_{I(dB)}$ = 20 Log S_{21} = 20dB
$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)}$ = 20dB

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 19. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS=S_{11}dB
S_{11}dB=20 Log $|S_{11}|$
OUTPUT RETURN LOSS=S_{22}dB
S_{22}dB=20 Log $|S_{22}|$
INPUT VSWR=≤1.5
OUTPUT VSWR=≤1.5

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 20, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

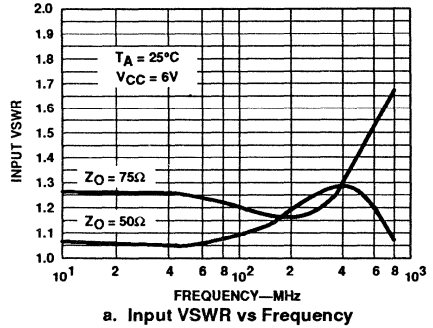
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

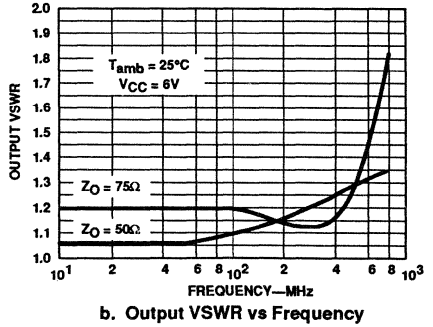
$IP_2=P_{OUT}+IMR_2$

$IP_3=P_{OUT}+IMR_3/2$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA/SE5205A we have chosen an output level of -10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.



a. Input VSWR vs Frequency



b. Output VSWR vs Frequency

Figure 19. Input/Output VSWR vs Frequency

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to High-Frequency Amplifiers by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.

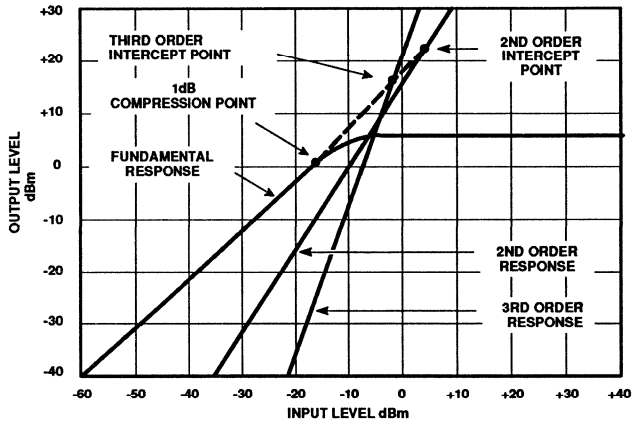


Figure 20.

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Date of Issue	August 20, 1990
Status	Product Specification
RF Communications	

NE/SA5209

Wideband variable gain amplifier

DESCRIPTION

The NE5209 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

The NE5209 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1kΩ) differential inputs. The output is 50Ω differential. Therefore, the 5209 can simultaneously perform AGC, impedance transformation, and the balun functions.

The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

FEATURES

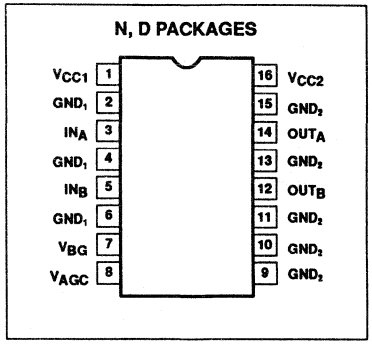
- Gain to 1.5GHz
- 850MHz bandwidth
- High impedance differential input
- 50Ω differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional $V_{CONTROL}$ / V_{GAIN} linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi-purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

PIN CONFIGURATION

N, D PACKAGES



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE5209D
16-Pin Plastic DIP	0 to +70°C	NE5209N
16-Pin Plastic SO	–40 to +85°C	SA5209D
16-Pin Plastic DIP	–40 to +85°C	SA5209N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	–0.5 to +8.0	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 16-Pin Plastic DIP 16-Pin Plastic SO	 1450 1100	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
T_{STG}	Storage temperature range	–65 to +150	°C

NOTES:
3.Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
16-Pin DIP: θ_{JA} = 85°C/W
16-Pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	V_{CC1} = V_{CC2} = 4.5 to 7.0V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 –40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 –40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC1} = V_{CC2} = +5V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{CC}	Supply current	DC tested	38	43	48	mA
		Over temperature[1]	30		55	mA
A_V	Voltage gain (single-ended in/single-ended out)	DC tested, R_L = 10kΩ	17	19	21	dB
		Over temperature[1]	16		22	dB
A_V	Voltage gain (single-ended in/differential out)	DC tested, R_L = 10kΩ	23	25	27	dB
		Over temperature[1]	22		28	dB
R_{IN}	Input resistance (single-ended)	DC tested at ±50µA	0.9	1.2	1.5	kΩ
		Over temperature[1]	0.8		1.7	kΩ
R_{OUT}	Output resistance (single-ended)	DC tested at ±1mA	40	60	75	Ω
		Over temperature[1]	35		90	Ω
V_{OS}	Output offset voltage (output referred)			±20	±100	mV
		Over temperature[1]			±250	mV
V_{IN}	DC level on inputs		1.6	2.0	2.4	V
		Over temperature[1]	1.4		2.6	V
V_{OUT}	DC level on outputs		1.9	2.4	2.9	V
		Over temperature[1]	1.7		3.1	V
PSRR	Output offset supply rejection ratio		20	45		dB
	(output referred)	Over temperature[1]	15			dB
V_{BG}	Bandgap reference voltage	4.5V<V_{CC}<7V R_{BG} = 10kΩ	1.2	1.32	1.45	V
		Over temperature[1]	1.1		1.55	V

Wideband variable gain amplifier | NE/SA5209

DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC1} = V_{CC2} = +5.0V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
R_{BG}	Bandgap loading	Over temperature[1]	2	10		kΩ
V_{AGC}	AGC DC control voltage range	Over temperature[1]		0-1.3		V
I_{BAGC}	AGC pin DC bias current	0V<V_{AGC}<1.3V		–0.7	–6	µA
		Over temperature[1]			–10	µA

NOTES:
1."Over Temperature Range" testing is as follows:
NE is 0 to +70°C
SA is –40 to +85°C
At the time of this data sheet release, the D package over-temperature data sheet limits are guaranteed via guardbanded room temperature testing only.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC1} = V_{CC2} = +5.0V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
BW	–3dB bandwidth		600	850		MHz
		Over temperature[1]	500			MHz
GF	Gain flatness	DC – 500MHz		±0.4		dB
		Over temperature[1]		±0.6		dB
V_{IMAX}	Maximum input voltage swing (single-ended) for linear operation[2]			200		mV_{P-P}
V_{OMAX}	Maximum output voltage swing (single-ended)	R_L = 50Ω		400		mV_{P-P}
	for linear operation[2]	R_L = 1kΩ		1.9		V_{P-P}
NF	Noise figure (unmatched configuration)	R_S = 50Ω, f = 50MHz		9.3		dB
V_{IN-EQ}	Equivalent input noise voltage spectral density	f = 100MHz		2.5		nV/√Hz
S12	Reverse isolation	f = 100MHz		–60		dB
$\Delta G/\Delta V_{CC}$	Gain supply sensitivity (single-ended)			0.3		dB/V
$\Delta G/\Delta T$	Gain temperature sensitivity	R_L = 50Ω		0.013		dB/°C
C_{IN}	Input capacitance (single-ended)			2		pF
BW_{AGC}	–3dB bandwidth of gain control function			20		MHz
P_{O-1dB}	1dB gain compression point at output	f = 100MHz		–3		dBm
P_{I-1dB}	1dB gain compression point at input	f = 100MHz, V_{AGC} =0.1V		–10		dBm
$IP3_{OUT}$	Third-order intercept point at output	f = 100MHz, V_{AGC} >0.5V		+13		dBm
$IP3_{IN}$	Third-order intercept point at input	f = 100MHz, V_{AGC} <0.5V		+5		dBm
ΔG_{AB}	Gain match output A to output B	f = 100MHz, V_{AGC} = 1V		0.1		dB

NOTE:
1."Over Temperature Range" testing is as follows:
NE is 0 to +70°C
SA is –40 to +85°C
At the time of this data sheet release, the D package over-temperature data sheet limits are guaranteed via guardbanded room temperature testing only.
2.With R_L > 1kΩ, overload occurs at input for single-ended gain < 13dB and at output for single-ended gain > 13dB. With R_L = 50Ω, overload occurs at input for single-ended gain < 6dB and at output for single-ended gain > 6dB.

Wideband variable gain amplifier NE/SA5209

NE5209 APPLICATIONS

The NE5209 is a wideband variable gain amplifier (VGA) circuit which finds many applications in the RF, IF and video signal processing areas. This application note describes the operation of the circuit and several applications of the VGA. The simplified equivalent schematic of the VGA is shown in Figure 1. Transistors Q1-Q6 form the wideband Gilbert multiplier input stage which is biased by current source I1. The top differential pairs are biased from a buffered and level-shifted signal derived from the V_{AGC} input and the RF input appears at the lower differential pair. The circuit topology and layout offer low input noise and wide bandwidth. The second stage is a differential transimpedance stage with current feedback which maintains the wide bandwidth of the input stage. The output stage is a pair of emitter followers with 50Ω output impedance. There is also an on-chip bandgap reference with buffered output at 1.3V, which can be used to derive the gain control voltage.

Both the inputs and outputs should be capacitor coupled or DC isolated from the signal sources and loads. Furthermore, the two inputs should be DC isolated from each other and the two outputs should likewise be DC isolated from each other. The NE5209 was designed to provide optimum performance from a 5V power source. However, there is some range around this value (4.5 – 7V) that can be used.

The input impedance is about 1kΩ. The main advantage to a differential input configuration is to provide the balun function. Otherwise, there is an advantage to common mode rejection, a specification that is not normally important to RF designs. The source impedance can be chosen for two different performance characteristics: Gain, or noise performance. Gain optimization will be realized if the input impedance is matched to about 1kΩ. A 4:1 balun will provide such a broadband match from a 50Ω source. Noise performance will be optimized if the input impedance is matched to about 200Ω. A 2:1 balun will provide such a broadband match from a 50Ω source. The minimum noise figure can then be expected to be about 7dB. Maximum gain will be about 23dB for a single-ended output. If the differential output is used and properly matched, nearly 30dB can be realized. With gain optimization, the noise figure will degrade to about 8dB. With no matching unit at the input, a 9dB noise figure can be expected from a 50Ω source. If the source is terminated, the noise figure will increase to about 15dB. All these noise figures will occur at maximum gain.

The NE5209 has an excellent noise figure vs gain relationship. With any VGA circuit, the noise performance will degrade with decreasing gain. The 5209 has about a 1.2dB noise figure degradation for each 2dB gain reduction. With the input matched for optimum gain, the 8dB noise figure at 23dB gain will degrade to about a 20dB noise figure at 0dB gain.

The NE5209 also displays excellent linearity between voltage gain and control voltage. Indeed, the relationship is of sufficient linearity that high fidelity AM modulation is possible using the NE5209. A maximum control voltage frequency of about 20MHz permits video baseband sources for AM.

A stabilized bandgap reference voltage is made available on the NE5209 (Pin 7). For fixed gain applications this voltage can be resistor divided, and then fed to the gain control terminal (Pin 8). Using the bandgap voltage reference for gain control produces very stable gain characteristics over wide temperature ranges. The gain setting resistors are not part of the RF signal path, and thus stray capacitance here is not important.

The wide bandwidth and excellent gain control linearity make the NE5209 VGA ideally suited for the automatic gain control (AGC) function in RF and IF processing in cellular radio base stations, Direct Broadcast Satellite (DBS) decoders, cable TV systems, fiber optic receivers for wideband data and video, and other radio communication applications. A typical AGC configuration using the NE5209 is shown in Figure 2. Three NE5209s are cascaded with appropriate AC coupling capacitors. The output of the final stage drives the full-wave rectifier composed of two UHF Schottky diodes BAT17 as shown. The diodes are biased by R1 and R2 to V_{CC} such that a quiescent current of about 2mA in each leg is achieved. An NE5230 low voltage op amp is used as an integrator which drives the V_{AGC} pin on all three NE5209s. R3 and C3 filter the high frequency ripple from the full-wave rectified signal. A voltage divider is used to generate the reference for the non-inverting input of the op amp at about 1.7V. Keeping D3 the same type as D1 and D2 will provide a first order compensation for the change in Schottky voltage over the operating temperature range and improve the AGC performance. R6 is a variable resistor for adjustments to the op amp reference voltage. In low cost and large volume applications this could be replaced with a fixed resistor, which would result in a slight loss of the AGC dynamic range. Cascading three NE5209s will give a dynamic range in excess of 60dB.

The NE5209 is a very user-friendly part and will not oscillate in most applications. However, in an application such as with gains in excess of 60dB and bandwidth beyond 100MHz, good PC board layout with proper supply decoupling is strongly recommended.

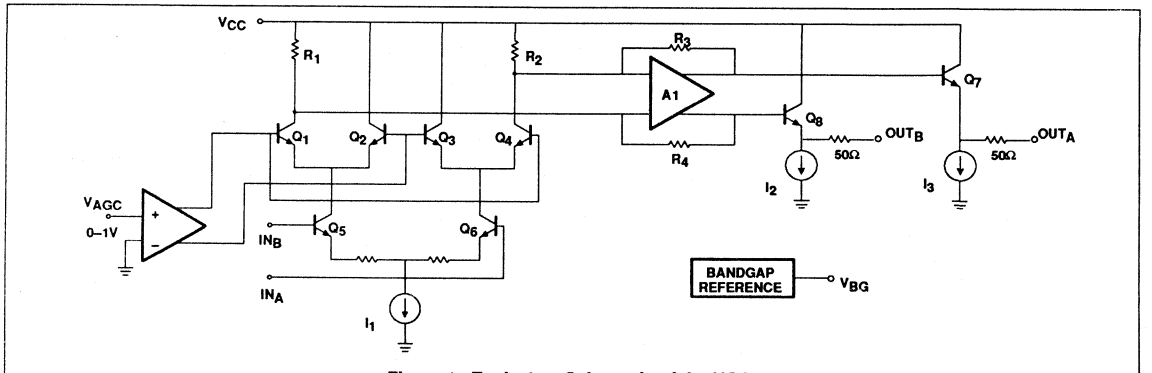


Figure 1. Equivalent Schematic of the VGA

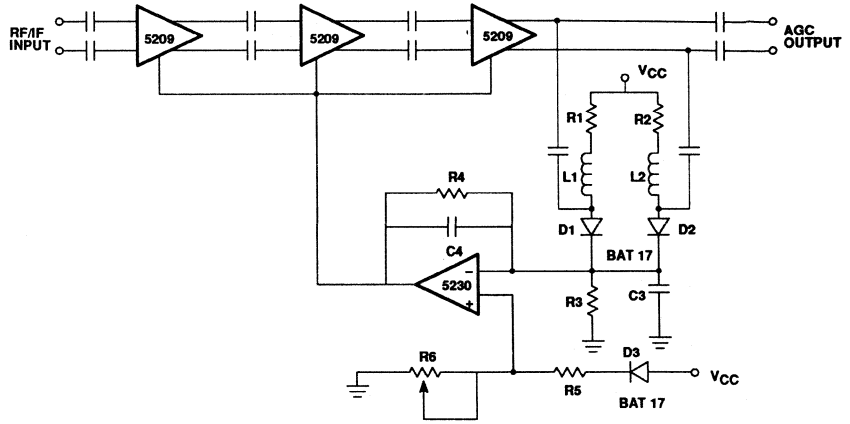


Figure 2. AGC Configuration Using Cascaded NE5209s

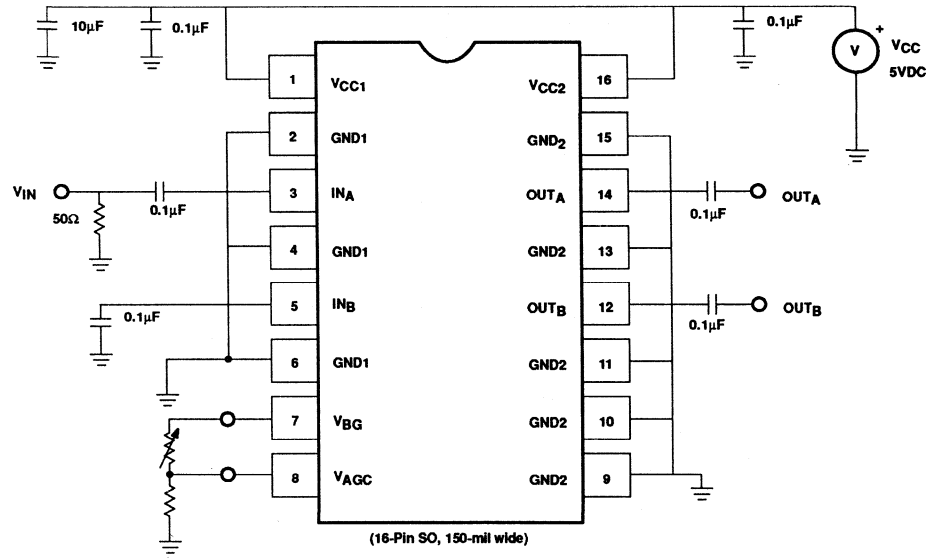
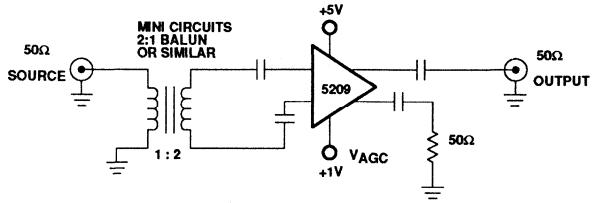
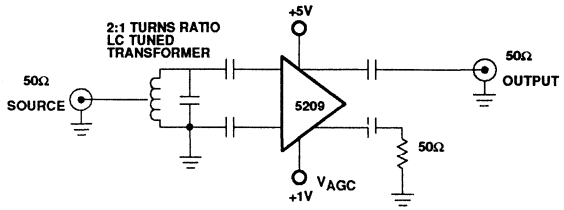


Figure 3. VGA AC Evaluation Board



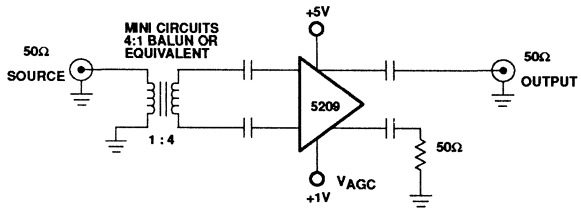
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain.

Figure 4. Broadband Noise Optimization



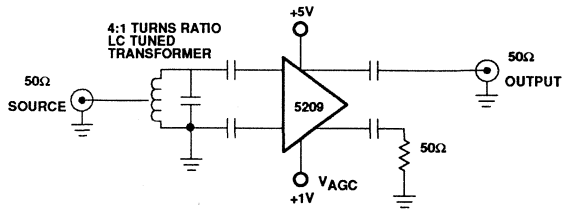
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain. Narrowband circuits have the advantage of greater stability, particularly when multiple devices are cascaded.

Figure 5. Narrowband Noise Optimization



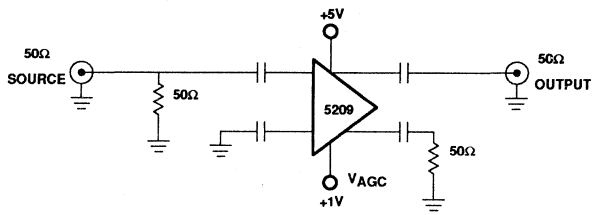
This circuit will exhibit about an 8dB noise figure with 24dB gain.

Figure 6. Broadband Gain Optimization



This circuit will exhibit approximately an 8dB noise figure and 25dB gain.

Figure 7. Narrowband Gain Optimization



The noise figure of this configuration will be approximately 15dB.

Figure 8. Simple Amplifier Configuration

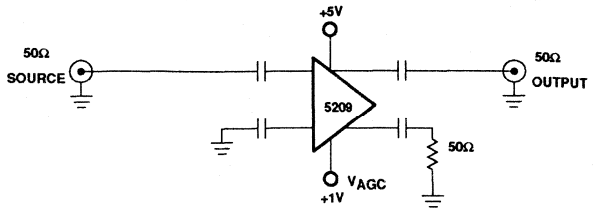


Figure 9 Unterminated Configuration

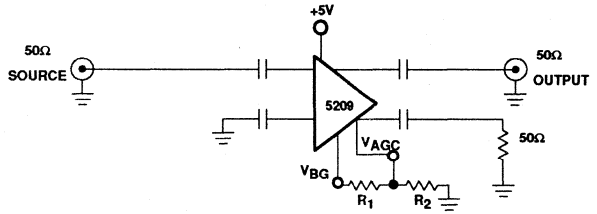


Figure 10. User-Programmable Fixed Gain Block

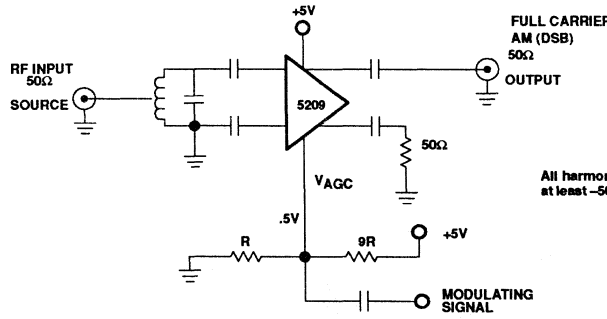


Figure 11. AM Modulator

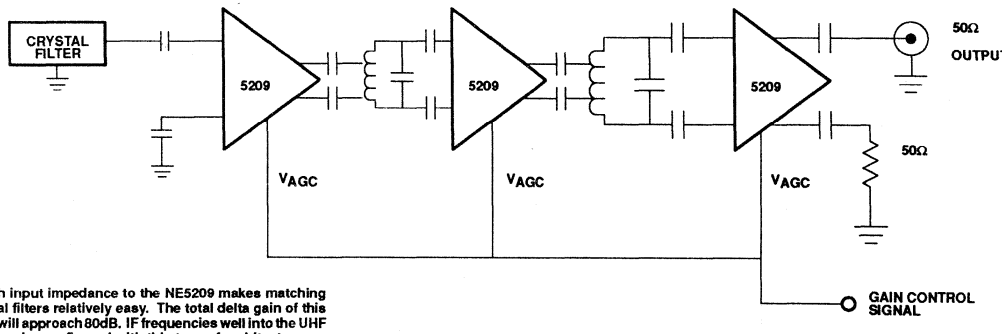


Figure 12. Receiver AGC IF Chain

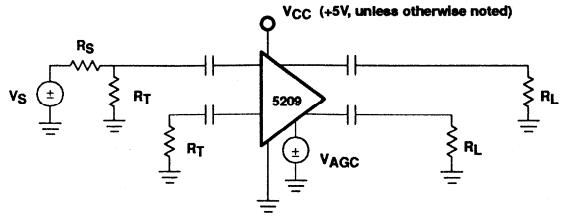


Figure 13. Test Set-up 1 (Used for all Graphs)

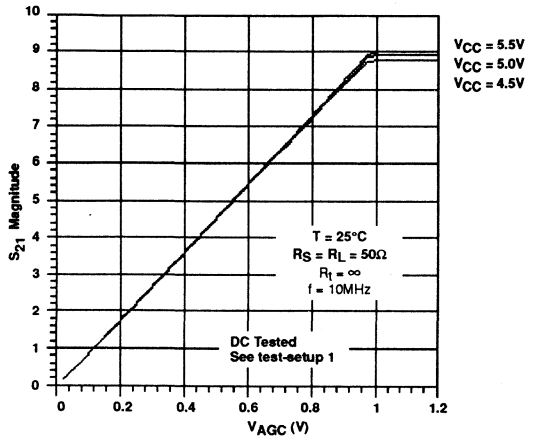


Figure 14. Gain vs V_{AGC} and V_{CC}

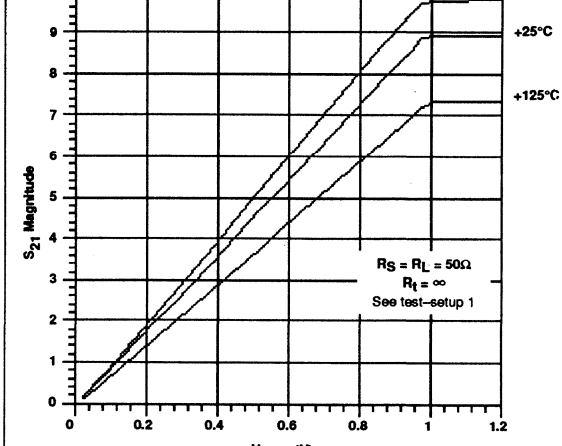


Figure 15. Insertion Gain vs V_{AGC} and Temperature

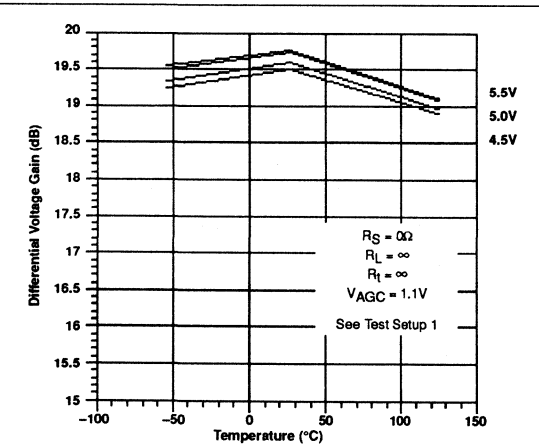


Figure 16. Voltage Gain vs Temperature and V_{CC}

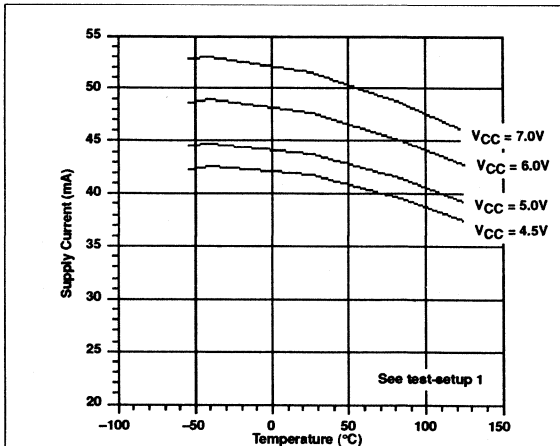


Figure 17. Supply Current vs Temperature and V_{CC}

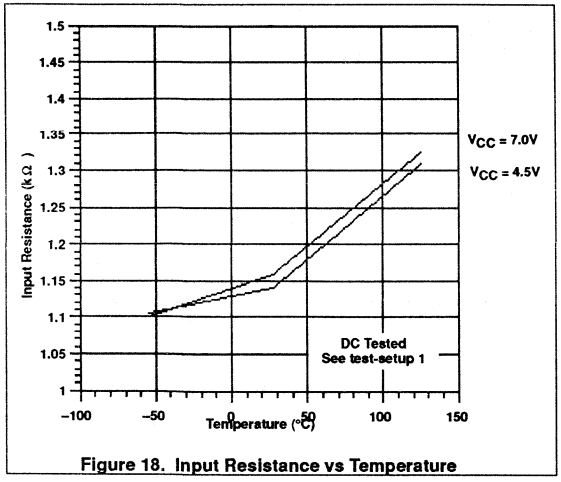


Figure 18. Input Resistance vs Temperature

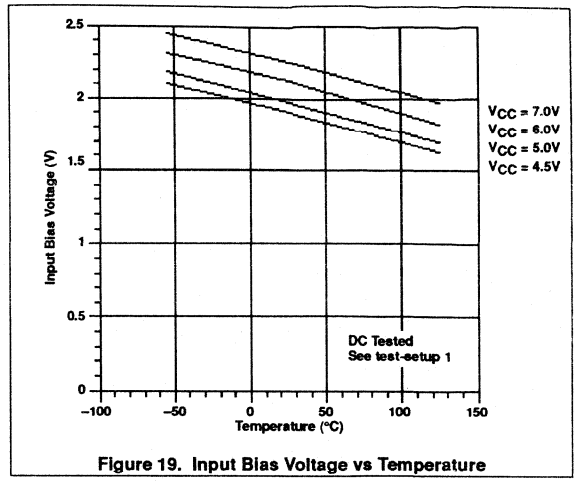


Figure 19. Input Bias Voltage vs Temperature

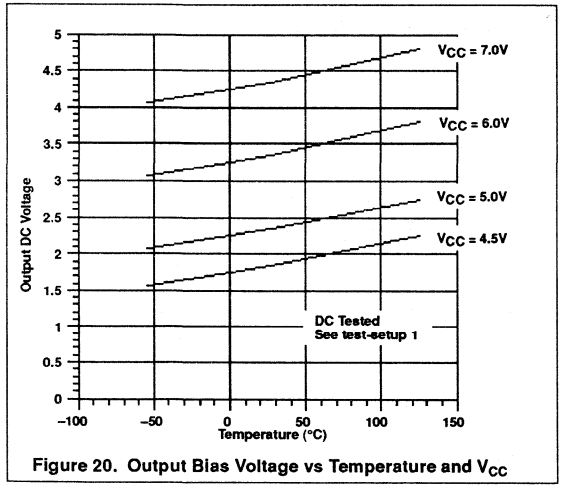


Figure 20. Output Bias Voltage vs Temperature and V_{CC}

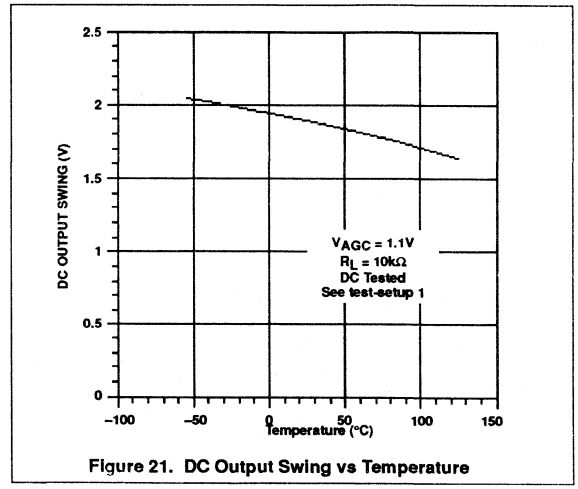


Figure 21. DC Output Swing vs Temperature

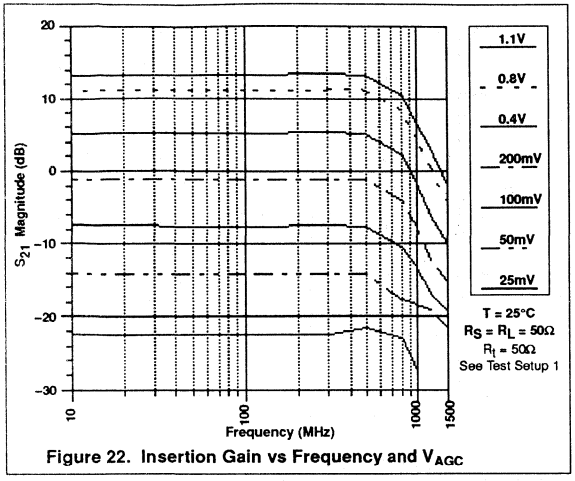


Figure 22. Insertion Gain vs Frequency and V_{AGC}

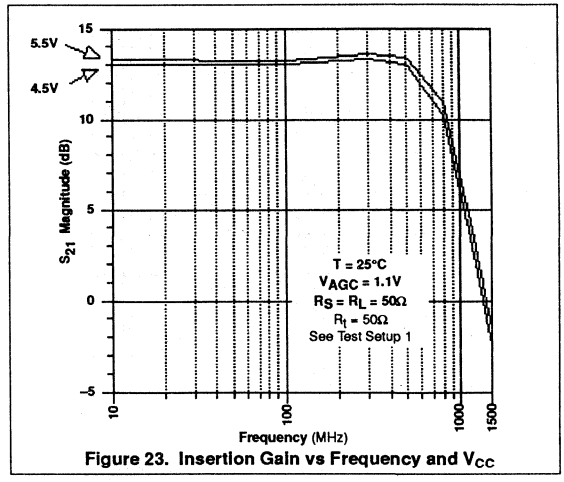


Figure 23. Insertion Gain vs Frequency and V_{CC}

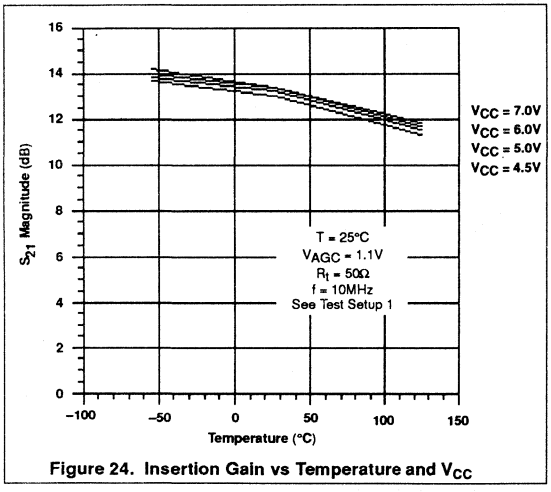


Figure 24. Insertion Gain vs Temperature and V_{CC}

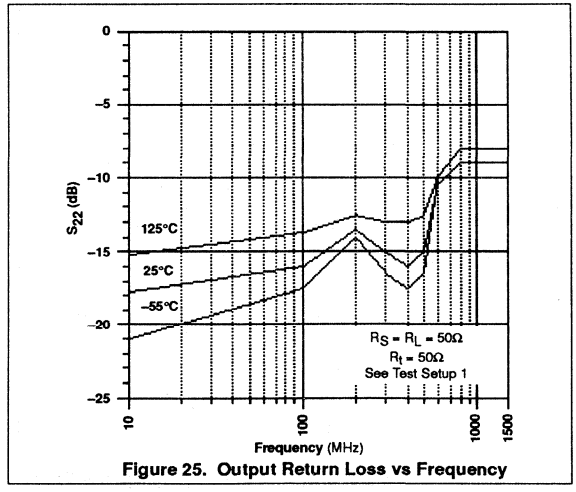


Figure 25. Output Return Loss vs Frequency

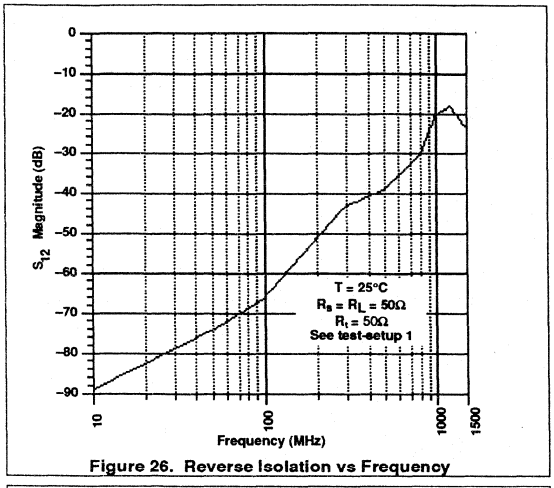


Figure 26. Reverse Isolation vs Frequency

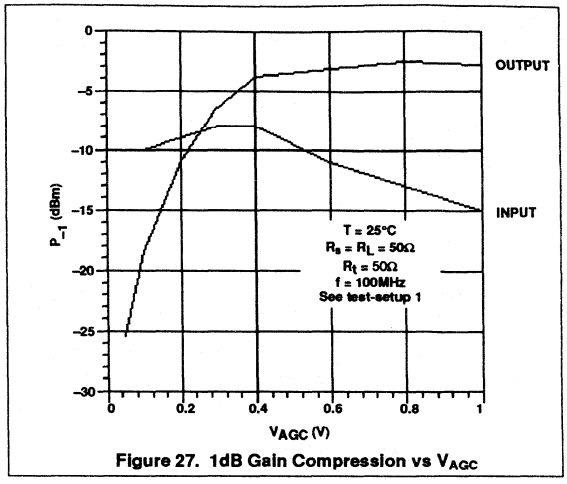


Figure 27. 1dB Gain Compression vs V_{AGC}

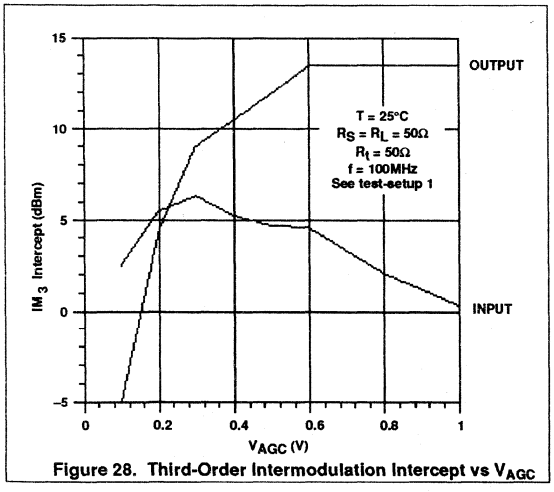


Figure 28. Third-Order Intermodulation Intercept vs V_{AGC}

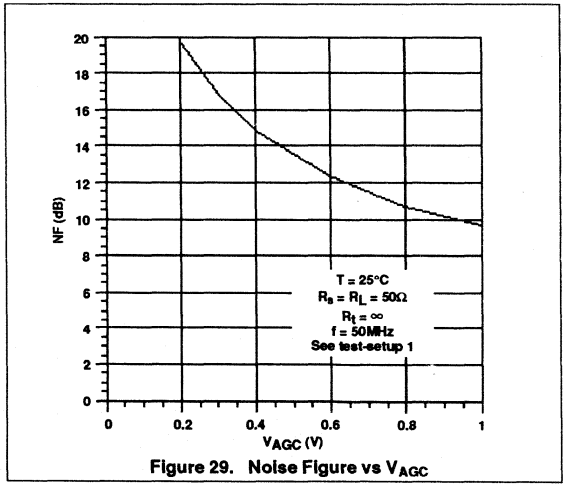


Figure 29. Noise Figure vs V_{AGC}

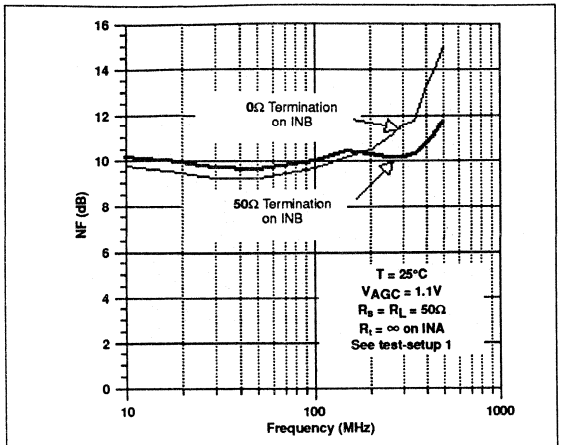


Figure 30. Noise Figure vs Frequency

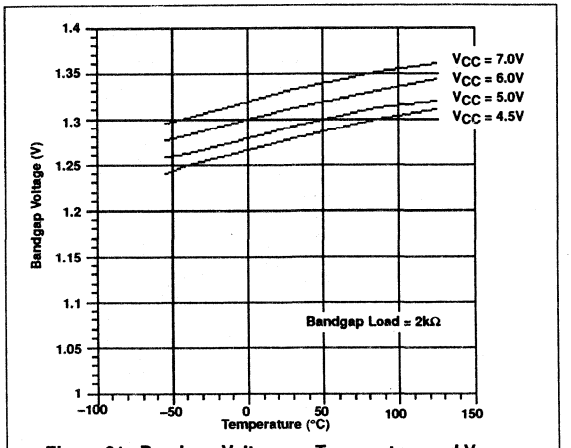


Figure 31. Bandgap Voltage vs Temperature and V_{CC}

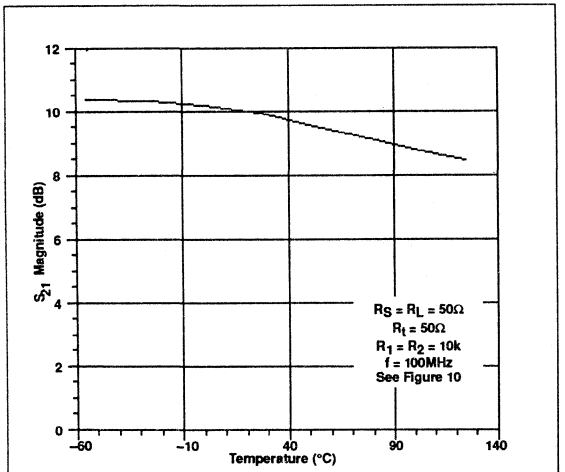
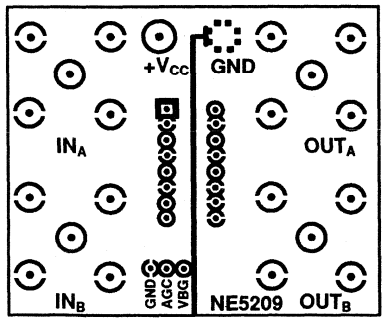
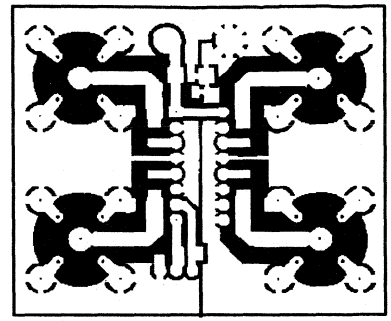


Figure 32. Fixed Gain vs Temperature

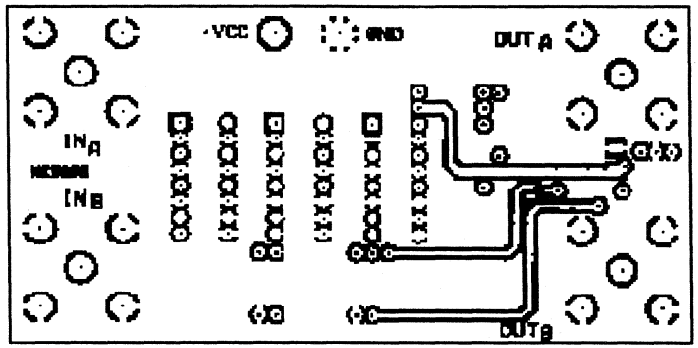


TOP VIEW - COMPONENT SIDE

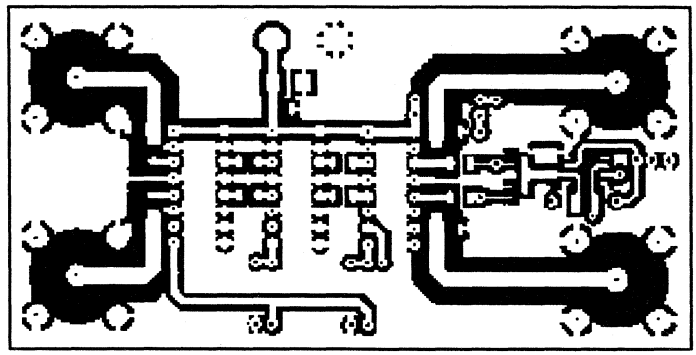


TOP VIEW - SOLDER SIDE

VGA AC Evaluation Board Layout



TOP VIEW - COMPONENT SIDE



TOP VIEW - SOLDER SIDE

AGC Configuration Using Cascaded NE5209s - Layout

NE/SE5539
High Frequency Operational Amplifier

Product Specification

DESCRIPTION

The NE/SE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter-follower inputs provide a true differential high input impedance device. Proper external compensation will allow design operation over a wide range of closed-loop gains, both inverting and non-inverting, to meet specific design requirements.

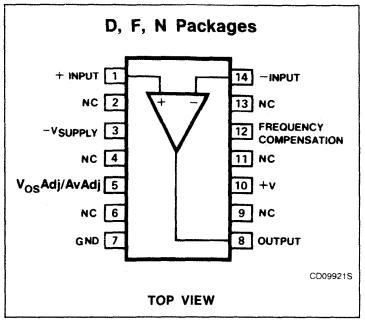
FEATURES

- **Bandwidth**
  - **Unity gain – 350MHz**
  - **Full power – 48MHz**
  - **GBW – 1.2 GHz at 17dB**
- **Slew rate: 600/Vμs**
- **A_{VOL}: 52dB typical**
- **Low noise – 4nV/$\sqrt{Hz}$ typical**
- **MIL-STD processing available**

APPLICATIONS

- **High speed datacomm**
- **Video monitors & TV**
- **Satellite communications**
- **Image processing**
- **RF instrumentation & oscillators**
- **Magnetic storage**
- **Military communications**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE5539N
14-Pin Plastic SO	0 to +70°C	NE5539D
14-Pin Cerdip	0 to +70°C	NE5539F
14-Pin Plastic DIP	−55°C to +125°C	SE5539N
14-Pin Cerdip	−55°C to +125°C	SE5539F

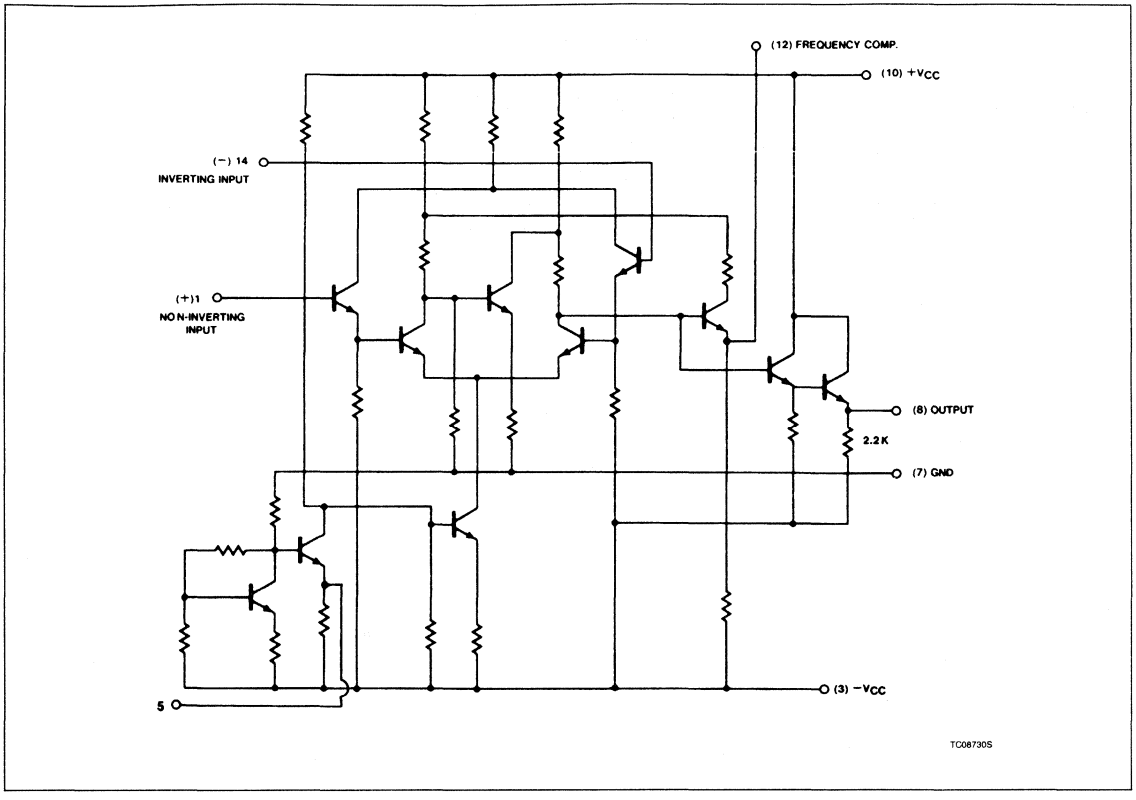
ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±12	V
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still-air)[2]		
	F package	1.17	W
	N package	1.45	W
	D package	0.99	W
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Max junction temperature	150	°C
T_A	Operating temperature range		
	NE	0 to 70	°C
	SE	−55 to +125	°C
T_{SOLD}	Lead temperature (10sec max)	300	°C

NOTES:

1. Differential input voltage should not exceed 0.25V to prevent excessive input bias current and common-mode voltage 2.5V. These voltage limits may be exceeded if current is limited to less than 10mA.
2. Derate above 25°C, at the following rates:
   F package at 9.3 mW/°C
   N package at 11.6 mW/°C
   D package at 7.9 mW/°C

EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		SE5539			NE5539			UNIT
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$V_O = 0V$, $R_S = 100\Omega$	Over temp		2	5				mV
			$T_A = 25°C$		2	3		2.5	5	
	$\Delta V_{OS}/\Delta T$				5			5		µV/°C
I_{OS}	Input offset current		Over temp		0.1	3				µA
			$T_A = 25°C$		0.1	1			2	
	$\Delta I_{OS}/\Delta T$				0.5			0.5		nA/°C
I_B	Input bias current		Over temp		6	25				µA
			$T_A = 25°C$		5	13		5	20	
	$\Delta I_B/\Delta T$				10			10		nA/°C
CMRR	Common-mode rejection ratio	$F = 1kHz$, $R_S = 100\Omega$, $V_{CM} \pm 1.7V$		70	80		70	80		dB
			Over temp	70	80					dB
R_{IN}	Input impedance				100			100		kΩ
R_{OUT}	Output impedance				10			10		Ω

DC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = \pm 8V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			SE5539			NE5539			UNIT
					Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 470Ω to $-V_{CC}$		+Swing				+2.3	+2.7		V
				−Swing				−1.7	−2.2		
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$ to GND	Over temp	+Swing	+2.3	+3.0					V
				−Swing	−1.5	−2.1					
			$T_A = 25°C$	+Swing	+2.5	+3.1					V
				−Swing	−2.0	−2.7					
$I_{CC}+$	Positive supply current	$V_O = 0$, $R_1 = \infty$		Over temp		14	18				mA
				$T_A = 25°C$		14	17		14	18	
$I_{CC}-$	Negative supply current	$V_O = 0$, $R_1 = \infty$		Over temp		11	15				mA
				$T_A = 25°C$		11	14		11	15	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000				μV/V
				$T_A = 25°C$					200	1000	
A_{VOL}	Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 150\Omega$ to GND, 470Ω to $-V_{CC}$						47	52	57	dB
A_{VOL}	Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 2\Omega$ to GND									dB
				$T_A = 25°C$				47	52	57	
A_{VOL}	Large signal voltage gain	$V_O = +2.5V, -2.0V$ $R_L = 2k\Omega$ to GND		Over temp	46		60				dB
				$T_A = 25°C$	48	53	58				

DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			SE5539			UNIT
					Min	Typ	Max	
V_{OS}	Input offset voltage			Over temp		2	5	mV
				$T_A = 25°C$		2	3	
I_{OS}	Input offset current			Over temp		0.1	3	μA
				$T_A = 25°C$		0.1	1	
I_B	Input bias current			Over temp		5	20	μA
				$T_A = 25°C$		4	10	
CMRR	Common-mode rejection ratio	$V_{CM} = \pm 1.3V$, $R_S = 100\Omega$			70	85		dB
$I_{CC}+$	Positive supply current			Over temp		11	14	mA
				$T_A = 25°C$		11	13	
$I_{CC}-$	Negative supply current			Over temp		8	11	mA
				$T_A = 25°C$		8	10	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000	μV/V
				$T_A = 25°C$				
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$	Over temp	+Swing	+1.4	+2.0		V
				−Swing	−1.1	−1.7		
			$T_A = 25°C$	+Swing	+1.5	+2.0		
				−Swing	−1.4	−1.8		

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $R_L = 150\Omega$ to GND & 470Ω to $-V_{CC}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Gain bandwidth product	$A_{CL} = 7$, $V_0 = 0.1\ V_{P-P}$		1200			1200		MHz
	Small-signal bandwidth	$A_{CL} = 2$, $R_L = 150\Omega$[1]		110			110		MHz
t_S	Settling time	$A_{CL} = 2$, $R_L = 150\Omega$[1]		15			15		ns
SR	Slew rate	$A_{CL} = 2$, $R_L = 150\Omega$[1]		600			600		V/μs
t_{PD}	Propagation delay	$A_{CL} = 2$, $R_L = 150\Omega$[1]		7			7		ns
	Full power response	$A_{CL} = 2$, $R_L = 150\Omega$[1]		48			48		MHz
	Full power response	$A_V = 7$, $R_L = 150\Omega$[1]		20			20		MHz
	Input noise voltage	$R_S = 50\Omega$, 1MHz		4			4		$nV/\sqrt{Hz}$
	Input noise current	1MHz		6			6		$pA/\sqrt{Hz}$

NOTE:
1. External compensation.

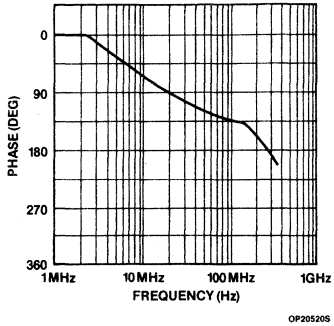
AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			UNIT
			Min	Typ	Max	
BW	Gain bandwidth product	$A_{CL} = 7$		700		MHz
	Small-signal bandwidth	$A_{CL} = 2$[1]		120		MHz
t_S	Settling time	$A_{CL} = 2$[1]		23		ns
SR	Slew rate	$A_{CL} = 2$[1]		330		V/μs
t_{PD}	Propagation delay	$A_{CL} = 2$[1]		4.5		ns
	Full power response	$A_{CL} = 2$[1]		20		MHz

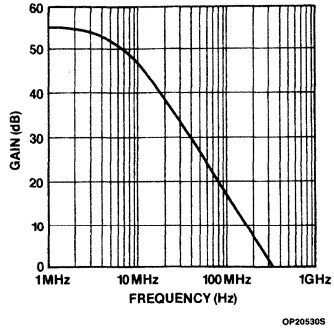
NOTE:
1. External compensation.

TYPICAL PERFORMANCE CURVES

NE5539 Open-Loop Phase

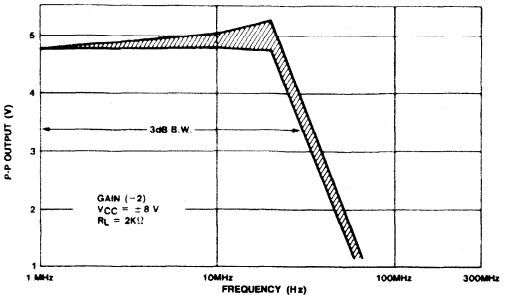


NE5539 Open-Loop Gain



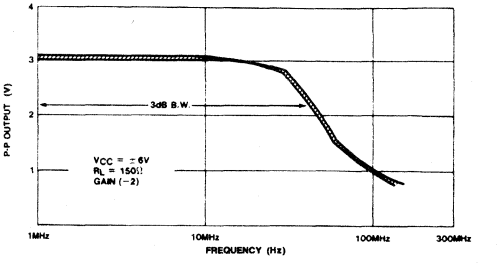
TYPICAL PERFORMANCE CURVES (Continued)

Power Bandwidth (SE)



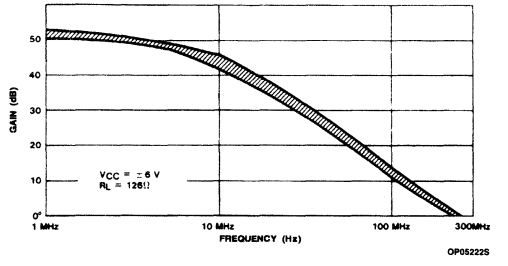
OP05202S

Power Bandwidth (NE)



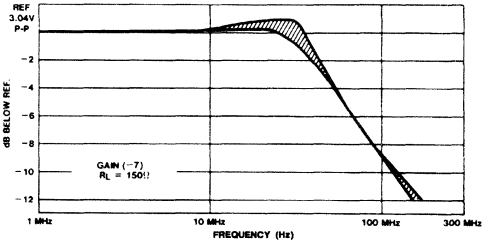
OP05212S

SE5539 Open-Loop Gain vs Frequency



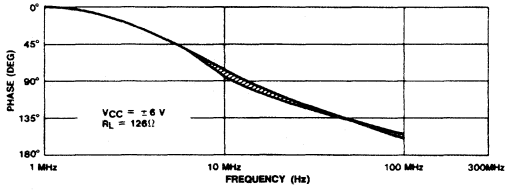
OP05222S

Power Bandwidth

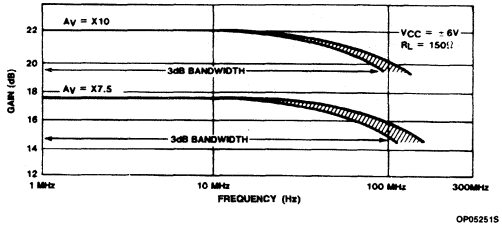


OP05231S

SE5539 Open-Loop Phase vs Frequency



Gain Bandwidth Product vs Frequency



OP05251S

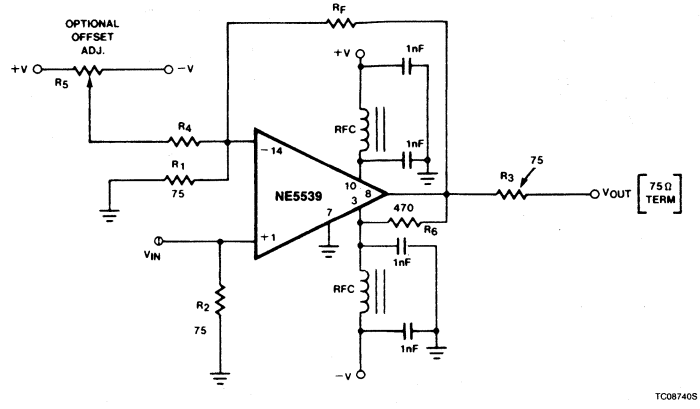
NOTE

Indicates typical distribution $-55°C \leq T_A \leq 125°C$

OP05241S

CIRCUIT LAYOUT CONSIDERATIONS

As may be expected for an ultra-high frequency, wide-gain bandwidth amplifier, the physical circuit layout is extremely critical. Breadboarding is not recommended. A double-sided copper-clad printed cirucit board will result in more favorable system operation. An example utilizing a 28dB non-inverting amp is shown in Figure 1.

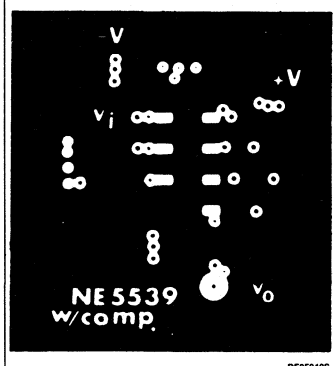


NOTES:
R_1 = 75Ω 5% CARBON
R_2 = 75Ω 5% CARBON
R_3 = 75Ω 5% CARBON
R_4 = 36k 5% CARBON

R_5 = 20k TRIMPOT (CERMET)
R_F = 1.5k (28dB GAIN)
R_6 = 470Ω 5% CARBON

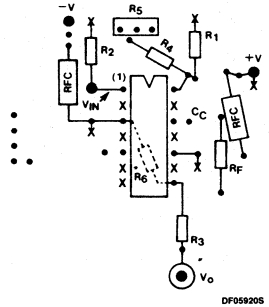
RFC 3T # 26 BUSS WIRE ON FERROXCUBE VK 200 09/3B CORE
BYPASS CAPACITORS
1nF CERAMIC
(MEPCO OR EQUIV.)

Top Plane Copper[1] (Component Side)



DF05910S

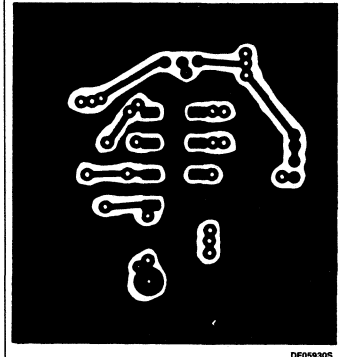
Component Side (Component Layout)



DF05920S

NOTES:
(X) indicates ground connection to top plane.
*R_6 is on bottom side.

Bottom Plane Copper[1]



DF05930S

NOTE:
1. Bond edges of top and bottom ground plane copper.

Figure 1. 28dB Non-Inverting Amp Sample PC Layout

NE5539 COLOR VIDEO AMPLIFIER

The NE5539 wideband operational amplifier is easily adapted for use as a color video amplifier. A typical circuit is shown in Figure 2 along with vector-scope[1] photographs showing the amplifier differential gain and phase response to a standard five-step modulated staircase linearity signal (Figures 3, 4 and 5). As can be seen in Figure 4, the gain varies less than 0.5% from the bottom to the top of the staircase. The maximum differential phase shown in Figure 5 is approximately +0.1°.

The amplifier circuit was optimized for a 75Ω input and output termination impedance with a gain of approximately 10 (20dB).

NOTE:

1. The input signal was 200mV and the output 2V. V_{CC} was ±8V.

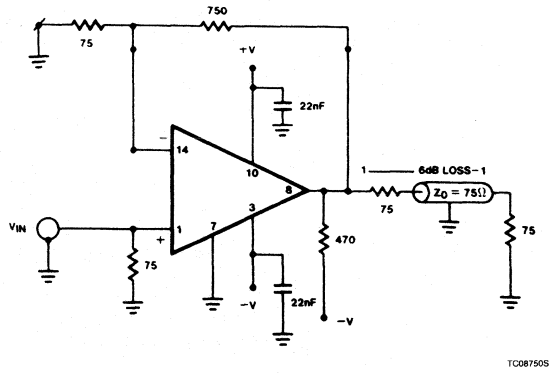


Figure 2. NE5539 Video Amplifier

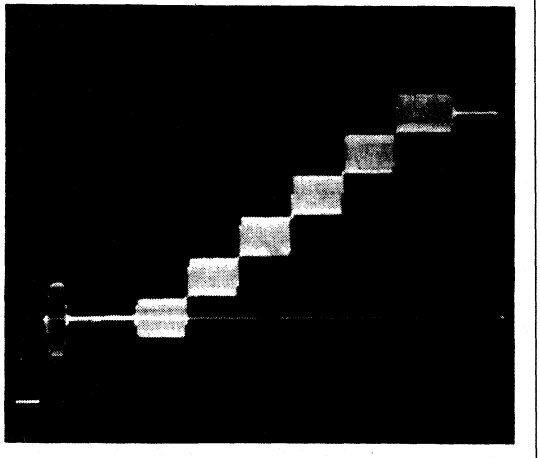


Figure 3. Input Signal

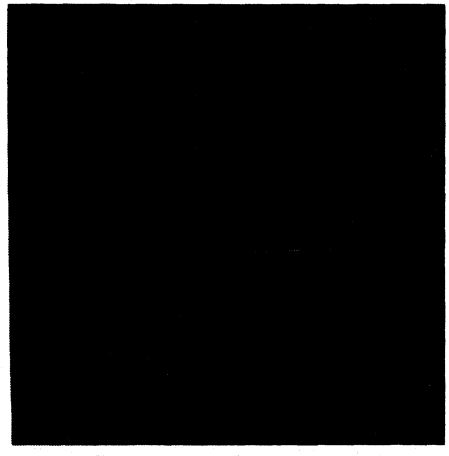


Figure 4. Differential Gain < 0.5%

NOTE:

Instruments used for these measurements were Tektronix 146 NTSC test signal generator, 520A NTSC vectorscope, and 1480 waveform monitor.

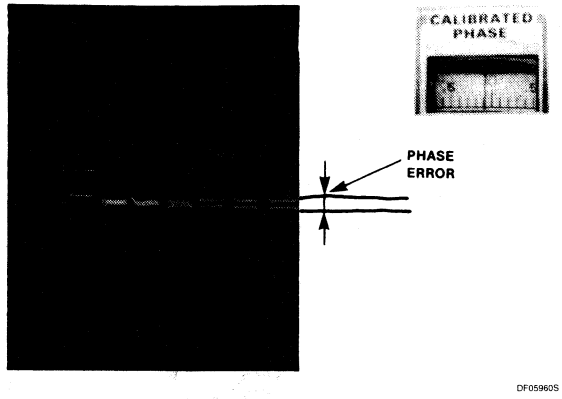


Figure 5. Differential Phase +0.1°

APPLICATIONS

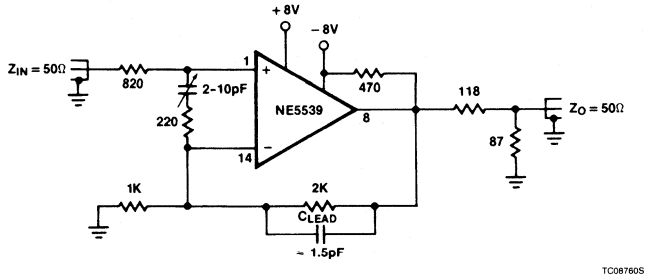


Figure 6. Non-Inverting Follower

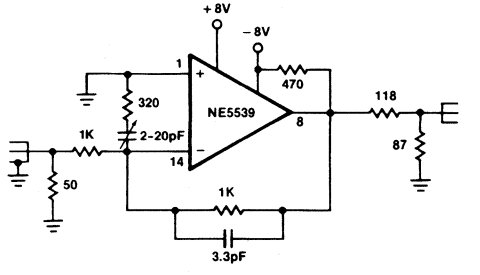


Figure 7. Inverting Follower

NE5592
Video Amplifier

Product Specification

DESCRIPTION

The NE5592 is a dual monolithic, two-stage, differential output, wideband video amplifier. It offers a fixed gain of 400 without external components and an adjustable gain from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers.

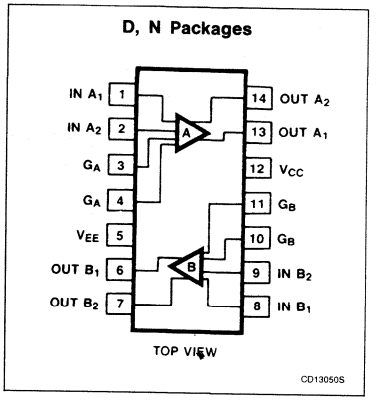
FEATURES

- **110MHz unity gain bandwidth**
- **Adjustable gain from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**

APPLICATIONS

- **Floppy disk head amplifier**
- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memory**
- **Video recorder systems**

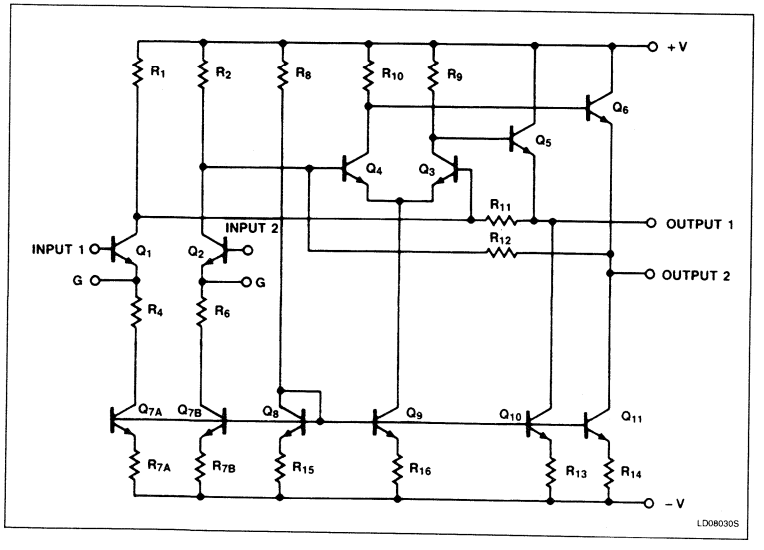
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to 70°C	NE5592N
14-Pin SO package	0 to 70°C	NE5592D

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common mode Input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating temperature range NE5592	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
$P_{D\ MAX}$	Maximum power dissipation, $T_A = 25°C$ (still air)[1] D package N package	 1.03 1.48	 W W

NOTE:
1. Derate above 25°C at the following rates:
   D package 8.3mW/°C
   N package 11.9mW/°C

DC ELECTRICAL CHARACTERISTICS $T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltage is $V_S = \pm 6.0V$, and gain select pins are connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
A_{VOL}	Differential voltage gain	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	400	480	600	V/V
R_{IN}	Input resistance		3	14		kΩ
C_{IN}	Input capacitance			2.5		pF
I_{OS}	Input offset current			0.3	3	μA
I_{BIAS}	Input bias current			5	20	μA
	Input noise voltage	BW 1kHz to 10MHz		4		$nV/\sqrt{Hz}$
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio	$V_{CM} \pm 1V$, $f < 100kHz$ $V_{CM} \pm 1V$, $f = 5MHz$	60	93 87		dB dB
PSRR	Supply voltage rejection ratio	$\Delta V_S = \pm 0.5V$	50	85		dB
	Channel separation	$V_{OUT} = 1V_{P-P}$; $f = 100kHz$ (output referenced) $R_L = 1k\Omega$	65	70		dB
V_{OS}	Output offset voltage gain select pins open	$R_L = \infty$ $R_L = \infty$		0.5 0.25	1.5 0.75	V V
V_{CM}	Output common-mode voltage	$R_L = \infty$	2.4	3.1	3.4	V
V_{OUT}	Output differential voltage swing	$R_L = 2k\Omega$	3.0	4.0		V
R_{OUT}	Output resistance			20		Ω
I_{CC}	Power supply current (total for both sides)	$R_L = \infty$		35	44	mA

DC ELECTRICAL CHARACTERISTICS

$V_{SS} = \pm 6V$, $V_{CM} = 0$, $0°C \leq T_A \leq 70°C$, unless otherwise specified. Recommended operating supply voltage is $V_S = \pm 6.0V$, and gain select pins are connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
A_{VOL}	Differential voltage gain	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	350	430	600	V/V
R_{IN}	Input resistance		1	11		kΩ
I_{OS}	Input offset current				5	μA
I_{BIAS}	Input bias current				30	μA
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio	$V_{CM} \pm 1V$, $f < 100kHz$ $R_S = \phi$	55			dB
PSRR	Supply voltage rejection ratio	$\Delta V_S = \pm 0.5V$	50			dB
	Channel separation	$V_{OUT} = 1V_{P-P}$; $f = 100kHz$ (output referenced) $R_L = 1k\Omega$		70		dB
V_{OS}	Output offset voltage gain select pins connected together	$R_L = \infty$			1.5	V
	gain select pins open	$R_L = \infty$			1.0	V
V_{OUT}	Output differential voltage swing	$R_L = 2k\Omega$	2.8			V
I_{CC}	Power supply current (total for both sides)	$R_L = \infty$			47	mA

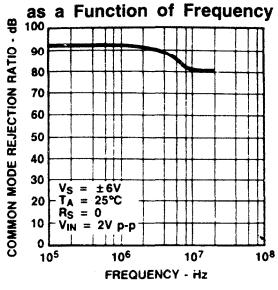
AC ELECTRICAL CHARACTERISTICS

$T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltage $V_S = \pm 6.0V$. Gain select pins connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
BW	Bandwidth	$V_{OUT} = 1V_{P-P}$		25		MHz
t_R	Rise time			15	20	ns
t_{PD}	Propagation delay	$V_{OUT} = 1V_{P-P}$		7.5	12	ns

TYPICAL PERFORMANCE CHARACTERISTICS

Common-Mode Rejection Ratio as a Function of Frequency



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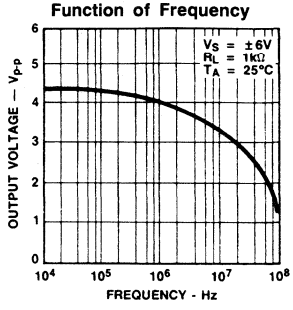
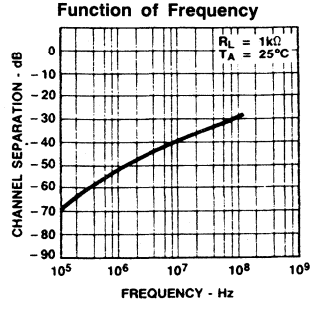
Output Voltage Swing as a Function of Frequency



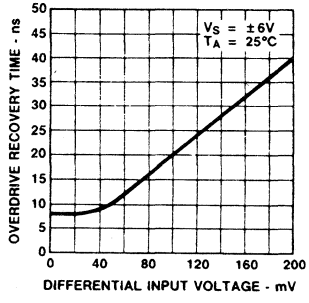
OP18590S

Channel Separation as a Function of Frequency



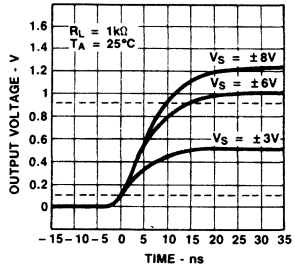
OP18600S

Differential Overdrive Recovery Time



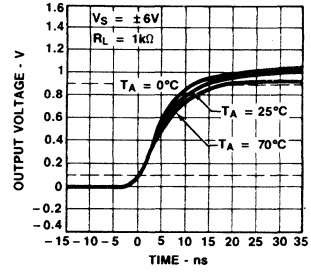
OP18610S

Pulse Response as a Function of Supply Voltage



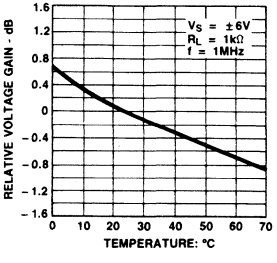
OP18620S

Pulse Response as a Function of Temperature



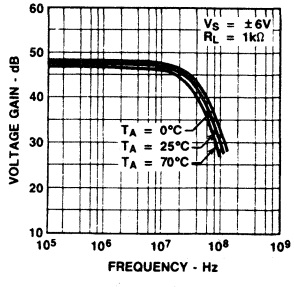
OP18630S

Voltage Gain as a Function of Temperature



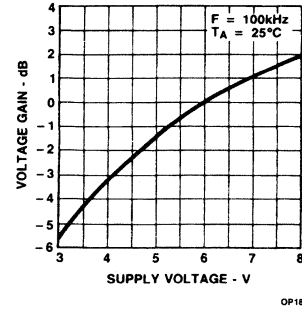
OP18640S

Gain vs Frequency as a Function of Temperature



OP18650S

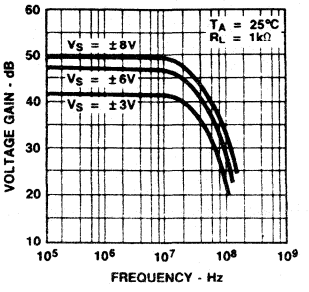
Voltage Gain as a Function of Supply Voltage



OP18660S

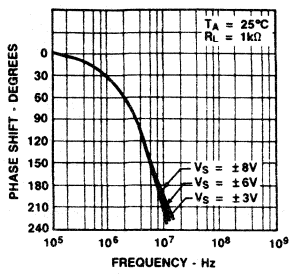
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Gain vs Frequency as a Function of Supply Voltage



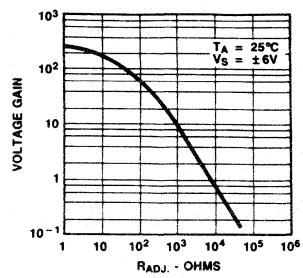
OP18670S

Phase vs Frequency as a Function of Supply Voltage



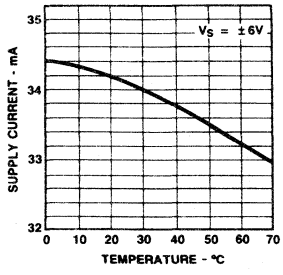
OP18680S

Voltage Gain as a Function of R_{ADJ}



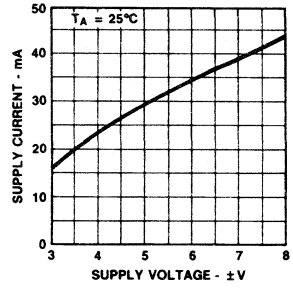
OP18690S

Supply Current as a Function of Temperature



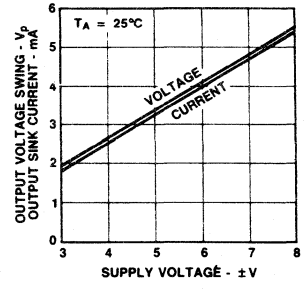
OP18700S

Supply Current as a Function of Supply Voltage



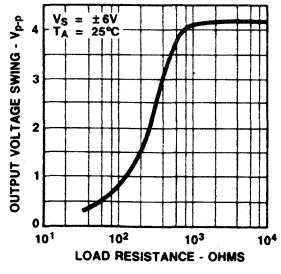
OP18710S

Output Voltage Swing and Sink Current as a Function of Supply Voltage



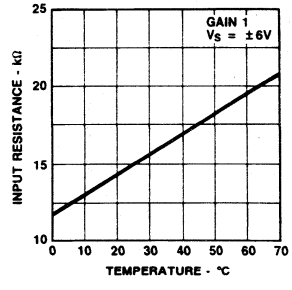
OP18720S

Output Voltage Swing as a Function of Load Resistance



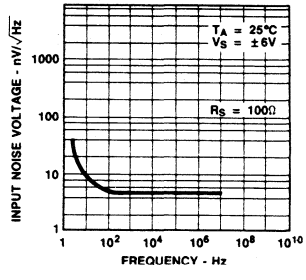
OP18730S

Input Resistance as a Function of Temperature



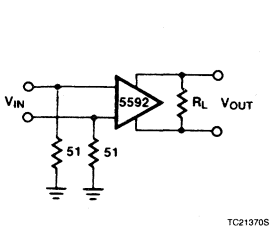
OP18740S

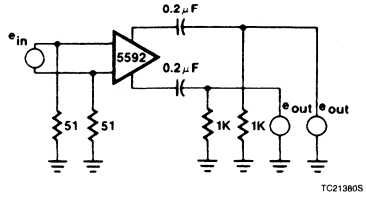
Input Noise Voltage as a Function of Frequency

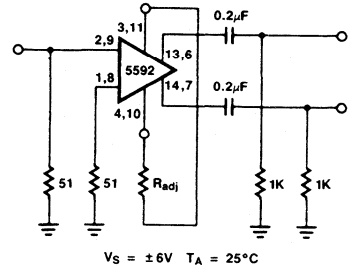


OP18750S

TEST CIRCUITS T_A = 25°C, unless otherwise specified.







Microcontroller for television and video (MTV)

83C053/83C054/87C054

DESCRIPTION

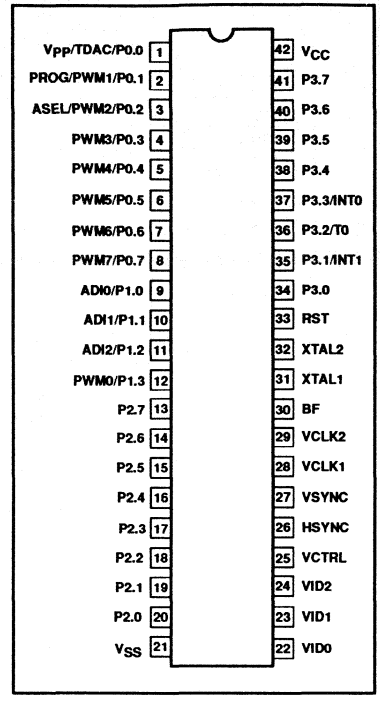
The Microcontroller for Television and Video (MTV) applications is a derivative of Philips' industry-standard 80C51 microcontroller that is intended for use as the central control mechanism in a television receiver or tuner. Providing tuner functions and an On Screen Display facility, it represents a next-generation replacement for the currently available parts.

The MTV is available in either an 8K masked ROM, 16K masked ROM, or 16K One Time Programmable (OTP) EPROM version. The only difference between these versions is the size or type of program memory.

FEATURES

- 8192 × 8 masked ROM (83C053), 16384 × 8 masked ROM (83C054), or 16384 × 8 OTP EPROM (87C054)
- 192 × 8 RAM
- On Screen Display (OSD) Controller
- Three digital video outputs
- Multiplexer/mixer and background intensity controls
- Flexible formatting with OSD New Line Option
- 128 × 10 display RAM
- 60 × 18 × 14 character generator ROM
- Eight text-shadowing modes
- Text color selectable per character
- Background color selectable per word
- Background color vs. video selectable per character
- Eight 6-bit pulse width modulators for analog voltage integration
- One 14-bit PWM for high-precision voltage integration
- D/A converter and comparator with three-input multiplexer
- Nine dedicated I/Os plus 28 port bits
- 15 port bits have alternate uses
- Four high-current open-drain port outputs
- 12 high-voltage (+12V) open drain outputs
- Programmable video input and output polarities
- 80C51 instruction set
- No external memory capability
- 42-pin shrunk DIP (0.07-inch center pins)
- High-speed CMOS technology
- 5V ± 10% operation

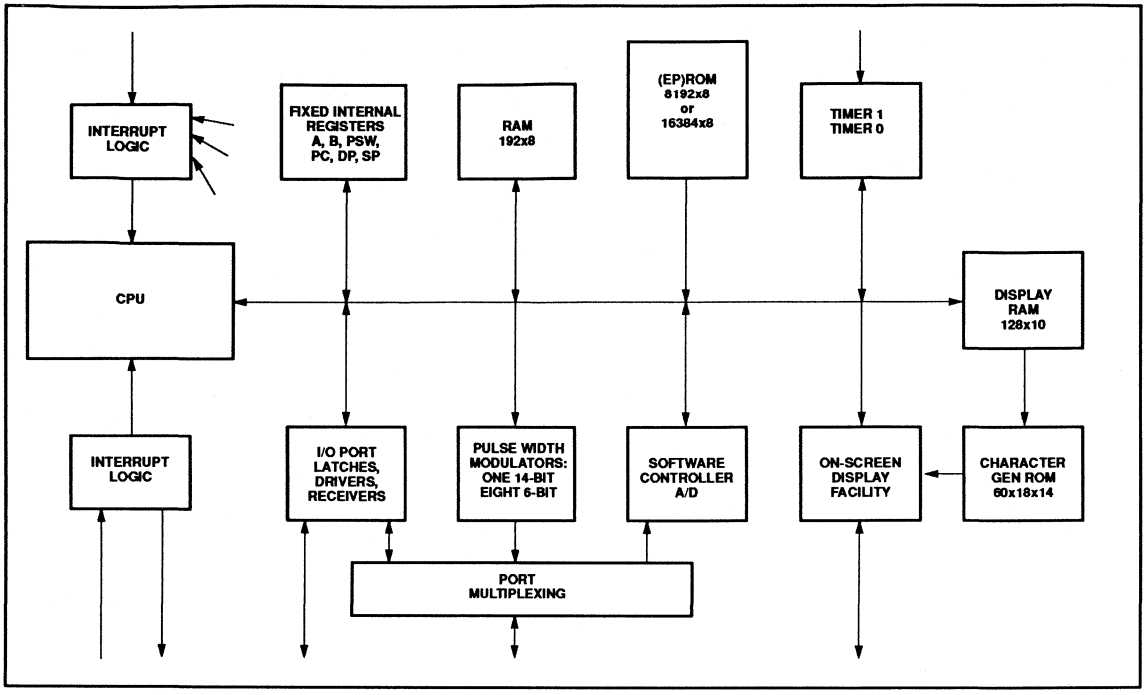
PIN CONFIGURATION



PART NUMBER SELECTION

ROM	EPROM	TEMPERATURE AND PACKAGE	FREQUENCY
P83C053BBP NB		0 to +70°C, plastic DIP	3.5 to 12MHz
P83C054BBP NB	P87C054BBP NB	0 to +70°C, plastic DIP	3.5 to 12MHz

BLOCK DIAGRAM



PIN DESCRIPTIONS

MNEMONIC	PIN NO. DIP	TYPE	NAME AND FUNCTION
VCLK1	28	I	**Video Clock 1:** Input for the horizontal timing reference for the On Screen Display facility. VCLK1 and VCLK2 are intended to be used with an external LC circuit to provide an on-chip oscillator. The period of the video clock is determined such that the width of a pixel in the On Screen Display is equal to the inter-line separation of the raster.
VCLK2	29	O	**Video Clock 2:** Output from the on-chip video oscillator.
HSYNC	26	I	**Horizontal Sync:** A dedicated input for a TTL-level version of the horizontal sync pulse. The polarity of this pulse is programmable; its trailing edge is used by the On Screen Display facility as the reference for horizontal positioning.
VSYNC	27	I	**Vertical Sync:** A dedicated input for a TTL-level version of the vertical sync pulse. The polarity of this pulse is programmable, and either edge can serve as the reference for vertical timing.
VID2:0	22–24	O	**Digital Video bus:** Three totem pole outputs comprising digital RGB (or other color encoding) from the On Screen Display facility. The polarity of these outputs is controlled by a programmable register bit.
VCTRL	25	O	**Video Control:** A totem-pole output indicating whether the On Screen Display facility is currently presenting active video on the VID2:0 outputs. This signal should be used to control an external multiplexer (mixer) between normal video and the video derived from VID2:0. The polarity of this outputs is controlled by a programmable register bit.
BF	30	O	**Background/Foreground:** A totem-pole output which, when VCTRL is active, indicates whether the current video data represents a foreground (low) or background (high) dot in a character. This signal can be used to reduce the intensity of the background color and thus emphasize the text. If a 40-pin version of this part is ever produced, BF will not be pinned out.
P0.0-P0.7	1–8	I/O	**Port 0:** An 8-bit open-drain bidirectional port. Port 0 pins that have ones written to them float, and in that state can be used as high-impedance inputs. The port 0 pins can also serve as outputs from the high-precision Pulse Width Modulator (TDAC) and seven of the eight lower-precision Pulse Width Modulator functions. For each PWM block, a register bit controls whether the corresponding pin is controlled by the block or by port 0; port 0 controls the pin immediately after a Reset. Regardless of how each pin is controlled, it can be externally pulled up as high as +12V±5%, and the state of the pin can be read from the Port 0 register by the program.
	1	I	**V_{PP} (P0.0)** – This pin receives the 12V programming supply voltage during EPROM programming.
	2	I	**PROG (P0.1)** – This pin receives the programming pulses during EPROM programming.
	3	I	**ASEL (P0.2)** – Input which indicates which bits of the EPROM address are applied to port 2.
	1	O	**TDAC (P0.0)** – This is the output for the 14-bit high-precision PWM.
	2–8	O	**PWM1–7 (P0.1–P0.7)** – Outputs for the 6-bit PWMs 1 through 7.
P1.0-P1.3	9–12	I/O	**Port 1:** A 4-bit open-drain bidirection port. Port 1 pins that have ones written to them float, and in that state can be used as high-impedance inputs. P1.3 can also serve as the eighth lower-precision Pulse Width Modulator output (PWM0), and can be externally pulled up as high as +12V±5%. P1.2:0 have optional alternate use as ADI2:0, inputs to the Software A/D conversion facility. If a 40-pin version of this part is ever produced, P1.3/PWM0 will not be pinned out. Any of the port 1 pins are driven low if the corresponding port register bit is written as 0, or, for P1.3 only, if the TDAC module presents a 0. The state of the pin can always be read from the port register by the program.
	9–11	I	**ADI0–2 (P1.0–P1.2)** – Inputs for the software A/D facility.
	12	O	**PWM0 (P1.3)** – Output for the PWM0 6-bit PWM.
P2.0-P2.7	20–13	I/O	**Port 2:** An 8-bit open-drain bidirectional port. Port 2 pins that have ones written to them float, and in that state can be used as high-impedance inputs. P2.3:0 have high current capability (10 mA at 0.5V) for LEDs. Any of the port 2 pins are driven low if the port register bit is written as 0. The state of the pin can always be read from the port register by the program.
P3.0-P3.7	34–42	I/O	**Port 3:** An 8-bit open-drain bidirectional port. Port 3 pins that have ones written to them float, and in that state can be used as high-impedance inputs. P3.0, P3.4, and P3.7 can be externally pulled up as high as +12V±5%, while P3.5 and P3.6 have 10mA drive capability. Some of the port 3 pins can also serve alternate functions, as follows:
	35	I	**INT1 (P3.1)** – External Interrupt 1.
	36	I	**T0 (P3.2)** – Timer 0 external input.
	37	I	**INT0 (P3.3)** – External Interrupt 0.

PIN DESCRIPTIONS (Continued)

MNEMONIC	PIN NO. DIP	TYPE	NAME AND FUNCTION
RST	33	I	**Reset:** If this pin is high for two machine cycles (24 oscillator periods) while the oscillator is running, the MTV is reset. Also, this pin is used as a serial input to enter a test or EPROM programming mode, as on the 87C751.
XTAL1	31	I	**Crystal 1:** Input to the inverting oscillator amplifier and clock generator circuit that provides the timing reference for all MTV logic other than the OSD facility. XTAL1 and XTAL2 can be used with a quartz crystal or ceramic resonator to provide an on-chip oscillator. Alternatively, XTAL1 can be conncected to an external clock, and XTAL2 left unconnected.
XTAL2	32	O	**Crystal 2:** Output from the inverting oscillator amplifier.
V_{CC}		I	**Power Supply:** This is the power supply for normal and power-down modes.
V_{SS}		I	**Ground:** 0V reference.

ROM CODE SUBMISSION

When submitting a ROM code for the 83C053 or 83C054, the following must be specified:

1. The 8k byte (83C053), or 16k byte (83C054) user ROM program.
2. The OSD ROM space.

This information can be submitted in an 87C054, or in two EPROMs (2764), or electronically on the ROM Code Bulletin Board (see your local sales office for the number).

ROM CODE SUBMITTAL REQUIREMENTS

ADDRESS	CONTENT	COMMENT
0000H to 1FFFH (83C053) 000H to 3FFFH (83C054)	DATA	User ROM data
C000H to CFFFH	OSD	On-Screen Display character table

PROGRAMMING THE OSD EPROM

Overview

The OSD EPROM space starts at location C000H and ends at location CFFFH. However, not all locations within this space are used, due to the addressing scheme of the OSD.

The start location of the next character can be calculated by adding 40H to the start location of the previous character. For example, character #1 starts at C000H; then characters 2, 3, and 4 start at C040H, C080H, and C0C0H, respectively.

Character Description

Each character is 14 bits wide by 18 lines high.

A character is split about a vertical axis into two sections, UPPER and LOWER. Each section contains 7 bits of the character, such that the LOWER section contains 1–7 and the UPPER section contains bits 8–14.

NOTE: During programming and verification, each section is programmed using bytes of DATA. The MSB of the DATA is not used; however, the MSB location physically exists, and so will program and verify.

The LOWER section of the character is programmed when the LSB of the program address equals 0, and the UPPER section when the LSB equals 1.

Character Programming

An example of an OSD character bit map, and the program DATA to obtain that character is shown in Table 1.

OSD EPROM Bit Map

The mapping for the full OSD EPROM is shown in Table 2.

Example

To program the character given above into the first character location of the OSD EPROM would require the following address/DATA sequence:

C000/00H;	C001/00H;	C002/00H;
C003/00H;	C004/0CH;	C005/1EH;
C006/0CH;	C007/1EH;	C008/0CH;
C009/1EH;	C00A/0CH;	C00B/1EH;
C00C/0CH;	C00D/1EH;	C00E/0CH;
C00F/1EH;	C010/7CH;	C011/1FH;
C012/7CH;	C013/1FH;	C014/7CH;
C015/1FH;	C016/0CH;	C017/1EH;
C018/0CH;	C019/1EH;	C01A/0CH;
C01B/1EH;	C01C/0CH;	C01D/1EH;
C01E/0CH;	C01F/1EH;	C020/00H;
C021/00H;	C022/00H;	C023/00H

Table 1. Example of an OSD Character Bit Map

CHARACTER BIT MAP		PROGRAM DATA	
	UPPER LOWER ←— —→←— —→ 11111 43210987654321	UPPER	LOWER
Line 1 →	00000000000000	X0000000	X0000000
Line 2 →	00000000000000	X0000000	X0000000
Line 3 →	00111100001100	X0011110	X0001100
Line 4 →	00111100001100	X0011110	X0001100
Line 5 →	00111100001100	X0011110	X0001100
Line 6 →	00111100001100	X0011110	X0001100
Line 7 →	00111100001100	X0011110	X0001100
Line 8 →	00111100001100	X0011110	X0001100
Line 9 →	00111100001100	X0011110	X0001100
Line 10 →	00111100001100	X0011110	X0001100
Line 11 →	00111111111100	X0011111	X1111101
Line 12 →	00111111111100	X0011111	X1111101
Line 13 →	00111111111100	X0011111	X1111101
Line 14 →	00111100001100	X0011110	X0001100
Line 15 →	00111100001100	X0011110	X0001100
Line 16 →	00111100001100	X0011110	X0001100
Line 17 →	00111100001100	X0011110	X0001100
Line 18 →	00111100001100	X0011110	X0001100
	00111100001100	X0011110	X0001100
	00000000000000	X0000000	X0000000
	00000000000000	X0000000	X0000000

NOTE:
X can be 0 or 1, and will program and verify correctly.

Table 2. OSD EPROM Bit Map

CHARACTER NO.	ADDRESS	CHARACTER LINE NO.	COMMENTS
1	C000 C001 C002 C003 • • • C022 C023 C024–C03F	1 1 2 2 • • • 18 18 Unused	Lower byte Upper byte Lower byte Upper byte • • • Lower byte Upper byte
2	C040–C063 C064–C07F	1–18 Unused	
3	C080–C0A3 C0A4–C0BF	1–18 Unused	
• • •	• • •	• • •	• • •
62	CFC0–CFE3 CFE4–CFFF	1–18 Unused	NEWLINE
63	CFC0–CFE3 CFE4–CFFF	1–18 Unused	BSPACE
64	CFC0–CFE3 CFE4–CFFF	1–18 Unused	SPLITBSPACE

NOTE:
Locations 62, 63, and 64 should be programmed to 0's.

COMPARISON TO THE 80C51

The elements of the MTV are shown in the Block Diagram. The features of the MTV are identical to those of the 80C51, except as noted herein.

Pinout and Testing

Since neither data nor program memory is externally expandable on the MTV, the 80C51 pins ALE, $\overline{EA}$, and $\overline{PSEN}$ are not implemented on the MTV.

I/O Ports

On both the 80C51 and the MTV, port 0 is open-drain, but on the 80C51 it can be used for external memory expansion while on the MTV its alternate use is for Pulse Width Modulated outputs.

On the 80C51, port 1 is 8 bits, is mostly unallocated (general purpose), and is quasi-bidirectional (that is, having a weak pullup transistor that can be overdriven). On the MTV it is a 4-bit open-drain port, and includes alternate uses for analog inputs and a PWM output.

On the 80C51, port 2 is quasi-bidirectional and can be used for external memory expansion; on the MTV, port 2 is open-drain and unallocated.

On the 80C51, port 3 is quasi-bidirectional and all eight bits have alternate uses. On the MTV, three port 3 bits have some of the same alternate uses as on the 80C51 but not necessarily on the same pins, while five pins are open-drain and unallocated.

Idle Mode

The idle mode is not implemented on the MTV.

Power-Down Mode

The power-down mode is not implemented on the MTV. The PCON register has the following format:

PCON

7	6	5	4	3	2	1	0
–	–	–	–	GF1	GF0	–	–

Interrupts

The interrupt facilities of the MTV differ from those of the 80C51 as follows:

1. Since there is not a serial port, there are no interrupts nor control bits relating to this interrupt. The interrupts and their vector addresses are as follows:

Event	Program Memory Address
Reset	000
External INT0	003
Timer 0	00B
External INT1	013
Timer 1	01B
VSync Start	023

2. The VSYNC input used by the On Screen Display facility can generate an interrupt. The active polarity of the pulse is programmable, as described in a later section. The interrupt occurs at the leading edge of the pulse.
3. External Interrupt 1 is modified so that an interrupt is generated when the input switches in either direction (on the 8051, there is a programmable choice between interrupt on a negative edge or a low level on INT1). This facility allows for software pulse-width measurement handling of a remote control.
4. The IP register is not used, and the IE register is similar to that on the 80C51:

IE

7	6	5	4	3	2	1	0
EA	–	–	EVS	ET1	EX1	ET0	EX0

Six-Bit PWM DACs

The structure of these modules is shown in Figure 2. First, the basic MCU clock is divided by 4 to get a waveform that clocks a 6-bit counter which is common to all the PWMs, including the 14-bit one. This divided clock is hereafter called the PWM counter clock.

Each PWM block has a special function register PWMn arranged as follows:

PWM0-PWM7

7	6	5	4	3	2	1	0
PWE	–	PV5	PV4	PV3	PV2	PV1	PV0

If the PWE bit for a particular PWM block is 1, the block is active and controls its assigned port pin; if PWE is 0 the corresponding port pin is controlled by the port. The "value" field (PV5 ... PV0) of each PWM register is compared to (the LS 6 bits of) the common counter. When the value matches, the output FF is cleared, so that the output pin is driven low. When the value rolls over to zero, the output FF is set, so that the output pin is released. Thus the output waveform has a fixed period of 64 PWM counter clocks; its duty cycle is determined by PWMn.5:0.

Three of the nine total PWMs operate as described above; for three others, both the rising and falling edges of the output are delayed by one PWM clock; for the remaining three, both edges are delayed by two PWM clocks. This feature reduces the radio-frequency emission that would otherwise occur when the counter rolled over to zero and all nine open-drain outputs were released.

14-Bit PWM DAC (TDAC)

This feature was partially described in the preceding section. As shown in Figure 3, the 6-bit counter used for the lower precision PWMs is in fact the least significant part of a 14-bit counter used for this facility. The nature of the counter is such that it can achieve a stable output value through its MSB, and the value can propagate through logic like that shown in Figure 3, and the logic output can be stable within one period of the PWM counter clock (e.g., 250 ns) if edge-triggered logic is used to capture the logic output, or within one phase of the PWM counter clock (e.g., 125 ns) if a phase of the PWM counter clock is used to capture the logic output. For cost and die-size reasons, it is preferable that the TDAC counter be a ripple counter.

This feature is controlled by two special function registers:

TDACL

7	6	5	4	3	2	1	0
TD7	TD0	TD1	TD2	TD3	TD4	TD5	TD6

TDACH

7	6	5	4	3	2	1	0
TDE	–	TD13	TD12	TD11	TD10	TD9	TD8

When software wishes to change the 14-bit value (TD0 – TD13), it should first write TDACL and then write TDACH. Alternatively, if the required precision of the duty cycle is satisfied by 6 bits or less, software can simply write TDACH. Note from Figure 3 that this block includes an "extra" 14-bit latch between TDACL/H and the comparator and other logic. The programmed value is clocked into the operative latch when the 7 low-order bits of the counter roll over to zero, provided that the software is not in the midst of loading a new 14-bit value (that is, it is not between writing TDACL and writing TDACH).

In a similar fashion to the lower-precision PWMs, this facility has an output FF that is set when the lower 7 bits of the counter overflow/wrap. The *more* significant 7 bits of the operative latch's programmed value are compared for equality against the *less* significant 7 bits of the counter, and the output FF is cleared when they match. Thus this output has a fixed period of 128 PWM counter clocks, and the duty cycle is determined by the programmed value.

For the higher-precision aspect of this feature, the 7 more-significant bits of the counter are used in a logic block with the 7 less-significant bits of the programmed value. The 7th LSB (binary value 64) of the programmed value is ANDed with the 7th MSB (128) of the counter, the 6th LSB of the value is ANDed with the counter's 6th and 7th MSBs being 10, and so on through the LSB

of the programmed value being ANDed with the counter's 7MSBs being 100000. Then these 7 ANDed terms are ORed. If the result is true/1 at the time the 7 LSBs of the counter match the MSBs of the programmed value, the output is forced high for 1 (additional) PWM counter clock.

The result is that, if the value-64 bit of the 14-bit value is programmed to 1, every other cycle of 128 PWM counter clocks has its duty cycle stretched by one counter clock; if the value-32 bit is programmed to 1, every 4th cycle is stretched, and so on through, if the value-1 bit is programmed to 1, one cycle out of each 128 is stretched.

Assuming the external integrator can handle all this, the net effect is a PWM DAC that has the period of a 7-bit design (which makes the integrator easier and more feasible to design) with the accuracy of a 14-bit one. There is some question whether all of the least significant bits can be effectively integrated, or whether they simply act as a source of ripple in the integrated voltage. An obvious prerequisite for such precision is that the load on the voltage must be very light, like a single op amp or comparator.

The TDAC feature differs from the corresponding features of predecessor parts in several ways:

1. The 14-bit value is functionally composed of major and minor portions of 7 bits each.
2. The 14-bit value is programmed as a contiguous multi-register value that can be manipulated straight-forwardly via arithmetic instructions.
3. As discussed for the 6-bit DACs, both of the preceding parts had a feature whereby the PWM output could be inverted, redundantly with complementing the 14-bit value. This feature has been eliminated.

	ADDRESS TYPE				
	DIRECT	BIT	REGISTER	USE	
DATA MEMORY	00-07		R0-R7	On-chip RAM (R0-7 if PSW.4-3 = 00)	
	08-0F		R0-R7	On-chip RAM (R0-7 if PSW.4-3 = 01)	
	10-17		R0-R7	On-chip RAM (R0-7 if PSW.4-3 = 10)	
	18-1F		R0-R7	On-chip RAM (R0-7 if PSW.4-3 = 11)	
	20	07-00		On-chip RAM	
	21-2E	77-08		On-chip RAM	
	2F	7F-78		On-chip RAM	
	30-7F			On-chip RAM	
SPECIAL FUNCTION REGISTERS	80	87-80	P0	Port 0	ON-CHIP RAM IF ACCESSED INDIRECTLY
	81		SP	Stack Pointer	
	82		DPL	Data Pointer LSBYTE	
	83		DPH	Data Pointer MSBYTE	
	87		PCON	Power Control	
	88	8F-88	TCON	Timer Control	
	89		TMOD	Timer Mode	
	8A		TL0	Timer 0 LSBYTE	
	8B		TL1	Timer 1 LSBYTE	
	8C		TH0	Timer 0 MSBYTE	
	8D		TH1	Timer 1 MSBYTE	
	90	97-90	P1	Port 1	
	98	9F-98	OSAT	On Screen Attributes	
	99		OSDT	On Screen Data	
	9A		OSAD	On Screen Address	
	A0	A7-A0	P2	Port 2	
	A8	AF-A8	IE	Interrupt Enable	
	B0	B7-B0	P3	Port 3	
	C0	C7-C0	OSCON	On Screen Display Control	
	C1		OSMOD	On Screen Display Mode	
	C2		OSORG	On Screen Display Origin	
	C3		RAMCHR	For Test Use Only	
	C4		RAMATT	For Test Use Only	
	D0	D7-D0	PSW	Program Status Word	
	D2		TDACL	Hi-Res Pulse Width Modulator	
	D3		TDACH	Hi-Res Pulse Width Modulator	
	D4-D7		PWM0-3	Lo-Res Pulse Width Modulators	
	D8	DF-D8	SAD	D/A and Voltage Comparator	
	DC-DF		PWM4-7	Lo-Res Pulse Width Modulators	
	E0	E7-E0	A	Accumulator	
	F0	F7-F0	B	B Register	

Figure 1. Data Memory and Special Function Registers on the MTV

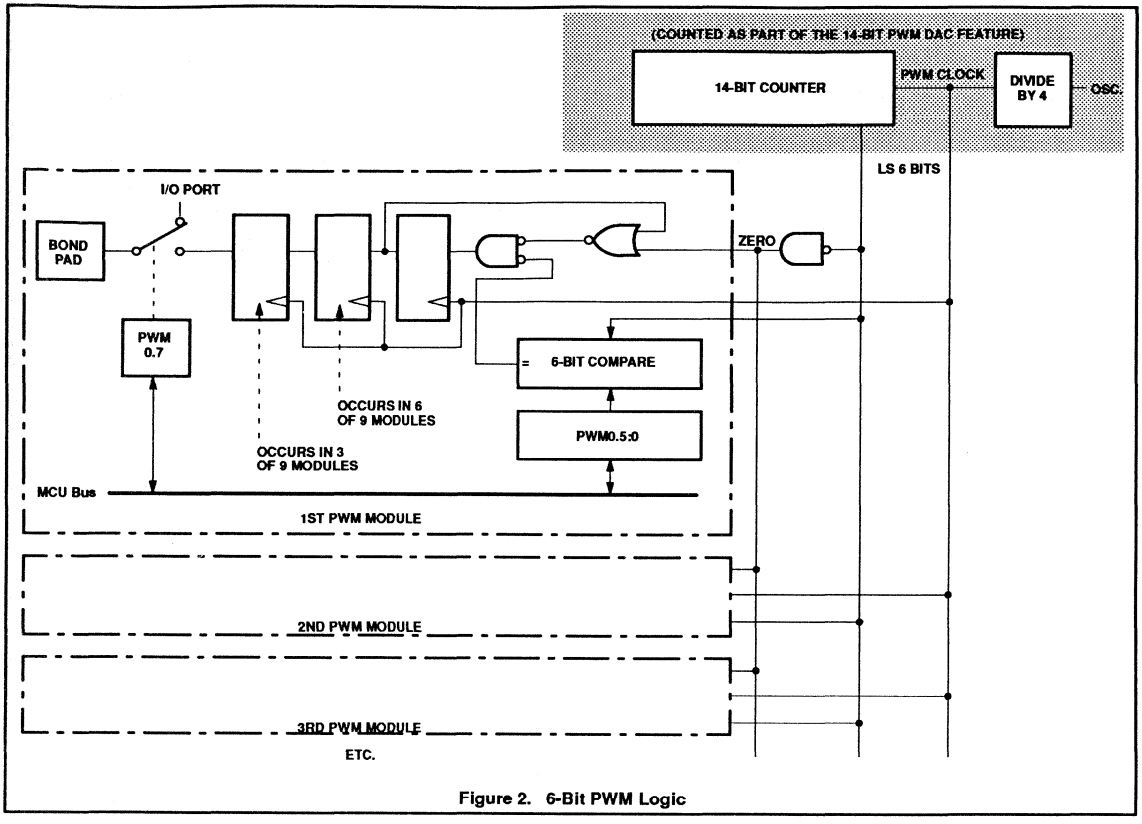


Figure 2. 6-Bit PWM Logic

Software A/D Facility

This facility is shown in Figure 4. It represents an alternate use whereby any of the P1.0 through P1.2 pins can be selected as one input of a linear voltage comparator. The block includes one special function register:

SAD

7	6	5	4	3	2	1	0
VHi	CH1	CH0	St	SAD3	SAD2	SAD1	SAD0

As shown in Figure 4 the other input of the comparator is connected to a 4-bit D/A that is controlled by the 4 LSBs of the SAD register, producing a reference voltage nominally 0.15625V to 4.84375V by steps of 0.3125V. The output of the comparator (high/low) can be read by the program as the MSB of the register, which is bit addressable.

The St bit should be written as 1 in order to initiate a voltage comparison. After writing St=1, the program should include intervening instructions totalling at least six machine cycles (72 CLK periods or 6 microseconds at 12MHz), before the instruction that accesses and tests VHi.

The chan field controls which pin, if any, is connected to this facility:

CH1	CH0	pin
0	0	none
0	1	P1.0
1	0	P1.1
1	1	P1.2

Port 1 has open-drain drivers which will not materially affect an analog voltage as long as any and all pins used for software A/D measurement have corresponding ones in the port register.

On Screen Display (OSD) Module

This block is the largest of the additions that are specific to this product. Its basic function is to superimpose text on the television video image, to indicate various parameters and settings of the receiver or tuner. External circuitry handles the mixing (multiplexing) of the text and the TV video.

The overall OSD block has four input pins: two for a video clock, plus the horizontal and vertical sync signals. The video clock pins are used to connect an LC circuit to an on-chip video oscillator that is independent of the normal MCU clock. The L and C values are chosen so that a video pulse, of a duration equal to the VCLK period, will produce a more-or-less square dot on the screen, that is, a dot having a width approximately equal to the vertical distance between consecutive scan lines.

The video oscillator is stopped (with VCLK2 low) while horizontal sync is asserted, and is released to operate at the trailing edge of horizontal sync. This technique helps provide uniform horizontal positioning of characters/dots from one scan line to the next.

The block has four outputs, three color video signals, and a control signal. Since this block is the major feature of the part, its main inputs and outputs are dedicated pins, without alternate port bits.

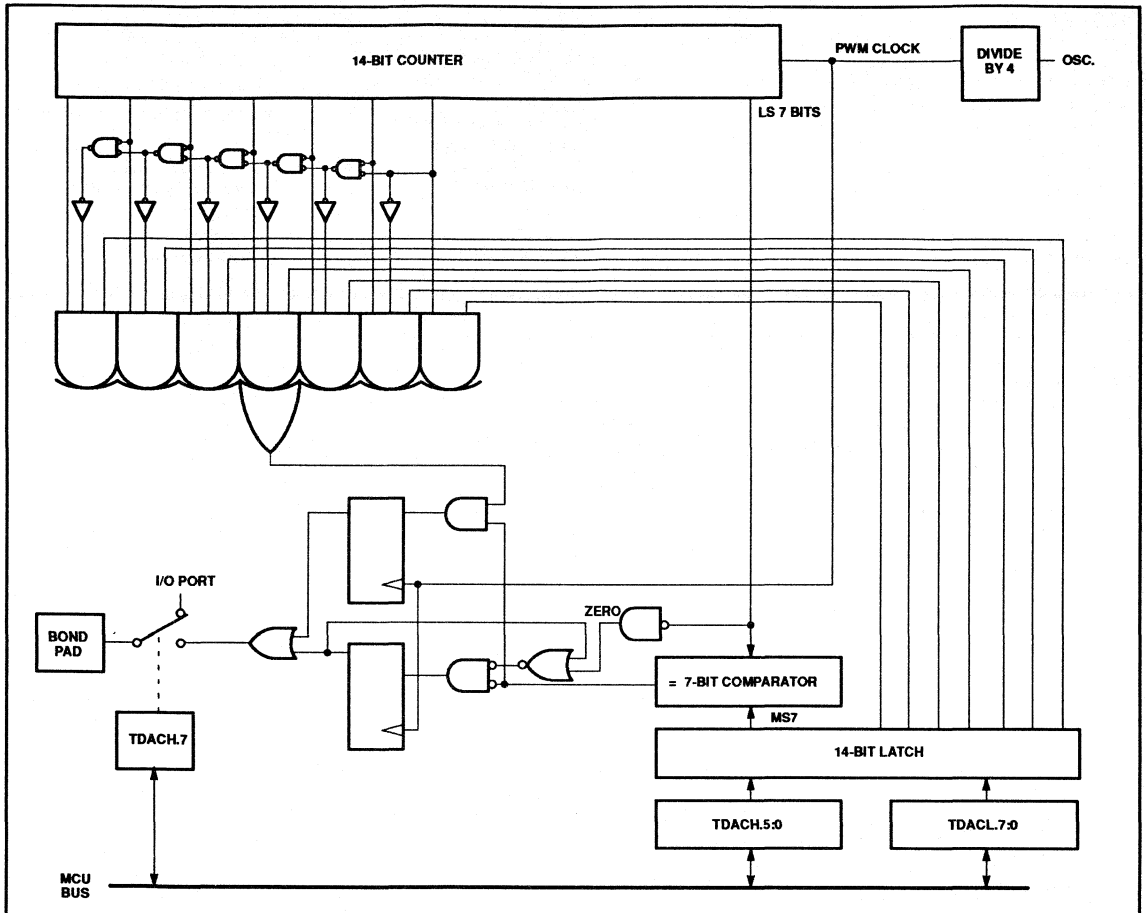


Figure 3. 14-Bit PWM (TDAC) Logic

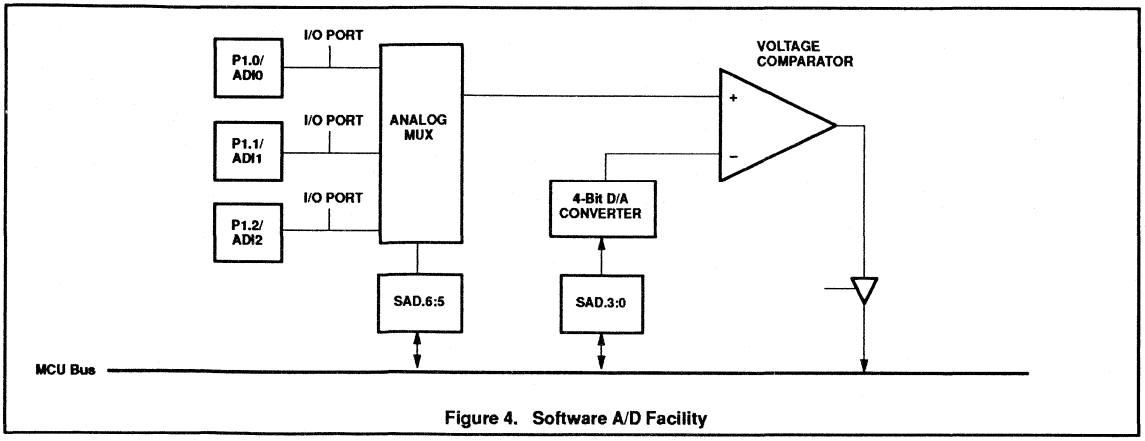


Figure 4. Software A/D Facility

Display RAM

The OSD of the MTV differs from that in preceding devices in one major way: It does not fix the number and size of displayed rows of text. Several predecessor parts allowed two displayed rows of 16 characters each. The MTV simply has 128 locations of display RAM, each of which can contain a displayed character or a New Line character that indicates the end of a row. A variant of the New Line character is used to indicate the end of displayed data.

The three major elements of the OSD facility are shown in the Block Diagram. Each display RAM location includes 6 data bits and 4 attribute bits. The 6 data bits from display RAM, along with a line-within-row count, act as addresses into the character generator ROM, which contains 60 displayable bit maps (64 minus one for each of New Line and three Space characters). Each bit map includes 18 scan lines by 14 dots. The character generator ROM is maskable or programmable along with the program ROM to allow for various character sets and languages.

The programming interface to display RAM is provided by three special function registers:

OSAD

7	6	5	4	3	2	1	0
–	OSAD6	OSAD5	OSAD4	OSAD3	OSAD2	OSAD1	OSAD0

OSDT

7	6	5	4	3	2	1	0
–	–	OSDT5	OSDT4	OSDT3	OSDT2	OSDT1	OSDT0

OSAT (with OSDT = New Line)

7	6	5	4	3	2	1	0
–	–	–	E	–	SR	D	Sh

OSAT (with OSDT = BSpace or SplitBSpace)

7	6	5	4	3	2	1	0
–	–	–	B	–	BC2	BC1	BC0

OSAT (with OSDT = any other)

7	6	5	4	3	2	1	0
–	–	–	B	–	FC2	FC1	FC0

OSAD ("On Screen ADress") contains the address at which data will next be written into display RAM, while the ten active bits in OSDT ("On Screen DaTa") plus OSAT ("On Screen ATtributes") correspond exactly to the 10 bits in each display RAM location. FColor indicates the color of foreground (1) pixels in the ROM bit map for this character, while B indicates whether background (0) pixels should show the current background color (B=1) or television video (B=0). Thus, for the 1 bits in a character's bit map, the VID2:0 pins are driven with (FColor) and VCTRL is driven active, while for 0 bits VID2:0 are driven with the background color (except for shadow bits) and VCTRL is driven with the B bit.

Writing OSAT simply latches the attribute bits into a register, while writing OSDT causes the data bus information, plus the contents of the OSAT register, to be written into display RAM. Thus, for a given display RAM location, OSAT should be written before OSDT. If successive characters are to be written into display RAM with the same attributes, OSAT need not be rewritten for each character, only prior to writing OSDT for the first character with those particular attributes.

In reality, there is a potential conflict between the timing of a write to OSDT and an access to display RAM by the OSD logic for data display. This is resolved by the use of a true dual-ported RAM for display memory.

OSAD is automatically incremented by one after each time OSDT and display RAM are written. Except in special test modes that are beyond the scope of this spec release, display RAM cannot be read by the MCU program.

The OSAT attribute bits associated with the BSpace (data=111110), SplitBSpace (111111), and New Line (111101) characters are interpreted differently from those that accompany other data characters. With BSpace and SplitBSpace, B is interpreted as described above, but the 3 color bits specify the Background color (BColor) for subsequent characters. For BSpace, a change in B and BColor becomes effective at the left edge of the character's bit map. For SplitBSpace, a change in B and BColor occurs halfway through the character horizontally. The normal Space character (111100) has no effect on the BColor value.

BColor values 000 and 111 minimize the occurrence of transient states among the VID2:0 outputs.

The background color defined by the most recently encountered BSpace or SplitBSpace character is maintained on the VID2:0 pins except at the following times:

1. During the active time of HSYNC,
2. During the active time of VSYNC,
3. During those pixels of an active character that correspond to a 1 in the character's bit map,
4. During a "shadow" bit.

The BColor value is not cleared between vertical scans, so that if a single background color is all that is needed in an application, it can be set via a single BSpace character during program initialization, and never changed thereafter. In order for such a BSpace to actually affect the MTV's internal BColor register the Mode field of the OSMOD register must be set to 01 (or higher) so that the OSD hardware is operating.

With a New Line character, if the E bit is 1, no further rows are displayed on the screen. If E is 0 and D is 1, all of the characters in the following row are displayed with Double height and width. If E is 0 and Sh is 1, all of the characters in the following row are displayed with shadowing, as described in a later section. If E is 0 and SR is 1, the next row is a "short row": It is only 4 or 8 scan lines high rather than 18 or 36. Short rows can be used for underlined text.

The latches in which the E, D, Sh, and SR bits are captured are cleared to zero at the start of each vertical scan. This means that if the first text line on the screen is a short row, or if it contains either double size or shadowing, the text must be preceded by a New Line character. Like all such characters, this initial New Line advances the vertical screen position; the VStart value (see below) should take this fact into account.

Other OSD Registers

A number of changes in the OSD architecture have reduced the number of other special function registers involved in the feature, below the number needed with predecessor devices:

1. The elimination of certain options such as 4, 6, or 8X character sizes and alternate use of two of the video outputs.
2. The moving of certain other options from central registers to display RAM, such as foreground color codes and background selection.

OSCON

7	6	5	4	3	2	1	0
IV	Pv	Lv	Ph	Pc	Po	DH	BFe

The IV bit is the interrupt flag for the OSD feature. It is set by the leading edge of the VSYNC pulse, and is cleared by the hardware when the VSYNC interrupt routine is vectored to. It can also be set or cleared by software writing a 1 or 0 to this bit.

NOTE

It is theoretically possible that a VSYNC interrupt could be missed, or an extra one generated, if OSCON is read, then modified internally (e.g., in Ac), and the result written back to OSCON. However, none of the other bits in OSCON are reasonable candidates for dynamic change. Special provisions are included in the MTV logic so that IV will not be changed by a single "read-modify-write" instruction such as SETB or CLR, unless the instruction specifically changes IV.

A 0 (1) in Pv designates that the VSYNC input is high-active (low-active). One effect of this bit is that the VID2:0 and VCTRL outputs are blocked (held at black/inactive) during the active time of VSYNC. The IV bit is set on the leading edge of the VSYNC pulse; thus Pv controls whether the OSD interrupt occurs in response to a high-to-low or low-to-high transition on VSYNC.

A 0 (1) in Lv designates that the leading edge (active level) of VSYNC, as defined by Pv, clears the state counter that is used to determine the vertical start of on-screen data. In effect, Lv=0(1) says that the leading (trailing) edge of VSYNC is the time reference for the video field.

A 0 (1) in Ph designates that the HSYNC input is high-active (low-active).

A 0 (1) in Pc designates that a high (low) on the VCTRL output means "show the color on VID2:0".

A 0 (1) in Po designates that a 0 (1) internal to the MTV corresponds to a low on one of the VID2:0 pins. This control bit is needed only because the Shadowing feature needs to generate black pixels without reference to a register value: Internally, the 3-bit code 000 always designates black.

If DH is 1, character sizes are doubled vertically but not horizontally. This feature allows the MTV to be used in "improved definition" systems that are not interlaced. The vertical doubling imposed by DH does not affect the VStart logic described below: It operates in HSync units regardless of DH or D.

If BFe is 1, the BF output tracks whether each bit in displayed characters is a foreground bit (low) or a background bit (high). If BFe is 0, the BF pin remains high.

OSORG

7	6	5	4	3	2	1	0
HS4	HS3	HS2	HS1	HS0	VS2	VS1	VS0

The HStart field (HS4 – HS0) defines the left end (start) of all of the on-screen character rows, as a multiple of four VCLKs. Active display begins 4(HStart)+1 VCLKs plus one single-sized character width after the trailing edge of HSYNC. Counting variations in Wc, there may be 17 to 143 VCLKs from the end of HSYNC to the start of the first character of each row.

The VStart field (VS2 – VS0) defines the top (start) of the first on-screen character row, as a multiple of four HSYNC pulses. Active display begins 4(VStart)-1 HSYNCs after the field's time reference point, a range of 3 to 31. Subsequent character rows occur directly below the first, such that the last scan line of one row is directly followed by the first scan line of the next row. Successive New Line characters (with or without the Short Row designation) can be used to vertically separate text rows on the screen.

Neither the HStart nor VStart parameter is affected by the D line attribute that is used to display double-sized characters.

OSMOD

7	6	5	4	3	2	1	0
Wc	–	Mode1	Mode0	–	SHM2	SHM1	SHM0

If the mode bits (Mode 1, Mode 0) are 00, the OSD feature is disabled. The VCLK oscillator is disabled, VID2:0 are set to black, and VCTRL is held inactive.This is the mode to which the MTV OSD logic is reset. A direct transition from this mode to active display (1x) would result in undefined operation and visual effects for the duration of the current video field (until the next VSYNC).

If the mode is 01, the VCLK oscillator is enabled and the OSD logic operates normally internally, but VID2:0 are set to black and VCTRL is held inactive. The OSD feature can be toggled between this state and 1x as desired to achieve real-time special effects such as "vertical wiping."

Mode 10 represents normal OSD operation. Active characters can be shown against TV video (for characters with B=0) or (for characters with B=1) against a background of the color defined as an attribute of BSpace and SplitBSpace characters.

In mode 11, characters can be displayed but all of the receiver's normal video is inhibited by holding VCTRL asserted throughout the active portion of each scan line. Since VID2:0 are driven with the current background color during this time, except during the foreground portion of displayed characters, this produces text against a solid background. This mode is useful for extensive displays that require user concentration.

If Wc is 1, then each displayed character is horizontally terminated after 12 bits have been output, as opposed to after 14 bits if Wc is 0. This allows text to be "packed" more tightly so that more characters can be displayed per line. In effect, the 2 bits out of the display ROM, which would otherwise be the rightmost 2 of the 14, are ignored when Wc is 1. Clearly, if this feature is to be used, it must be accounted for in the design of the bit maps in the display ROM.

The 3-bit ShMode field (SHM2 – SHM0) determines how characters are shadowed in rows for which the SH row attribute is 1. As shown in Figure 5, the values 000-110 indicate an apparent light source position ranging from the lower left clockwise to the lower right, while the value 111 indicates full-surround shadowing.

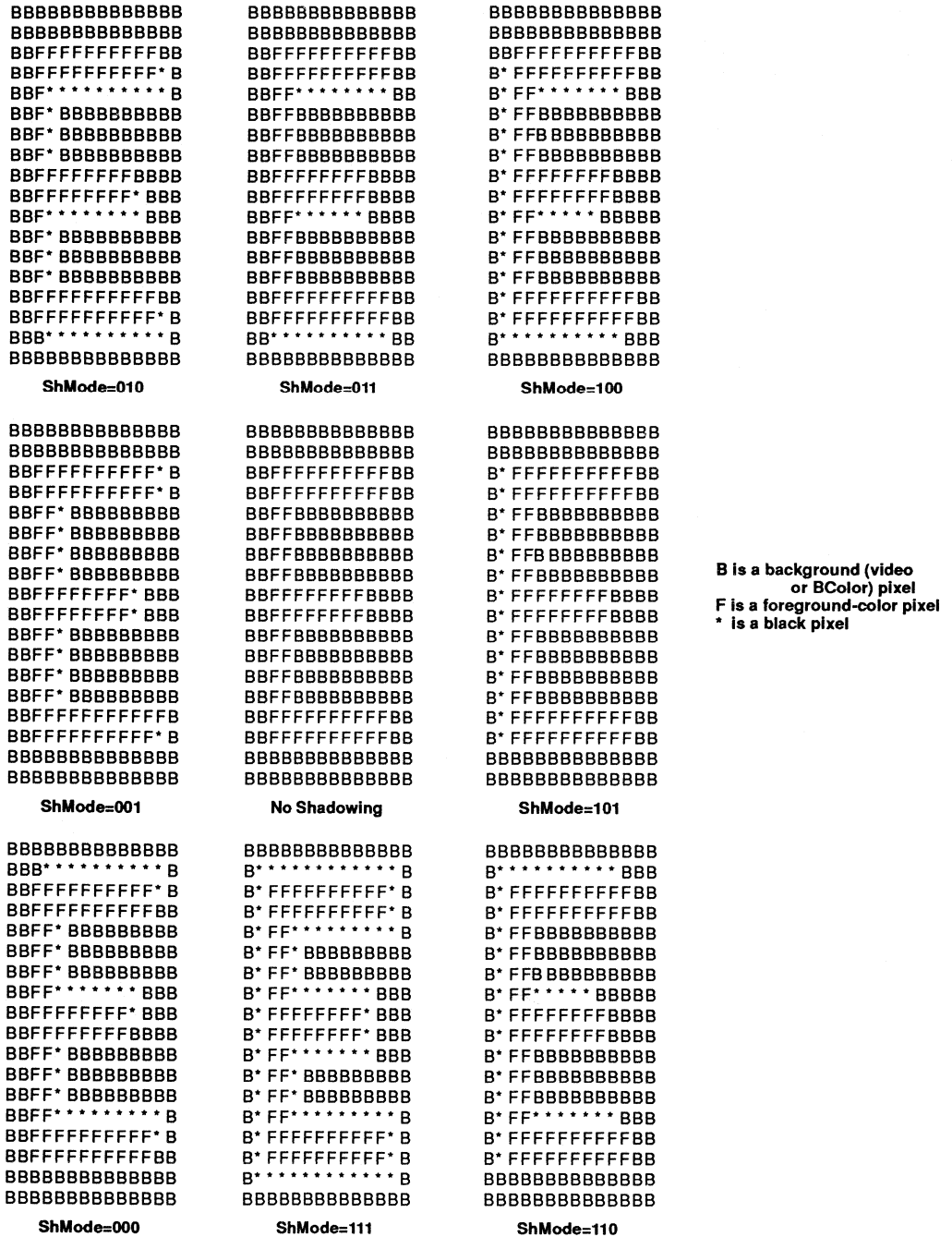


Figure 5. Effect of Shadowing on the Letter "E"

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT	NOTES
			MIN	MAX		
V_{IL}	Input low voltage		–0.5	$0.2V_{CC}$–0.1	V	
V_{IL1}	Input low voltage (VSYNC)	Neg. HSYNC polarity (OSPH = 1)	–0.5	$0.16 \times V_{CC}$	V	5
		Pos. HSYNC polarity (OSPH = 0)	–0.5	$0.20 \times V_{CC}$	V	5
V_{IH1}	Input high voltage (P1.2:0, P2.7:0, P3.6:5, P3.3:1, VSYNC, HSYNC)		$0.2V_{CC}$+0.9	V_{CC}+0.5	V	
V_{IH2}	Input high voltage (port 0, P1.3, P3.7, P3.4, P3.0)	I_{IH} = 2mA	$0.2V_{CC}$+0.9	12.6	V	
V_{IH3}	Input high voltage (VSYNC)		$0.6 \times V_{CC}$	V_{CC} + 0.5V	V	
$V_{IH} - V_{CC}$	Input high voltage (port 0, P1.3, P3.7, P3.4, P3.0) with respect to V_{CC}			8	V	1
I_{IN}	Input current (VSYNC)	Neg. HSYNC polarity (OSPH = 1)	–80	+120	µA	5
		Pos. HSYNC polarity (OSPH = 0)	0	+10	µA	5
V_{IH}	Input high voltage (XTAL1, VCLK1, RST)		$0.7V_{CC}$ o	V_{CC}+0.5	V	
V_{OL1}	Output low voltage (P2.3:0, P3.6:5)	I_{OL} = 10mA		0.5	V	
V_{OL2}	Output low voltage (TDAC, PWM0:7)	I_{OL} = 700µA		0.5	V	2
V_{OL3}	Output low voltage (all other outputs)	I_{OL} = 1.6mA		0.45	V	
V_{OH}	Output high voltage (port 1, VID2:0, VCTRL, BF)	I_{OH} = –60µA	2.4		V	
R_{RST}	Reset pulldown resistor		50	300	kΩ	
C_{IO}	Pin capacitance	Test freq = 1MHz, T_{amb} = 25°C		10	pF	
I_{PD}	Power-down current	V_{CC} = 2 to 6V		5	mA	
I_{CC}	Normal mode supply current	V_{CC} = 5.5V		30	mA	3
HYS	Hysteresis (VSYNC)	Either HSYNC polarity	0.445		V	

NOTES:

1. This maximum applies at all times, including during power switching, and must be accounted for in power supply design. During a power-on process, the +12 volt source used for external pullup resistors should not precede the V_{CC} of the MTV up their respective voltage ramps by more than this margin, nor, during a power-down process, should V_{CC} precede +12V down their respective voltage ramps by more than this margin.
2. The specified current rating applies when any of these pins is used as a Pulse Width modulated output. For use as a port output, the rating is as given subsequently.
3. I_{CC} measured with OSD block initialized and Reset remaining low.
4. The capacitance of pins P0.0 and P0.7 for the 87C054 exceeds 10pF. P0.0 is 40pF maximum, while P0.7 is 20pF maximum.
5. Input current for negative HSYNC polarity is a switching current. This current may alternate between positive current (into the pin) and negative (out of the pin) during the same HSYNC transition.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C

SYMBOL	PARAMETER	TENTATIVE LIMITS		UNIT	NOTES
		MIN	MAX		
$1/t_{CLCL}$	XTAL Frequency	6	12	MHz	1
t_{CHCX}	XTAL1 Clock high time	20		ns	2
t_{CLCX}	XTAL1 Clock low time	20		ns	2
t_{CLCH}	XTAL1 Clock rise time		20	ns	2
t_{CLCL}	XTAL1 Clock fall time	5	20	ns	2
$1/t_{VCLCL}$	VCLK Frequency	5	8	MHz	
$\lvert t_{VCOH}-t_{VCOL} \rvert$	Rise vs. fall time skew on any one of VID2:0, VCTRL, BF		40	ns	3
$\lvert t_{VCOH1}-t_{VCOH2} \rvert$	Rise time skew between any two of VID2:0, VCTRL, BF		30	ns	3
$\lvert t_{VCOL1}-t_{VCOL2} \rvert$	Fall time skew between any two of VID2:0, VCTRL, BF		30	ns	3

NOTES:
1. The MTV is tested at its maximum XTAL frequency, but not at any other (lower) rate.
2. These parameters apply only when an external clock signal is used.
3. These parameters assume equal loading at C_L = 100pF, for all the referenced outputs. These parameters are specified but not tested.

PROGRAMMING CONSIDERATIONS

EPROM Characteristics

The 87C054 is programmed by using a modified Quick-Pulse Programming algorithm similar to that used for devices such as the 87C51. It differs from these devices in that a serial data stream is used to place the 87C751 in the programming mode.

Figure 6 shows a block diagram of the programming configuration for the 87C054. Port pin P0.0 is used as the programming voltage supply input (V_{PP} signal). Port pin P0.1 is used as the program (PGM/) signal. This pin is used for the 25 programming pulses.

Port 2 is used as the address input for the byte to be programmed and accepts both the high and low components of the eleven bit address. Multiplexing of these address components is performed using the ASEL input. The user should drive the ASEL input high and then drive port 2 with the high order bits of the address. ASEL should remain high for at least 13 clock cycles. ASEL may then be driven low which latches the high order bits of the address internally. The high address should remain on port 2 for at least two clock cycles after ASEL is driven low. Port 2 may then be driven with the low byte of the address. The low address will be internally stable 13 clock cycles later. The address will remain stable provided that the low byte placed on port 2 is held stable and ASEL is kept low. **Note:** ASEL needs to be pulsed high only to change the high byte of the address.

Port 3 is used as a bidirectional data bus during programming and verify operations. During programming mode, it accepts the byte to be programmed. During verify mode, it provides the contents of the EPROM location specified by the address which has been supplied to Port 2.

The XTAL1 pin is the oscillator input and receives the master system clock. This clock should be between 1.2 and 6MHz.

The RESET pin is used to accept the serial data stream that places the 87C054 into various programming modes. This pattern consists of a 10-bit code with the LSB sent first. Each bit is synchronized to the clock input, X1.

Programming Operation

Figures 7 and 8 show the timing diagrams for the program/verify cycle. RESET should initially be held high for at least two machine cycles. P0.1 (PGM/) and P0.0 (V_{PP}) will be at V_{OH} as a result of the RESET operation. At this point, these pins function as normal quasi-bidirectional I/O ports and the programming equipment may pull these lines low. However, prior to sending the 10-bit code on the RESET pin, the programming equipment should drive these pins high (V_{IH}). The RESET pin may now be used as the serial data input for the data stream which places the 87C054 in the programming mode. Data bits are sampled during the clock high time and thus should only change during the time that the clock is low. Following transmission of the last data bit, the RESET pin should be held low.

Next the address information for the location to be programmed is placed on port 2 and ASEL is used to perform the address multiplexing, as previously described. At this time, port 1 functions as an output.

A high voltage V_{PP} level is then applied to the V_{PP} input (P0.0). (This sets Port 1 as an input port). The data to be programmed into the EPROM array is then placed on Port 3. This is followed by a series of programming pulses applied to the PGM/ pin (P0.1). These pulses are created by driving P0.1 low and then high. This pulse is repeated until a total of 25 programming pulses have occurred. At the conclusion of the last pulse, the PGM/ signal should remain high.

The V_{PP} signal may now be driven to the V_{OH} level, placing the 87C054 in the verify mode. (Port 3 is now used as an output port). After four machine cycles (48 clock periods), the contents of the addressed location in the EPROM array will appear on Port 3.

The next programming cycle may now be initiated by placing the address information at the inputs of the multiplexed buffers, driving the V_{PP} pin to the V_{PP} voltage level, providing the byte to be programmed to Port 3 and issuing the 26 programming pulses on the PGM/ pin, bringing V_{PP} back down to the V_{OH} level and verifying the byte. (See Table 3.)

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Flourless part number 2345–5 or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-s/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000µW/cm^2 rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

Table 3. Implementing Program/Verify Modes

OPERATION	SERIAL CODE	P0.1 (PGM/)	P0.0 (V_{PP})
Program user EPROM	286H	–*	V_{PP}
Verify user EPROM	286H	V_{IH}	V_{IH}

NOTE:
* Pulsed from V_{IH} to V_{IL} and returned to V_{IH}.

EPROM PROGRAMMING AND VERIFICATION

T_{amb} = 21°C to +27°C, V_{CC} = 5V ±10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	MAX	UNIT
$1/t_{CLCL}$	Oscillator/clock frequency	1.2	6	MHz
t_{AVGL}*	Address setup to P0.1 (PROG–) low	10µs + 24t_{CLCL}		
t_{GHAX}	Address hold after P0.1 (PROG–) high	48t_{CLCL}		
t_{DVGL}	Data setup to P0.1 (PROG–) low	38t_{CLCL}		
t_{DVGL}	Data setup to P0.1 (PROG–) low	38t_{CLCL}		
t_{GHDX}	Data hold after P0.1 (PROG–) high	36t_{CLCL}		
t_{SHGL}	V_{PP} setup to P0.1 (PROG–) low	10		µs
t_{GHSL}	V_{PP} hold after P0.1 (PROG–)	10		µs
t_{GLGH}	P0.1 (PROG–) width	90	110	µs
t_{AVQV}**	V_{PP} low (V_{CC}) to data valid		48t_{CLCL}	
t_{GHGL}	P0.1 (PROG–) high to P0.1 (PROG–) low	10		µs
t_{SYNL}	P0.0 (sync pulse) low	4t_{CLCL}		
t_{SYNH}	P0.0 (sync pulse) high	8t_{CLCL}		
t_{MASEL}	ASEL high time	13t_{CLCL}		
t_{MAHLD}	Address hold time	2t_{CLCL}		
t_{HASET}	Address setup to ASEL	13t_{CLCL}		
t_{ADSTA}	Low address to address stable	13t_{CLCL}		

NOTES:
* Address should be valid at least 24t_{CLCL} before the rising edge of P0.0 (V_{PP}).
** For a pure verify mode, i.e., no program mode in between, t_{AVQV} is 14t_{CLCL} maximum.

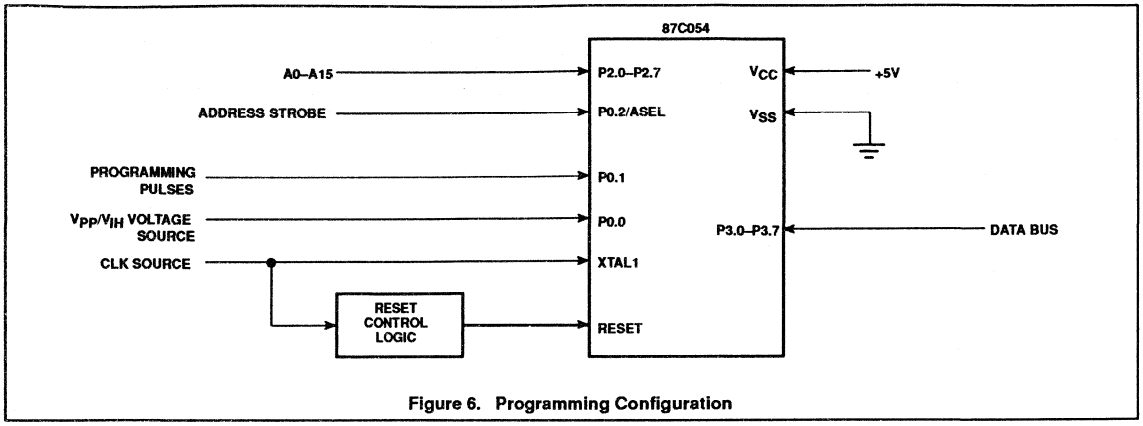


Figure 6. Programming Configuration

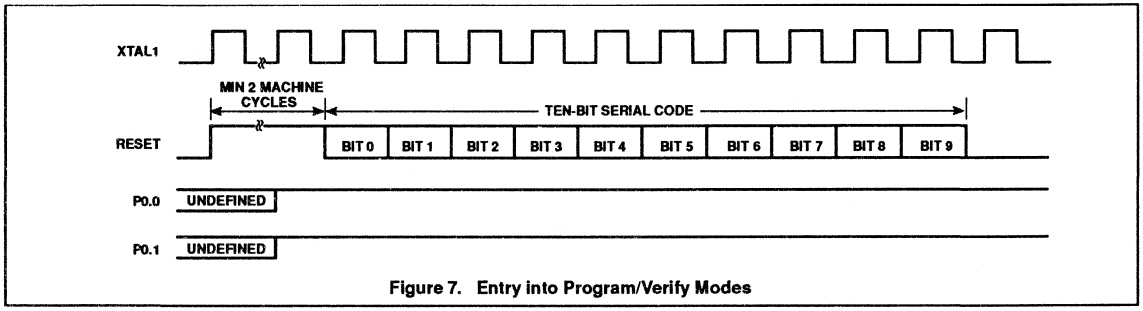


Figure 7. Entry into Program/Verify Modes

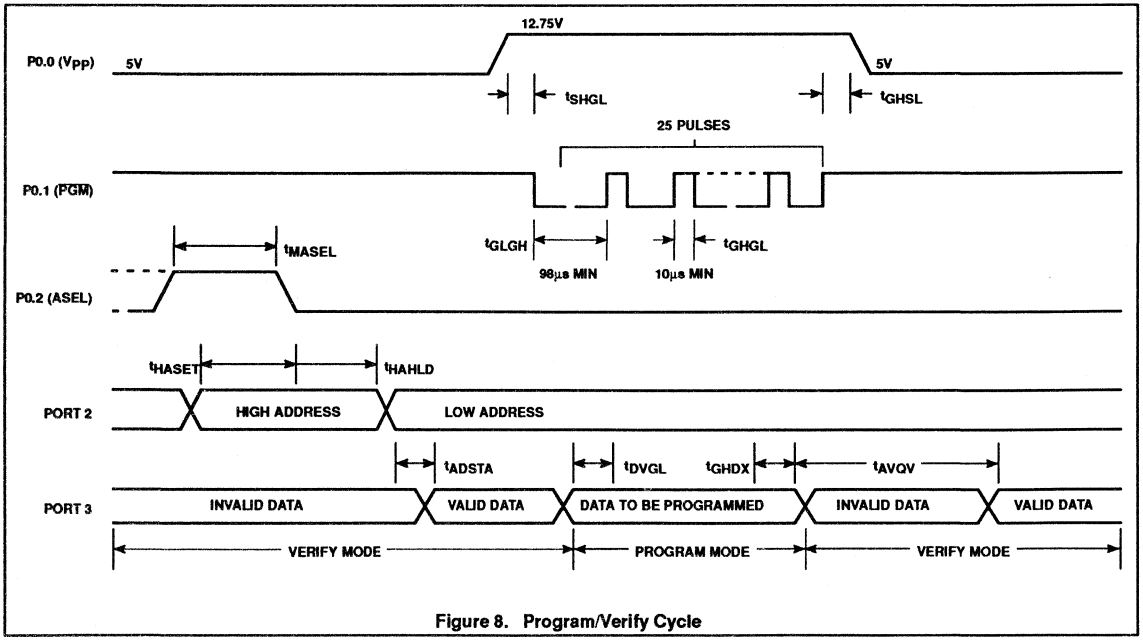


Figure 8. Program/Verify Cycle

8-bit microcontrollers with OSD and VST

84C44X; 84C64X; 84C84X

CONTENTS

1. FEATURES

1.1 84CXXX kernel

- 8-bit CPU, ROM, RAM, I/O in a single 42-lead shrink DIL package
- Over 80 instructions all of 1 or 2 cycles
- 29 quasi bidirectional standard I/O port lines
- Configuration of I/O lines individually selected by mask
- External interrupt T0/INTN
- 2 direct testable inputs T0, T1
- 8-bit programmable timer/event counter
- 3 single level vectored interrupts (external, timer/counter, I²C)
- Power-on-reset and low voltage detector
- Single power supply
- 2 power reduction modes: Idle and Stop
- Operating temperature range: –20 to +70 °C.
- Silicon gate CMOS fabrication process

1.2 Derivative features PCA84C640

- 6K bytes ROM
- 128 bytes RAM
- Multi-master I²C bus interface
- One 14-bit PWM output for VST
- AFC input (with 3-bit DAC and comparator)
- Five 6-bit PWM outputs for analog controls
- Eight port lines with 10 mA LED drive capability
- On screen display 2 rows of 16 characters
- OSD character set of 64 types
- Four programmable display dot sizes
- Seven colours for each character
- Half dot character rounding
- Programmable VSYNCN input polarity
- Programmable HSYNCN input polarity
- LC oscillator for on screen display function with the 84C441, 84C444, 84C641, 84C644, 84C841 and 84C844.
- RC oscillator for on screen display function with the 84C440, 84C443, 84C640, 84C643, 84C840 and 84C843.

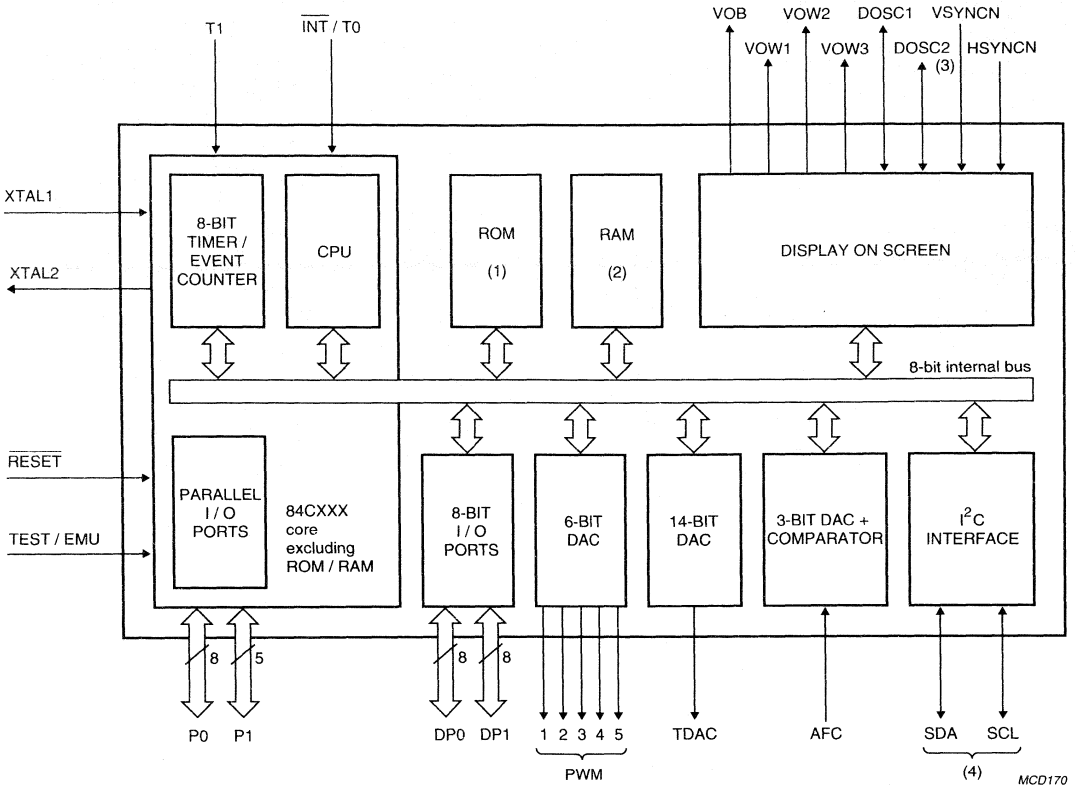
2. GENERAL DESCRIPTION

The 84C440, 84C441, 84C443, 84C444, 84C640, 84C641, 84C643, 84C644, 84C840, 84C841, 84C843 and 84C844 are 8-bit microcontrollers with On Screen Display (OSD) and Voltage Synthesized Tuning (VST) functions. All are members of the 84CXXX microcontroller family. Although the 84C640 is specifically referred to throughout this data sheet, the information applies to all the devices. The small differences between the 84C640 and the other devices are specified in the text and also highlighted in Section 12.

The 84C640 comprises the 84CXXX processor core, 6K bytes mask-programmable program ROM, 128 bytes RAM, a multi-master I²C bus interface, 2 direct testable lines, 18 general purpose bi-directional I/O lines plus 11 function-combined I/O lines, one 14-bit and five 6-bit PWM analog control outputs; AFC input for Voltage Synthesized Tuning and an On Screen Display facility for two rows of 16-characters.

Important

This data sheet details the specific properties of the 84C440, 84C441, 84C443, 84C444, 84C640, 84C641, 84C643, 84C644, 84C840, 84C841, 84C843, and 84C844. The shared characteristics of the 84CXXX family of microcontrollers are described in the 84CXXX family specification, which should be read in conjunction with this data sheet.



(1) 4 Kbytes for the 84C440, 84C441, 84C443 and 84C444. 6 Kbytes for the 84C640, 84C641, 84C643 and 84C644. 8 Kbytes for the 84C840, 84C841, 84C843 and 84C844.

(2) 128 bytes for the 84C440, 84C441, 84C443, 84C444, 84C640, 84C641, 84C643 and 84C644. 192 bytes for the 84C840, 84C841, 84C843 and 84C844.

(3) For use with an LC oscillator; only available with the 84C441, 84C444, 84C641, 84C644, 84C841 and 84C844.

(4) I²C-bus interface not available with the 84C443, 84C444, 84C643, 84C644, 84C843 and 84C844.

Fig.1 Block diagram.

3. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE				TEMPERATURE RANGE (°C)
	PINS	PIN POSITION	MATERIAL	CODE	
PCA84C440	42	SDIL	plastic	SOT270	−20 to + 70
PCA84C441	42	SDIL	plastic	SOT270	−20 to + 70
PCA84C443	42	SDIL	plastic	SOT270	−20 to + 70
PCA84C444	42	SDIL	plastic	SOT270	−20 to + 70
PCA84C640	42	SDIL	plastic	SOT270	−20 to + 70
PCA84C641	42	SDIL	plastic	SOT270	−20 to + 70
PCA84C643	42	SDIL	plastic	SOT270	−20 to + 70
PCA84C644	42	SDIL	plastic	SOT270	−20 to + 70
PCA84C840	42	SDIL	plastic	SOT270	−20 to + 70
PCA84C841	42	SDIL	plastic	SOT270	−20 to + 70
PCA84C843	42	SDIL	plastic	SOT270	−20 to + 70
PCA84C844	42	SDIL	plastic	SOT270	−20 to + 70

Note

A 48-lead QFP package will be available shortly.

4. PINNING INFORMATION

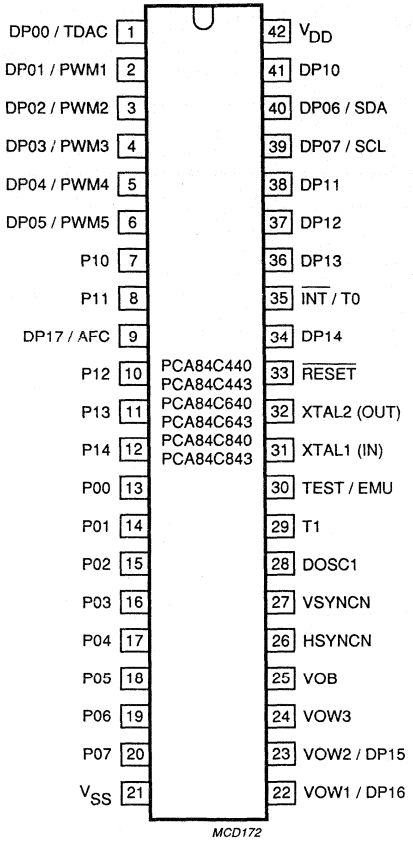


Fig.2 Pinning diagram; 84C440; 84C443; 84C640, 84C643, 84C840 and 84C843

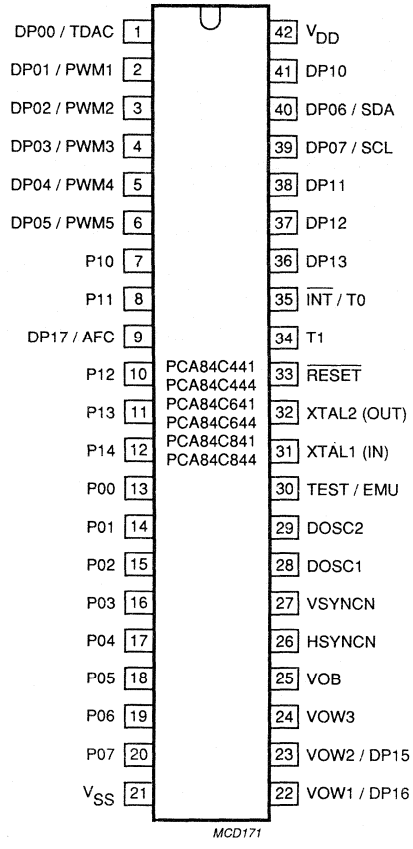


Fig.3 Pinning diagram; 84C441; 84C444; 84C641, 84C644, 84C841 and 84C844

Table 1 Pin description - 84C440; 84C443; 84C640, 84C643, 84C840 and 84C843

SYMBOL	PIN	DESCRIPTION
DP0.0/TDAC	1	Derivative Port 0 : quasi-bidirectional I/O line or 14-bit DAC PWM
DP0.1 to DP0.5/ PWM1 to PWM5	2 to 6	Derivative Port 1 : quasi-bidirectional I/O lines or 6-bit DAC PWM
P1.0 to P1.4	7, 8, 10 to 12	Port 1: quasi-bidirectional I/O lines
P0.0 to P0.7	13 to 20	Port 0: quasi-bidirectional I/O port
DP1.7/AFC	9	Derivative Port 1 : quasi-bidirectional I/O line or comparator input with 3-bit DAC
DP0.6/SDA	40	Derivative open drain I/O port or I^2C-bus data line
DP0.7/SCL	39	Derivative open drain I/O port or I^2C- bus clock line
$\overline{INT}$/T0	35	External interrupt or direct testable line
DP1.0 to DP1.4	41, 38, 37, 36, 34	Derivative Port 1: quasi-bidirectional I/O lines
DP1.5 to DP1.6/ VOW2 to VOW1	23, 22	Derivative Port 1 : quasi-bidirectional I/O lines or character video output
$\overline{RESET}$	33	Initialize input, active low
XTAL2, XTAL1	32, 31	Oscillator output or input terminal for system clock
TEST/EMU	30	Control input for testing and emulation mode. Ground for normal operation.
T1	29	Direct testable pin and event counter input
DOSC1	28	Connection to RC oscillator of OSD clock
VSYNCN	27	Vertical synchronous signal input
HSYNCN	26	Horizontal synchronous signal input
VOB	25	Blanking output
VOW3	24	Character video output of OSD
V_{SS}	21	Ground terminal
V_{DD}	42	Power supply terminal

Table 2 Pin description - 84C441; 84C444; 84C641, 84C644, 84C841 and 84C844

SYMBOL	PIN	DESCRIPTION
DP0.0/TDAC	1	Derivative Port 0 : quasi-bidirectional I/O line or 14-bit DAC PWM
DP0.1 to DP0.5/ PWM1 to PWM5	2 to 6	Derivative Port 1 : quasi-bidirectional I/O lines or 6-bit DAC PWM
P1.0 to P1.4	7, 8, 10 to 12	Port 1: quasi-bidirectional I/O lines
P0.0 to P0.7	13 to 20	Port 0: quasi-bidirectional I/O port
DP1.7/AFC	9	Derivative Port 1 : quasi-bidirectional I/O line or comparator input with 3-bit DAC
DP0.6/SDA	40	Derivative open drain I/O port or I²C-bus data line
DP0.7/SCL	39	Derivative open drain I/O port or I²C-bus clock line
$\overline{INT}$/T0	35	External interrupt or direct testable line
DP1.0 to DP1.3	41, 38, 37, 36	Derivative Port 1: quasi-bidirectional I/O lines
DP1.5 to DP1.6/ VOW2 to VOW1	23, 22	Derivative Port 1 : quasi-bidirectional I/O lines or character video output
$\overline{RESET}$	33	Initialize input, active low
XTAL2, XTAL1	32, 31	Oscillator output/input terminals for system clock
TEST/EMU	30	Control input for testing and emulation mode. Ground for normal operation.
T1	34	Direct testable pin and event counter input
DOSC1/DOSC2	28, 29	Connections to LC oscillator of OSD clock
VSYNCN	27	Vertical synchronous signal input
HSYNCN	26	Horizontal synchronous signal input
VOB	25	Blanking output
VOW3	24	Character video output of OSD
V_{SS}	21	Ground terminal
V_{DD}	42	Power supply terminal

5. RESET

The $\overline{\text{RESET}}$ pin is used as an active low input to initialize the microcontroller to a defined state. The Reset configuration is shown in Fig.5.

The Power-on-reset circuit monitors the voltage level of V_{DD}. If V_{DD} remains below the internal reference voltage level V_{ref} (typically 3.6 V), the oscillator is inhibited. When V_{DD} rises above V_{ref}, the oscillator is released and the internal reset is active for a period of t_d (typically 50 µs).

Three modes of Power-on-reset are possible:

1. An external $\overline{\text{RESET}}$ signal is applied during power-on.
2. If V_{DD} rises above the minimum operation voltage before time period t_d is exceeded, no external components are necessary, (See Fig 6).
3. External components are required if V_{DD} has a slow rise time, such that after the time period ($t_{Vref} + t_d$) has elapsed the supply voltage is still below the minimum operation voltage (V_{min}). See Figs 7 and 4. In order to ensure a correct reset operation the time constant RC must be $\geq 8t_{VDD}$.

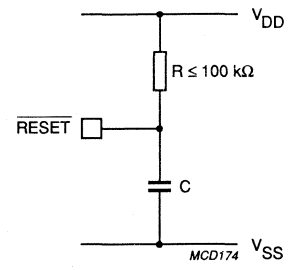


Fig.4 External components for $\overline{\text{RESET}}$ pin.

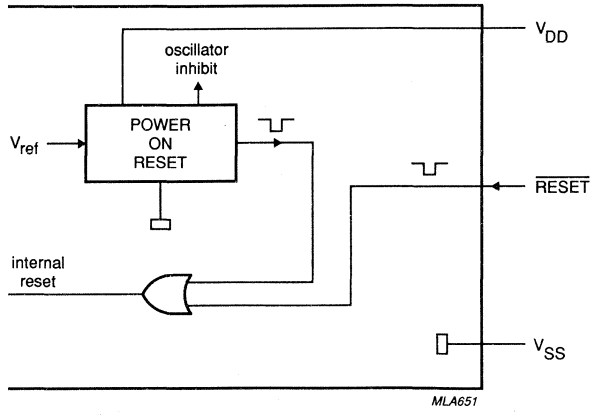


Fig.5 Reset configuration.

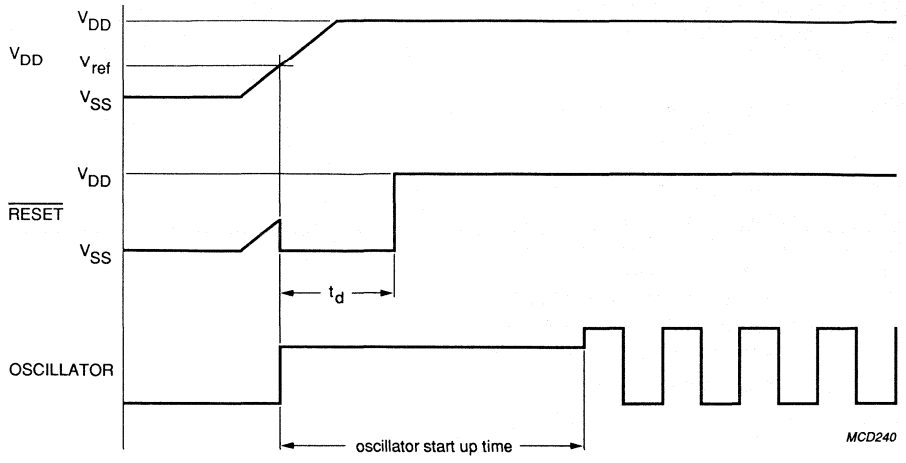


Fig.6 Reset with fast rising V_{DD}.

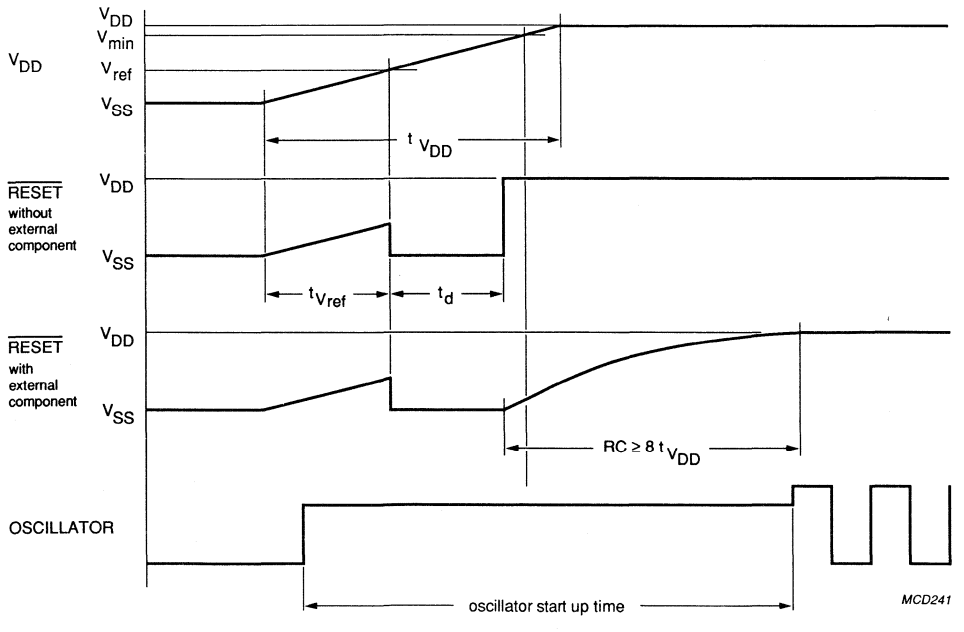


Fig.7 Reset with slow rising V_{DD}.

6. ANALOG CONTROL; 6-BIT PWM DACs

Five PWM outputs are available for analog control purposes e.g. volume, balance, brightness, saturation etc. The block diagram of a typical 6-bit PWM DAC is shown in Fig.8. Each PWM output can generate pulses of programmable length that have a repetition frequency of $f_{PWM}/64$, (where $f_{PWM} = f_{XTAL}/3$). The polarity of all five PWM outputs is selected by the state of the polarity control bit (P6LVL). Setting P6LVL to a logic 1 inverts all five PWM outputs. If the state of P6LVL is a logic 0, then the PWM outputs are not inverted. The PWM outputs PWM1 to PWM5, share the same pins as the Derivative Port lines DP0.1 to DP0.5. The PWM output function, for individual pins, is selected by setting the relevant PWM enable bit (PWMxE) to '1'. The Derivative Port function is selected by setting the relevant PWMxE bit to '0'.

A DC voltage proportional to the PWM control setting may be obtained by connecting an integrating network to each of the PWM outputs (see Fig.9). The analog value is calculated by multiplying the ratio of the high time and the repetition time of the pulse, by V_O.

The high time of any PWM output is: $t_{HIGH} = t_0 \times PWMDL$.

where: $t_0 = 3/f_{XTAL}$ and PWMDL is the decimal value of the contents of the PWM data latch.

The repetition time of any PWM output is: $t_R = t_0 \times 64$

Therefore, the analog output voltage is:
$V_A = (PWMDL/64) \times V_0$

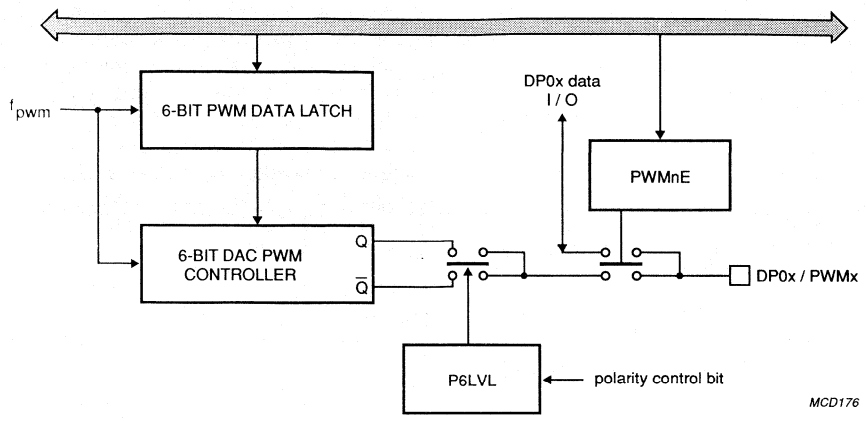


Fig.8 Block diagram; 6-bit PWM DAC.

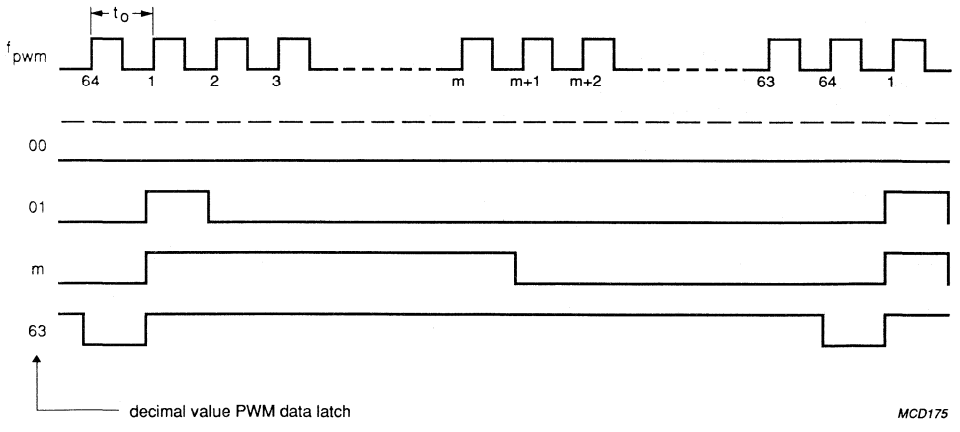


Fig.9 PWM output patterns (P6LVL = 0).

7. VST CONTROL; 14-BIT PWM DAC

The PCA84C640 has one 14-bit PWM DAC output with a resolution of 16384 levels for Voltage Synthesized Tuning. The PWM DAC is shown in Fig. 10 and consists of the following:

- two 7-bit DAC interface latches
- one 14-bit DAC data latch
- 14-bit counter
- pulse control

The 14-bit counter is continuously running and is clocked by f_0. The period (t_0) of the clock is $3/f_{XTAL}$.

The repetition time for one complete cycle of the 14-bit counter is: $t_r = t_0 \times 16384$.

The repetition time for one cycle of the lower 7-bits of the counter is: $t_{sub} = t_0 \times 128$.

Therefore, the number of t_{sub} periods in a complete cycle t_r is: $N = t_0 \times 16384/t_0 \times 128 = 128$

In order to ensure correct operation, data latch VSTH is loaded first and then data latch VSTL. The contents of VSTH are used for coarse adjustment; the contents of VSTL for fine adjustment. At the beginning of the first t_{sub} period following the loading of VSTL, both data latches are downloaded into data latch VSTREG. After the contents of VSTH and VSTL are latched into VSTREG one t_{sub} period is needed to generate the appropriate pulse pattern. To ensure correct DAC conversion two t_{sub} periods should be allowed before beginning the next sequence.

7.1 Coarse adjustment

The coarse adjustment output (OUT1) is reset LOW (inactive) at the start of each t_{sub} period. It will remain LOW until the time t_0 x (VSTH + 1) has elapsed and then will go HIGH and remain so until the next t_{sub} period starts.

7.2 Fine adjustment

Fine adjustment is achieved by generating additional pulses at the start of particular sub-periods. These pulses have a width of t_0. The subperiod in which a pulse is added is determined by the contents of VSTL data latch. Table 3 gives the subperiod numbers at the start of which an additional pulse is generated, depending on the bit in VSTL being '0'. When more than one bit is '0' a combination of additional pulses are generated. For example if VSTL = 1111010 additional pulses will be given in subperiods 16, 48, 64, 80 and 112; this is illustrated in Fig.12.

If VSTH = 0011101, VSTL = 1111010 and P14LVL = 0, then the TDAC output is as shown in Fig. 13.

Table 3 Additional pulse distribution

LOWER 7 BITS (VSTL)	ADDITIONAL PULSE IN SUBPERIODS t_{SUBN}
111 1110	64
111 1101	32, 96
111 1011	16, 48, 80, 112
111 0111	8, 24, 40, 56, 72, 88, 104, 120
110 1111	4, 12, 20, 28, 36, 44, 52, 60 .... 116, 124
101 1111	2, 6, 10, 14, 18, 22, 26, 30, ... 122, 126
011 1111	1, 3, 5, 7, 9, 11, 13, 15, 17, ... 125, 127

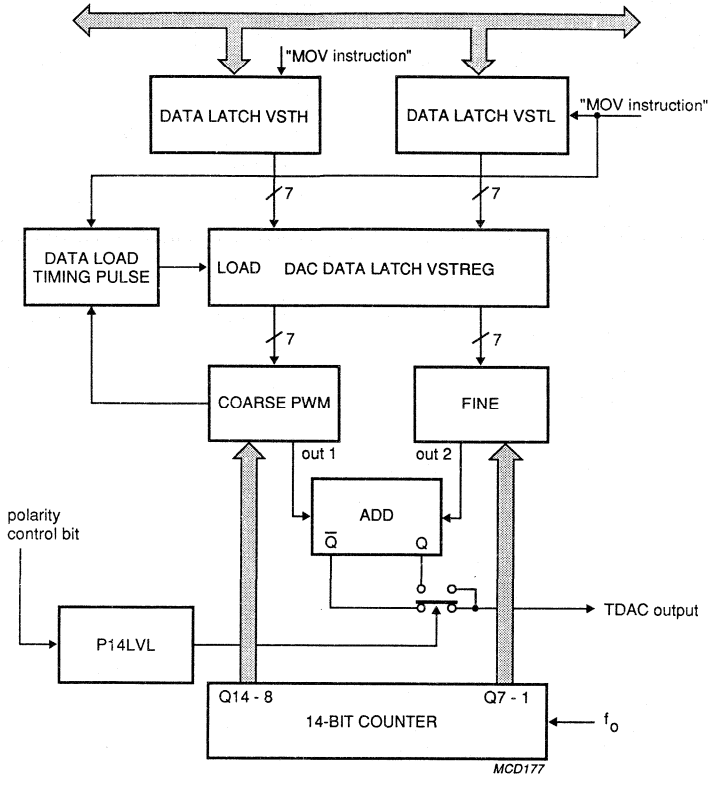


Fig.10 Block diagram: 14-bit PWM DAC.

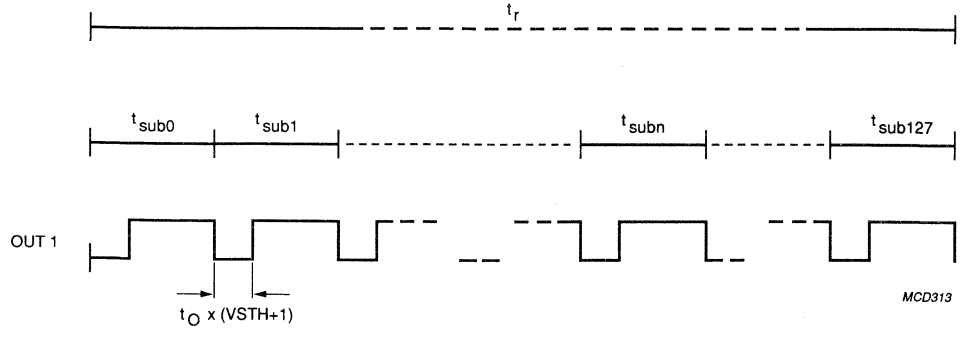


Fig.11 Coarse adjustment output (Out1).

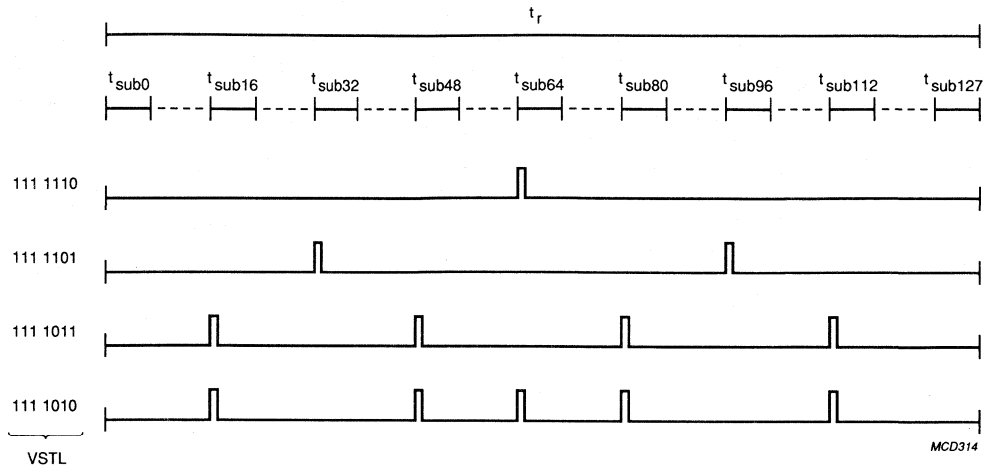


Fig.12 Fine adjustment output (Out2).

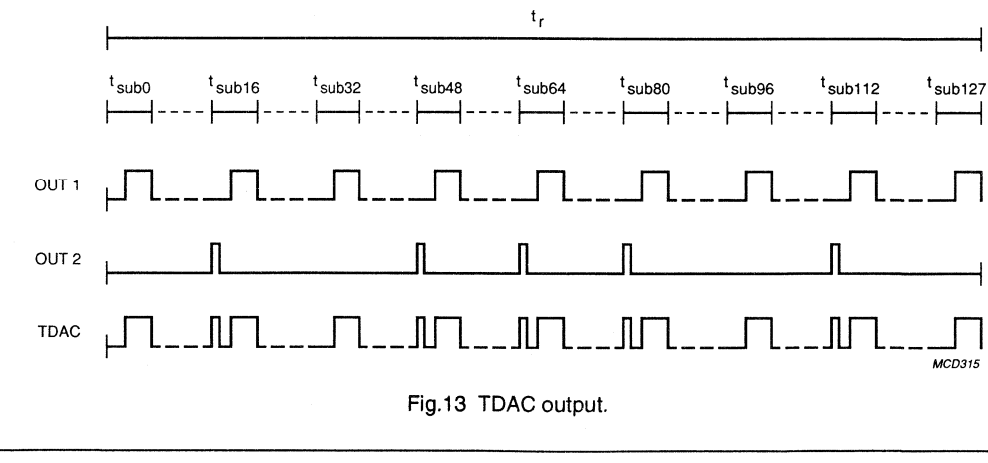


Fig.13 TDAC output.

8. AFC INPUT

The AFC input is used to measure the level of the Automatic Frequency Control signal. This is achieved by comparing the AFC input signal with the output of a 3-bit DAC as shown in Fig.14. DAC analog switches select one of 8 resistor taps connected between V_{DD} and V_{SS}. Consequently, eight different voltages may be selected (see Table 4). The compare signal AFCC, can be tested to determine whether the AFC input is higher or lower than the DAC level. The AFC input shares the same pin as the Derivative Port line DP1.7. The AFC function is selected by setting the enable bit AFCE to a logic 1. The Derivative Port function is selected by setting the AFCE bit to a logic 0.

Table 4 Selection of V_{ref}

AFC2	AFC1	AFC0	V_{ref}	V_{ref} (V_{DD} = 5.0 V)
0	0	0	V_{DD} x 0.125	0.625 V
0	0	1	V_{DD} x 0.250	1.250 V
0	1	0	V_{DD} x 0.375	1.875 V
0	1	1	V_{DD} x 0.500	2.500 V
1	0	0	V_{DD} x 0.625	3.125 V
1	0	1	V_{DD} x 0.750	3.750 V
1	1	0	V_{DD} x 0.875	4.375 V
1	1	1	V_{DD}	5.000 V

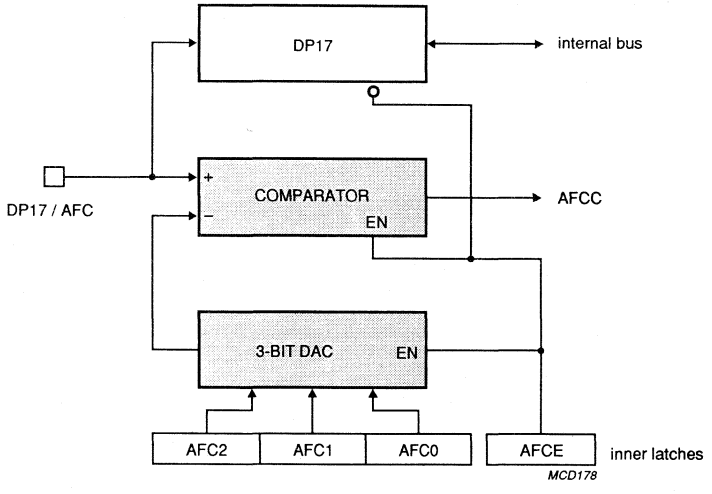


Fig.14 AFC circuit.

9. I/O

Each parallel I/O port line may be individually configured using one of three possible I/O mask options. The three I/O mask options are specified below:-

Option 1: Standard port with switched pull-up current source (see Fig. 15).

Option 2: Open drain (see Fig. 16).

Option 3: Push-pull (output only, see Fig. 17).

Table 5 specifies the possible port option list. When these devices are used for emulation purposes, in order to match the piggy back device provided it is recommended that the port options listed in Table 6 are used.

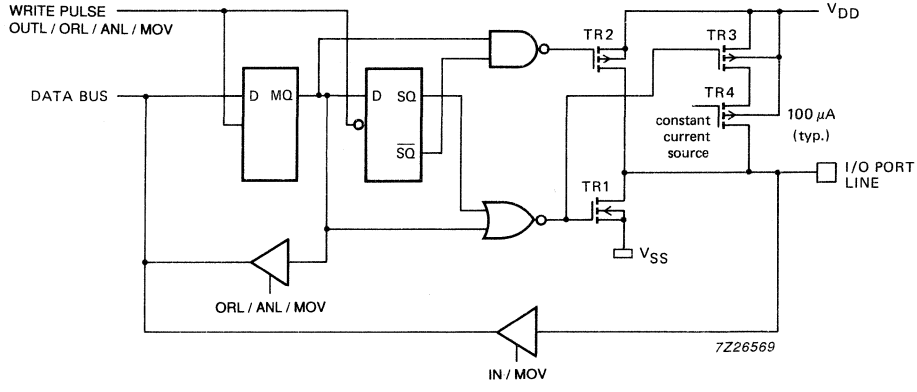


Fig.15 Standard output with switched pull-up current source (Option 1).

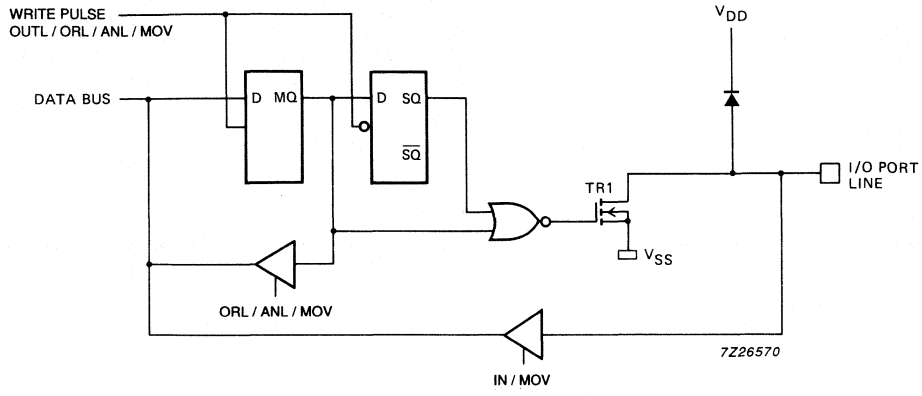


Fig.16 Open drain type I/O (Option 2).

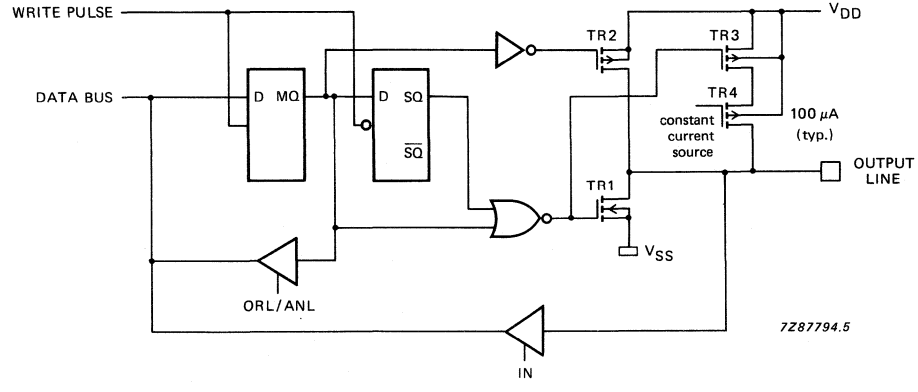


Fig.17 Push-pull type output (Option 3).

Table 5 User mask programmable port option list

PORT	PIN
P0.0	13
P0.1	14
P0.2	15
P0.3	16
P0.4	17
P0.5	18
P0.6	19
P0.7	20
P1.0	7
P1.1	8
P1.2	10
P1.3	11
P1.4	12
DP0.0	1
DP0.1	2
DP0.2	3
DP0.3	4
DP0.4	5
DP0.5	6
DP0.6	40
DP0.7	39
DP1.0	41
DP1.1	38
DP1.2	37
DP1.3	36
DP1.4	34
DP1.5	23
DP1.6	22
DP1.7	9
VOB	25.
VOW3	24.

Table 6 Port options for the 84C640 in emulation mode

PORT	PIN	OPTION
P0.0	13	1
P0.1	14	1
P0.2	15	1
P0.3	16	1
P0.4	17	1
P0.5	18	1
P0.6	19	1
P0.7	20	1
P1.0	7	1
P1.1	8	1
P1.2	10	1
P1.3	11	1
P1.4	12	1
DP0.0	1	
DP0.1	2	
DP0.2	3	
DP0.3	4	
DP0.4	5	
DP0.5	6	
DP0.6	40	2 S
DP0.7	39	2 S
DP1.0	41	
DP1.1	38	
DP1.2	37	
DP1.3	36	
DP1.4	34	
DP1.5	23	
DP1.6	22	
DP1.7	9	
VOB	25	
VOW3	24	

Notes

1. DP1.4 available only with the 84C440, 84C443, 84C640, 84C643, 84C840 and 84C843.
2. VOB and VOW3 pins; Option 1 not available.
3. Each pin can be configured to a High (S) or Low (R) state after power-on-reset. The required state of each pin is therefore specified by R or S.

10. ON SCREEN DISPLAY

10.1 Features

- Display format: 2 rows x 16 characters
- Software controlled vertical and horizontal display position
- 64 different characters in ROM - mask programmable
- Black box background
- Four programmable display character sizes
- Four programmable character dot matrix sizes: 6 x 9, 8 x 9, 6 x 13 or 8 x 13
- Half-dot rounding - for whole screen
- 4 from 7 colours possible on screen
- LC oscillator for on screen display function with the 84C441, 84C444, 84C641, 84C644, 84C841 and 84C844.
- RC oscillator for on screen display function with the 84C440, 84C443, 84C640, 84C643, 84C840 and 84C843.

HORIZONTAL DISPLAY POSITION CONTROL

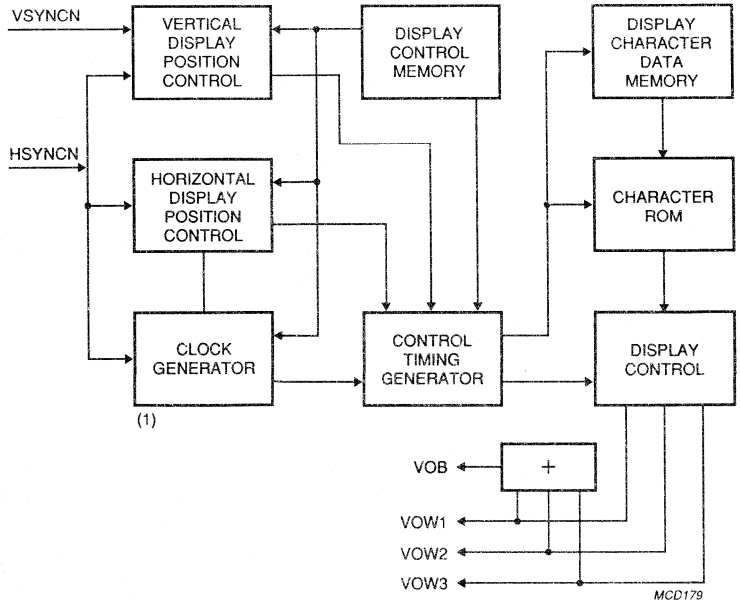
The horizontal position counter is incremented every OSD cycle after the programmed level of HSYNCN occurs at the HSYNCN pin. The counter is reset when the opposite polarity of the HSYNCN pulse is reached.

VERTICAL DISPLAY POSITION CONTROL

The vertical position counter is incremented every HSYNCN cycle and is reset by the VSYNCN signal.

CLOCK GENERATOR

The clock generator consists of an LC oscillator; the external LC network being connected across pins 28 and 29, see Fig.20. (The 84C440, 84C443, 84C640, 84C643, 84C840 and 84C843 use an RC oscillator connected between pin 28 and V_{SS}, see Fig.19). The OSD oscillator must be externally adjusted to the desired frequency (decreasing the OSD frequency gives broader characters). The oscillator is triggered on the trailing edge of HSYNC when the OSD logic is enabled and stops on the following leading edge of HSYNC.



(1) See Figs 19 and 20 for connection of external components.

Fig.18 OSD block diagram.

10.2 Display data registers

The display data registers consists of a group of 32 derivative registers located at addresses 20H to 3FH inclusive. The 16 registers located in memory at addresses 20H to 2FH contain display data for the first line. The remaining 16 registers located in memory at addresses 30H to 3FH, contain display data for the second line. At power-up the contents of the display data registers are undefined. The format of each Display data register is shown in Fig.21.

CC1 and CC0 - COLOUR CODE

The state of these two bits enable individual characters to be displayed in one of four colours.

MD0 to MD5 - CHARACTER CODE

The character set is stored in ROM and consists of 64 different characters. The selection of each character is dependent on the state of the 6 bits, MD0 to MD5.

10.3 Display control registers

The display control registers consists of a group of 6 derivative registers located at addresses 40H to 45H inclusive. (See Table 7 Display control registers). Each register may be read from or written to. After a reset operation the contents of the display control registers are zero.

Derivative register OSDCA

This register resides at address 40H.

HLVL - HORIZONTAL SYNCHRONOUS SIGNAL LEVEL

This bit selects the active level of the HSYNCN input signal. When HLVL is a logic 1, HSYNCN is active HIGH. When HLVL is a logic 0, HSYNCN is active LOW. See Fig.23.

VLVL - VERTICAL SYNCHRONOUS SIGNAL LEVEL

This bit selects the active level of the VSYNCN input signal. When VLVL is a logic 1, VSYNCN is active HIGH. When VLVL is a logic 0, VSYNCN is active LOW. See Fig.23.

STBY - STANDBY

This bit is used to enable or disable the OSD facility. If the STBY bit is a logic 1, the OSD oscillator is disabled. If the STBY bit is a logic 0, the OSD oscillator is enabled and the OSD facility is available. Before the oscillation frequency can be adjusted HSYNCN must be HIGH (if HLVL = 1). Oscillation stops by setting the HSYNCN pin LOW when HLVL = 1.

ROUND - CHARACTER ROUNDING CONTROL

The rounding function generates half dots where the corners of two dots meet. See Figs 24 and 25. The rounding function also works with multiple cell characters. When the Round bit is a logic 1, the rounding function is selected. When the Round bit is a logic 0, the rounding function is disabled.

RBLK - RASTER BLANKING CONTROL

When the RBLK bit is a logic 1, the VOB output is driven high to display the OSD characters on a blank screen. When the RBLK bit is a logic 0, the VOB output returns to its normal output state on the trailing edge of VSYNCN. See Fig.26.

CC34, CC24 and CC14 - CHARACTER COLOUR BITS

These bits are used for colour selection purposes. See Tables 9 to 14.

Table 7 Display control registers

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
40H	OSDCA	CC34	CC24	CC14	RBLK	ROUND	STBY	VLVL	HLVL
41H	LINE 0A	SZ01	SZ00	VP05	VP04	VP03	VP02	VP01	VP00
42H	LINE 0B	BLK0	VB0	HP05	HP04	HP03	HP02	HP01	HP00
43H	OSDCB	CDTW	CDTH	CC33	CC23	CC32	CC12	CC21	CC11
44H	LINE 1A	SZ11	SZ10	VP15	VP14	VP13	VP12	VP11	VP10
45H	LINE 1B	BLK1	VB1	HP15	HP14	HP13	HP12	HP11	HP10

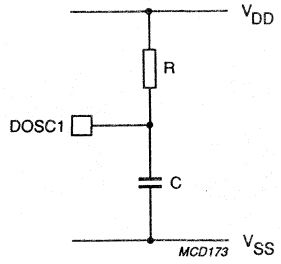


Fig.19 RC oscillator (84C440; 84C443; 84C640; 84C643; 84C840 and 84C843).

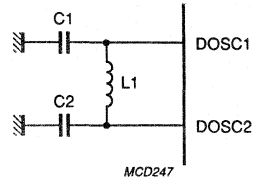


Fig.20 LC oscillator (84C441; 84C444; 84C641; 84C644; 84C841 and 84C844).

CC1 (MSB)	CC0	MD5	MD4	MD3	MD2	MD1	MD0 (LSB)

Fig.21 Display data register.

CC34 (MSB)	CC24	CC14	RBLK	ROUND	STBY	VLVL	HLVL (LSB)

Fig.22 Derivative register OSDCA.

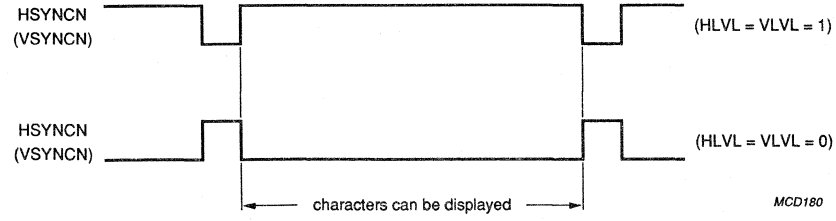


Fig.23 VSYNCN and HSYNCN active level.

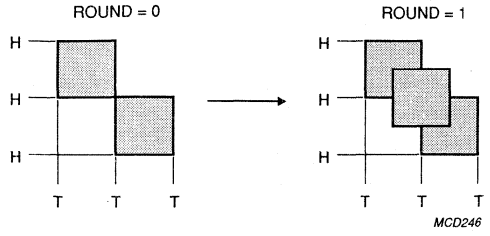


Fig.24 Rounding function.

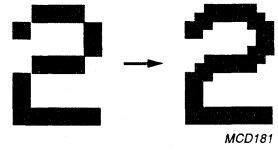


Fig.25 Rounding effect.

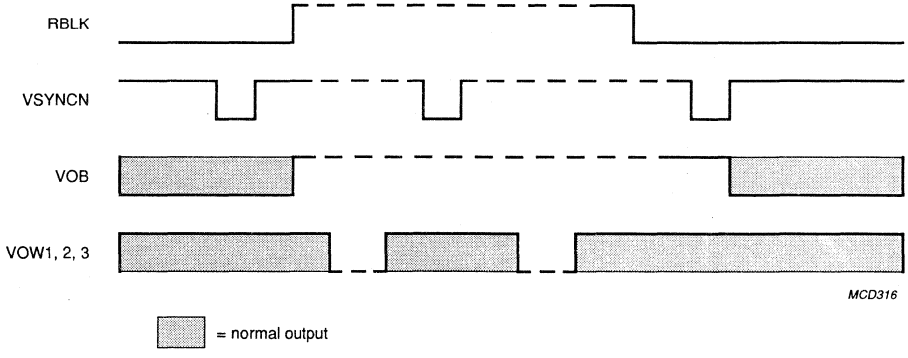


Fig.26 Raster blanking timing RLBK.

Derivative register LINE 0A

This register resides at address 41H. Its contents determine the character size and vertical position of the first row of display.

SZ00 and SZ01 - CHARACTER SIZE

The state of these two bits enable one of four possible character sizes to be selected for Row 0. Character sizes include background.

VP00 to VP05 - VERTICAL POSITION CONTROL

The vertical position of the first display row is selected by the state of the 6 bits, VP00 to VP05. The line number of the vertical start position for Row 0 is 4 x (decimal value of bits VP00 to VP05).

Row 0 and Row 1 must not overlap each other and therefore VP1 must be greater than or equal to (VP0 + H0), see Fig. 28. H0 is the character height of the characters in Row 0 and is a function of the number of dots per character and the state of the Size control bits SZ00 and SZ01. The four possible character heights are shown in Table 8.

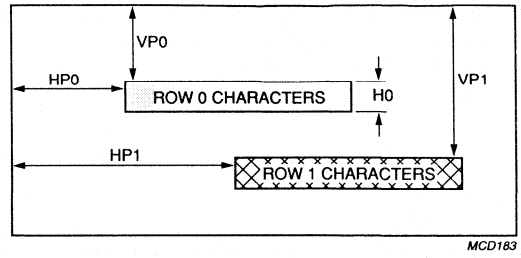


Fig.28 Display position.

SZ01 (MSB)	SZ00	VP05	VP04	VP03	VP02	VP01	VP00 (LSB)

Fig.27 Derivative register LINE 0A.

Table 8 OSD character sizes

DATA		CHARACTER SIZE				DOT MATRIX POINT	
SZx1	SZx0	VERTICAL		HORIZONTAL		VERTICAL	HORIZONTAL
		9D	13D	6D	8D		
0	0	18H	26H	12T	16T	2H	2T
0	1	36H	52H	24T	32T	4H	4T
1	0	54H	78H	36T	48T	6H	6T
1	1	72H	104H	48T	64T	8H	8T

Note

H denotes one horizontal line, T denotes one OSDC clock period and D denotes dots per character width/height.

Derivative register LINE 0B

The Derivative register LINE 0B resides at address 42H. Its contents determine the horizontal position of the first row of the display and whether the background and blanking functions are selected.

BLK0 - BLANKING

This bit enables or disables the character display. When BLK0 is a logic 1, the outputs VOW1, VOW2, VOW3 and VOB are disabled; consequently no characters are displayed. When BLK0 is a logic 1, the outputs VOW1, VOW2, VOW3 and VOB are enabled and characters are displayed.

VB0 - BACKGROUND

The state of the VB0 bit determines whether the background display is selected or not. If the VB0 bit is set to a logic 1, the characters in this line are displayed with background. If the VB0 bit is logic 0 the background is disabled and only the character is displayed.

HP01 to HP05 - HORIZONTAL POSITION CONTROL

These 6 bits determine the start position of the first display row. The horizontal position control is only active during OSDC clock cycles. (See Fig. 28).

The horizontal start position (HP) of Row 0 may be calculated using:

HP = 4 x (decimal value of bits HP00 to HP05) + 5 x (OSD C periods)

The decimal value of bits HP00 to HP05 must be greater than 10. Therefore, HP ≥ 45 (OSDC clock pulses).

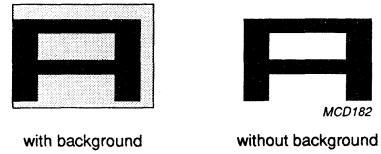


Fig.30 Background versus no background.

BLK0 (MSB)	VB0	HP05	HP04	HP03	HP02	HP01	HP00 (LSB)

Fig.29 Derivative register LINE 0B.

Derivative register OSDCB

The OSDCB register resides at address 43H. The contents of this register permit the size of the dot matrix grid to be selected and also enable four colours from a possible seven to be chosen for the display.

CDTW - CHARACTER DOT WIDTH CONTROL

The state of this bit determines the dot width of the character. When the CDTW bit is set to a logic 1, the character width is 6 dots. When the CDTW bit is set to a logic 0, the character width is 8 dots.

CDTH - CHARACTER DOT HEIGHT CONTROL

The state of this bit determines the dot height of the character. When the CDTH bit is set to a logic 1, the character height is 13 dots. When the CDTH bit is set to a logic 0, the character height is 9 dots.

CCXX - COLOUR CONTROL BITS

In every VSYNCN cycle one screen can select any 4 colours from 7 and in addition a blank or black screen. Colour selection is achieved using bits CC34, CC24 and CC14 in the OSDCA register; bits CC33, CC23, CC32, CC12, CC21, and CC11 in the OSDCB register and bits CC1 and CC0 from the display data registers. (See Table 9). Bits CC1X control VOW1 (red), bits CC2X control VOW2 (green) and bits CC3X control VOW3 (blue). Combinations of CCV2 and CCV3 control VOW1, VOW2 and VOW3.

In this way every combination of four colours can be made (black and white can not be displayed at the same time). Table 11 shows the possible combinations. The user may choose one colour out of each block. For example see Table 10.

Derivative register LINE 1A

This register resides at address 44H. Its contents determine the character size and vertical position of the second row of display.

SZ10 and SZ11 - CHARACTER SIZE

The state of these two bits enable one of four possible character sizes to be selected for Row 1. Character sizes include background. See Table 8 for character size selection.

VP10 to VP15 - VERTICAL POSITION CONTROL

The vertical position of the second display row is selected by the state of the 6 bits, VP10 to VP15. The line number of the vertical start position for Row 1 is 4 x (decimal value of bits VP15 to VP10).

Row 0 and Row 1 must not overlap each other and therefore VP1 must be greater than or equal to (VP0 + H0), see Fig. 28. H0 is the character height of the characters in Row 0 and is a function of the number of dots per character and the state of the size control bits SZ00 and SZ01. The four possible character heights are shown in Table 8.

CDTW (MSB)	CDTH	CC33	CC23	CC32	CC12	CC21	CC11 (LSB)

Fig.31 Derivative register OSDCB

Table 9 Character colour control

CC1	CC0	VOW1	VOW2	VOW3
0	0	CC11	CC21	$\overline{CC11 + CC21}$
0	1	CC12	$\overline{CC12 + CC32}$	CC32
1	0	$\overline{CC23 + CC33}$	CC23	CC33
1	1	CC14	CC24	CC34

Table 10 Example of selecting colours by programming CCxx

CHARACTER DATA	CHARACTER OUTPUT PINS		
VOW1 (Red)	VOW2 (Green)	VOW3 (Blue)	COLOUR
0	0	0	black
0	0	1	blue (2)
0	1	0	green (3)
0	1	1	cyan
1	0	0	red
1	0	1	magenta (4)
1	1	0	yellow (1)
1	1	1	white

Notes

If VOW1 = Red, VOW2 = Green, VOW3 = Blue, then using the bit combination CC11:1, CC21:1, CC12:0, CC32:1, CC23:1, CC33:0, CC14:1, CC24:0, CC34:1 the following colours may be selected.

1. Yellow; (CC1, CC0 = 00)
2. Blue; (CC1, CC0 = 01)
3. Green; (CC1, CC0 = 10)
4. Magenta; (CC1, CC0 = 11)

SZ11 (MSB)	SZ10	VP15	VP14	VP13	VP12	VP11	VP10 (LSB)

Fig.32 Derivative register LINE 1A.

Derivative register LINE 1B

The Derivative register LINE 1B resides at address 45H. Its contents determine the horizontal position of the second line of the display (Line 1) and whether the background and blanking functions are selected.

BLK1 - BLANKING

This bit enables or disables the character display. When BLK1 is a logic 1, the outputs VOW1, VOW2, VOW3 and VOB are disabled; consequently no characters are displayed. When BLK1 is a logic 1, the outputs VOW1, VOW2, VOW3 and VOB are enabled and characters are displayed.

VB1 - BACKGROUND

The state of the VB1 bit determines whether the background display is selected or not. If the VB1 bit is set to a logic 1, the characters in this line are displayed with background. If the VB1 bit is logic 0, the background is disabled and only the character is displayed. The visual effect of background versus no background is shown in Fig.30.

HP11 to HP15 - HORIZONTAL POSITION CONTROL

These 6 bits determine the start position of the second display line (Line 1). The horizontal position control is only active during OSDC clock cycles. (See Fig. 28). The horizontal start position (HP) of Line 1 may be calculated using:

HP = 4 x (decimal value of bits HP10 to HP15)) + 5 x (OSD C periods)

The decimal value of bits HP10 to HP15 must be greater than 10. Therefore, HP ≥ 45 (OSDC clock pulses)

Character ROM

Character ROM contains the dot character fonts. 13 x 8 dots are reserved for each character, regardless of the dot matrix size actually selected. The dot matrix grid is shown in Fig.34.

The document 'How to prepare the character ROM code for the OSD part of the PCA84C640' is available on request.

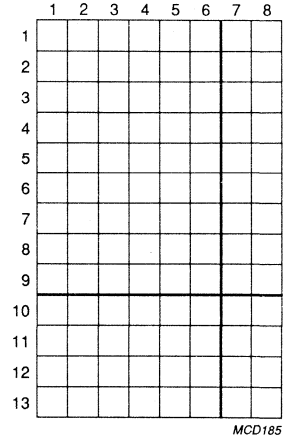


Fig.34 Character ROM.

BLK1 (MSB)	VB1	HP15	HP14	HP13	HP12	HP11	HP10 (LSB)

Fig.33 Derivative register LINE 1B.

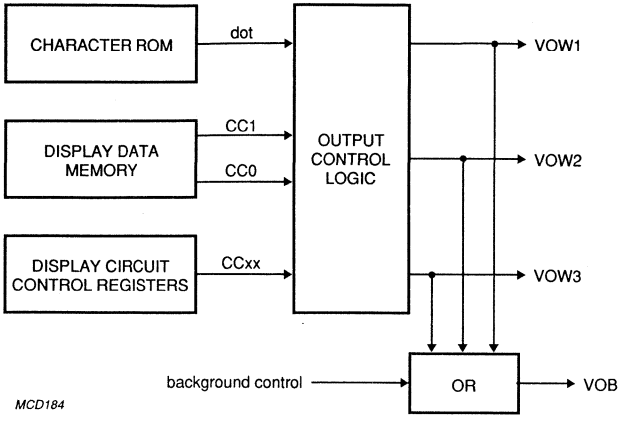


Fig.35 Colour control.

Table 11 Possible colour combinations

CHARACTER DATA		VOW1	VOW2	VOW3	COLOUR
CC1	CC0	CC11	CC21	$\overline{CC11+CC21}$	
0	0	0	0	1	blue
0	0	0	1	0	green
0	0	1	0	0	red
0	0	1	1	0	yellow

Table 12 Possible colour combinations

CHARACTER DATA		VOW1	VOW2	VOW3	COLOUR
CC1	CC0	CC12	$\overline{CC12+CC32}$	CC32	
0	1	0	0	1	blue
0	1	0	1	0	green
0	1	1	0	0	red
0	1	1	0	1	magenta

Table 13 Possible colour combinations

CHARACTER DATA		VOW1	VOW2	VOW3	COLOUR
CC1	CC0	$\overline{CC23+CC33}$	CC23	CC33	
1	0	0	0	1	blue
1	0	0	1	0	green
1	0	0	1	1	cyan
1	0	1	0	0	red

Table 14 Possible colour combinations

CHARACTER DATA		VOW1	VOW2	VOW3	COLOUR
CC1	CC0	CC14	CC24	CC34	
1	1	0	0	0	black
1	1	0	0	1	blue
1	1	0	1	0	green
1	1	0	1	1	cyan
1	1	1	0	0	red
1	1	1	0	1	magenta
1	1	1	1	0	yellow
1	1	1	1	1	white

11. EMULATION MODE

The emulation mode configuration is shown in Fig.36.

In the emulation mode configuration the PCA84C640's CPU is disabled and only its derivative logic is active. The device is controlled by the PCF84C00 bond-out chip. The PCA84C640's two derivative ports act as additional ports for the PCF84C00. The interaction between the two devices is as follows:

1. During the first machine cycle the PCF84C00 fetches an instruction from EPROM and then decodes that instruction.
2. During the second machine cycle the PCF84C00 executes the decoded instruction. If the instruction is related to the derivative ports then DXALE, DXRDN and/or DXWRN become active and the PCA84C640 operates as a peripheral of the PCF84C00.
3. Depending on the type of instruction executed during the second machine cycle the following data transfer happens:
   (a) During TS1 data from the EPROM is available on P0.0 to P0.7 which is then available on IB0.0 of the PCF84C00.
   (b) During TS4 data from the PCA84C640 can be transferred to the PCF84C00.
   (c) During TS6 data from the PCF84C00 can be transferred to the PCA84C640.

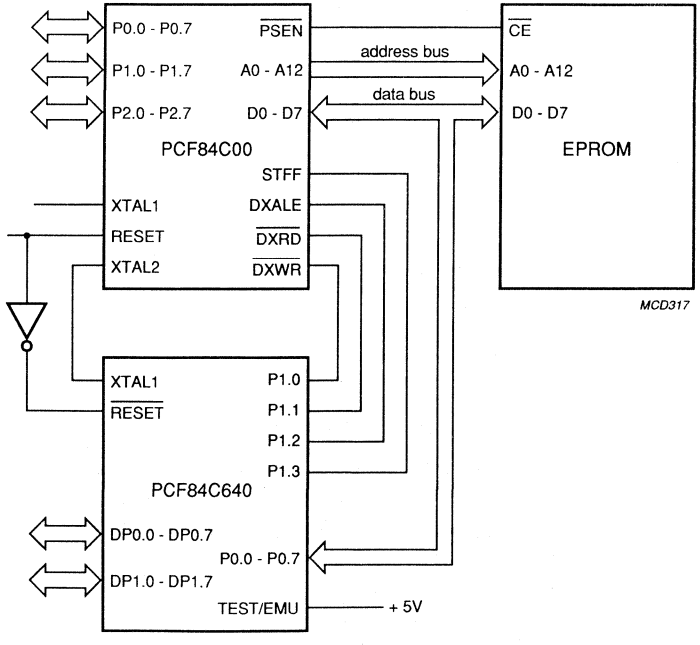


Fig.36 Emulation mode configuration.

12. DIFFERENCES BETWEEN THE 84C44X, 84C64X AND 84C84X

Table 15 Differences between the 84C440; 84C441; 84C443 and 84C444

FEATURE	84C440	84C441	84C443	84C444
ROM	4 Kbytes	4 Kbytes	4 Kbytes	4 Kbytes
RAM	128 bytes	128 bytes	128 bytes	128 bytes
OSD oscillator	RC	LC	RC	LC
general purpose I/O lines	18	17	18	17
pin assignment	pin 34 = DP1.4 pin 29 = T1	pin 34 = T1 pin 29 = DOSC2	pin 34 = DP1.4 pin 29 = T1	pin 34 = T1 pin 29 = DOSC2
Register DP1 - pin; bit DP1.4	available	not available	available	not available
Register DP1 - latch; bit DP1.4	available	not available	available	not available
port line DP14	available	not available	available	not available
I²C interface	available	available	not available	not available

Table 16 Differences between the 84C640; 84C641; 84C643 and 84C644

FEATURE	84C640	84C641	84C643	84C644
ROM	6 Kbytes	6 Kbytes	6 Kbytes	6 Kbytes
RAM	128 bytes	128 bytes	128 bytes	128 bytes
OSD oscillator	RC	LC	RC	LC
general purpose I/O lines	18	17	18	17
pin assignment	pin 34 = DP1.4 pin 29 = T1	pin 34 = T1 pin 29 = DOSC2	pin 34 = DP1.4 pin 29 = T1	pin 34 = T1 pin 29 = DOSC2
Register DP1 - pin; bit DP1.4	available	not available	available	not available
Register DP1 - latch; bit DP1.4	available	not available	available	not available
port line DP14	available	not available	available	not available
I²C interface	available	available	not available	not available

Table 17 Differences between the 84C840; 84C841; 84C843 and 84C844

FEATURE	84C840	84C841	84C843	84C844
ROM	8 Kbytes	8 Kbytes	8 Kbytes	8 Kbytes
RAM	192 bytes	192 bytes	192 bytes	192 bytes
OSD oscillator	RC	LC	RC	LC
general purpose I/O lines	18	17	18	17
pin assignment	pin 34 = DP1.4 pin 29 = T1	pin 34 = T1 pin 29 = DOSC2	pin 34 = DP1.4 pin 29 = T1	pin 34 = T1 pin 29 = DOSC2
Register DP1 - pin; bit DP1.4	available	not available	available	not available
Register DP1 - latch; bit DP1.4	available	not available	available	not available
port line DP14	available	not available	available	not available
I²C interface	available	available	not available	not available

13. REGISTER MAP

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER
00H	DP0.7 (x) R	DP0.6 (x) R	DP0.5 (x) R	DP0.4 (x) R	DP0.3 (x) R	DP0.2 (x) R	DP0.1 (x) R	DP0.0 (x) R	DP0R (pin)
01H	DP1.7 (x) R	DP1.6 (x) R	DP1.5 (x) R	DP1.4[1] (x) R	DP1.3 (x) R	DP1.2 (x) R	DP1.1 (x) R	DP1.0 (x) R	DP1R (pin)
02H	DP0.7 (1) R/W	DP0.6 (1) R/W	DP0.5 (1) R/W	DP0.4 (1) R/W	DP0.3 (1) R/W	DP0.2 (1) R/W	DP0.1 (1) R/W	DP0.0 (1) R/W	DP0R (latch)
03H	DP1.7 (1) R/W	DP1.6 (0) R/W	DP1.5 (0) R/W	DP1.4[1] (1) R/W	DP1.3 (1) R/W	DP1.2 (1) R/W	DP1.1 (1) R/W	DP1.0 (1) R/W	DP1R (latch)
10H	-	-	PWM15 (0) R/W	PWM14 (0) R/W	PWM13 (0) R/W	PWM12 (0) R/W	PWM11 (0) R/W	PWM10 (0) R/W	PWM1
11H	-	-	PWM22 (0) R/W	PWM24 (0) R/W	PWM23 (0) R/W	PWM22 (0) R/W	PWM21 (0) R/W	PWM20 (0) R/W	PWM2
12H	-	-	PWM35 (0) R/W	PWM34 (0) R/W	PWM33 (0) R/W	PWM32 (0) R/W	PWM31 (0) R/W	PWM30 (0) R/W	PWM3
13H	-	-	PWM45 (0) R/W	PWM44 (0) R/W	PWM43 (0) R/W	PWM42 (0) R/W	PWM41 (0) R/W	PWM40 (0) R/W	PWM4
14H	-	-	PWM55 (0) R/W	PWM54 (0) R/W	PWM53 (0) R/W	PWM52 (0) R/W	PWM51 (0) R/W	PWM50 (0) R/W	PWM5
15H	-	VST06 (0) R/W	VST05 (0) R/W	VST04 (0) R/W	VST03 (0) R/W	VST02 (00 R/W	VST01 (0) R/W	VST00 (0) R/W	VSTL
16H	-	VST13 (0) R/W	VST12 (0) R/W	VST11 (0) R/W	VST10 (0) R/W	VST09 (0) R/W	VST08 (0) R/W	VST07 (0) R/W	VSTH
17H	-	-	-	-	-	AFC2 (0) R/W	AFC1 (0) R/W	AFC0 (0) R/W	AFCO
18H	-	-	-	-	-	-	-	AFCC (x) R	AFCC
19H	SCLE (0) R/W	SDAE (0) R/W	PWM5E (0) R/W	PWM4E (0) R/W	PWM3E (0) R/W	PWM2E (0) R/W	PWM1E (0) R/W	TDACE (0) R/W	DP0E/PWME
1AH	-	-	-	AFCE (0) R/W	P14LVL (0) R/W	P6LVL (0) R/W	VOW2E (0) R/W	VOW1E (0) R/W	DP1E/ PWMLVL
20H-3FH	CC1 (x) W	CC0 (x) W	MD5 (x) W	MD4 (x) W	MD3 (x) W	MD2 (x) W	MD1 (x) W	MD0 (x) W	DATA DISPLAY MEMORY

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER
40H	CC34 (0) R/W	CC24 (0) R/W	CC14 (0) R/W	RBLK (0) R/W	ROUND (0) R/W	STBY (1) R/W	VLVL (0) R/W	HLVL 0 R/W	OSDCA
41H	SZ01 (0) R/W	SZ00 (0) R/W	VP05 (0) R/W	VP04 (0) R/W	VP03 (0) R/W	VP02 (0) R/W	VP01 (0) R/W	VP00 (0) R/W	LINE 0A
42H	BLK0 (0) R/W	VB0 (0) R/W	HP05 (0) R/W	HP04 (0) R/W	HP03 (0) R/W	HP02 (1) R/W	HP01 (0) R/W	HP00 (0) R/W	LINE 0B
43H	CDTW (0) R/W	CDTH (0) R/W	CC33 (0) R/W	CC23 (0) R/W	CC32 (0) R/W	CC12 (1) R/W	CC21 (0) R/W	CCV11 (0) R/W	OSDCB
44H	SZ11 (0) R/W	SZ10 (0) R/W	VP15 (0) R/W	VP14 (0) R/W	VP13 (0) R/W	VP12 (1) R/W	VP11 (0) R/W	VP10 (0) R/W	LINE 1A
45H	BKL1 (0) R/W	VB1 (0) R/W	HP15 (0) R/W	HP14 (0) R/W	HP13 (0) R/W	HP12 (1) R/W	HP11 (0) R/W	HP10 (0) R/W	LINE 1B

Notes

1. These bits are not available in the 84C441, 84C444, 84C641, 84C644, 84C841 and the 84C844.
2. The number within parentheses denotes the initial state; 'x' denotes don't care.

14. LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage range	−0.3	+7.0	V
V_I	all input voltages	−0.3	V_{DD} + 0.3	V
$-I_{OH}$	maximum source current - all port lines	-	10	mA
$-I_{OL}$	maximum sink current - all port lines	-	30	mA
P_{tot}	total power dissipation	-	900	mW
T_{stg}	storage temperature range	−55	+ 125	°C
T_{amb}	operating ambient temperature range - all devices	−20	+ 70	°C

15. DC CHARACTERISTICS

V_{DD} = 5 V ±10%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C; all voltages with respect to V_{SS} unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	operating voltage		4.5	5.0	5.5	V
I_{DD}	operating current	$f_{OSDCRC} = f_{OSDCLC} = f_{XTAL}$; see note 1				
		V_{DD} = 5 V; f_{XTAL} = 10 MHz	-	5	10	mA
		V_{DD} = 5 V; f_{XTAL} = 6 MHz	-	3.5	8	mA
I_{DD}	operating current	$f_{OSDCRC} = f_{OSDCLC}$ = STOP; see note 1				
		V_{DD} = 5 V; f_{XTAL} = 10 MHz	-	3	7	mA
		V_{DD} = 5 V; f_{XTAL} = 6 MHz	-	1.5	3.5	mA
I_{DD}	Idle mode current	V_{DD} = 5 V; f_{XTAL} = 10 MHz	-	1.3	3	mA
		V_{DD} = 5 V; f_{XTAL} = 6 MHz; see note 1	-	0.8	1.5	mA
I_{DD}	Stop mode current	V_{DD} = 5.5 V; see notes 1 and 2	-	5	10	µA
Inputs						
V_{IL}	input LOW voltage; Ports P0; P1; DP0; DP1; HSYNCN; VSYNCN		0	-	$0.3V_{DD}$	V
V_{IH}	input HIGH voltage; Ports P0; P1; DP0; DP1; HSYNCN; VSYNCN		$0.7V_{DD}$	-	V_{DD}	V
I_{IH}	input current RESET	V_{in} = 0.5 V	20	-	-	µA
V_{AI}	input voltage; DP1.7; AFC1		V_{SS}	-	V_{DD}	V
V_{AE}	conversion error range (AFC)		-	-	± 1/2	LSB
$\pm I_{LI}$	input leakage current; Ports P0; P1; DP0; DP1	$V_{SS} < V_I < V_{DD}$	-	-	10	µA
$\pm I_{LI}$	input leakage current INTN/T0; T1	$V_{SS} < V_I < V_{DD}$	0.01	0.20	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
I_{OL}	output LOW sink current; Port P0	V_{DD} = 5 V ±10%; V_O = 1.2 V	10	-	-	mA
I_{OL}	output LOW sink current; Ports P1; DP0; DP1; VOB; VOW3	V_{DD} = 5 V ±10%; V_O = 0.4 V	1.6	3	-	mA
I_{OH}	pull-up output HIGH source current; Ports P0; P1; DP0; DP1	V_{DD} = 5 V ± 10%; V_O = 0.7V_{DD}	40	-	-	µA
I_{OH}	pull-up output HIGH source current; Ports P0; P1; DP0; DP1	V_{DD} = 5 V ± 10%; V_O = V_{SS}	-	-	400	µA
I_{OH}	push-pull output HIGH source current; Ports P0; P1; DP0; DP1; VOB; VOW3	V_{DD} = 5 V ± 10%; V_O = V_{DD}–0.4V	1.6	3	-	mA

Notes

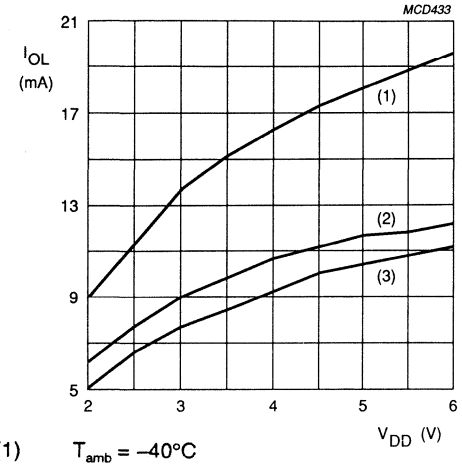
1. V_{IL} = V_{SS}; V_{IH} = V_{DD}; all outputs and sense input lines unloaded. All open drain ports connected to V_{SS}.
2. Crystal is connected between XTAL1 and XTAL2; T1 = V_{SS}; INTN/T0 = V_{DD}.

16. AC CHARACTERISTICS

16.1 Oscillator requirements

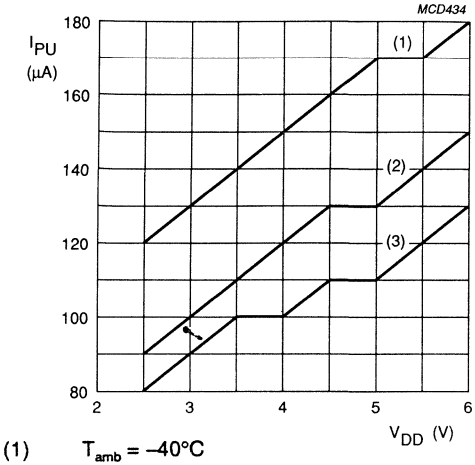
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{XTAL}	crystal frequency	V_{DD} = 5 V ±10%	1	10	MHz
f_{DOSC}	DOS oscillator frequency	V_{DD} = 5 V ±10%	-	10	MHz

16.2 Characteristic curves



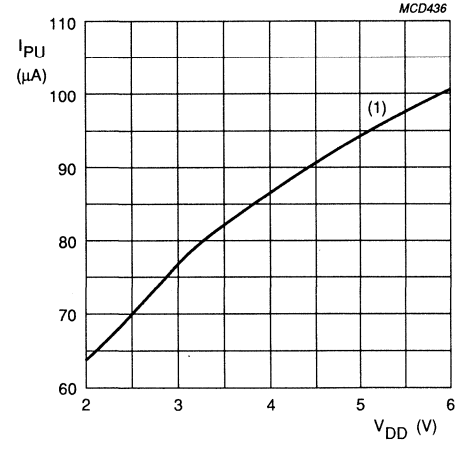
(1) T_{amb} = –40°C
(2) T_{amb} = 25°C
(3) T_{amb} = 85°C

Fig.37 Typical output sink current as a function of supply voltage; V_O = 0.4 V.



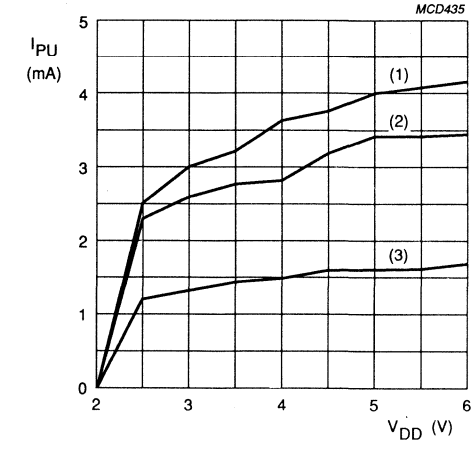
(1) T_{amb} = –40°C
(2) T_{amb} = 25°C
(3) T_{amb} = 85°C

Fig.38 Typical pull-up current as a function of supply voltage; V_O = 0 V.



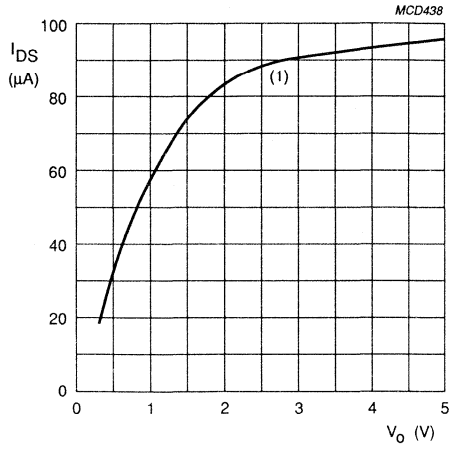
(1) T_{amb} = 25°C

Fig.39 Typical pull-up current as a function of supply voltage; $V_O = 0.7V_{DD}$.



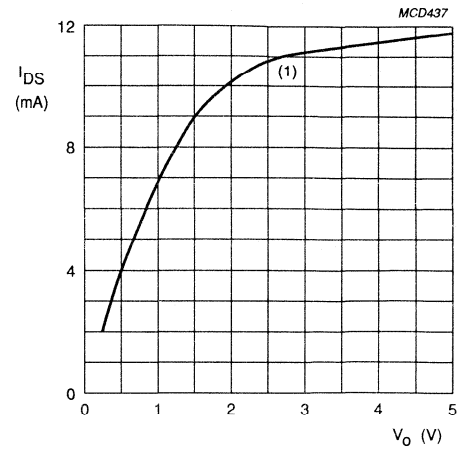
(1) T_{amb} = –40°C
(2) T_{amb} = 25°C
(3) T_{amb} = 85°C

Fig.40 Typical booster current as a function of supply voltage; $V_O = V_{DD} - 0.4$ V.



(1) T_{amb} = 25°C

Fig.41 Typical open drain sink capability as a function of V_O; Port 0



(1) T_{amb} = 25°C

Fig.42 Typical open drain sink capability as a function of V_O; DP0.0 to DP0.7, DP1.5 to DP1.7 and P1.0 to P1.4

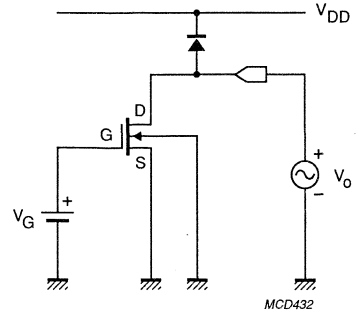
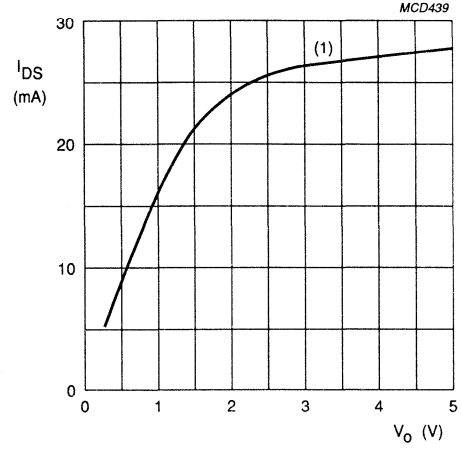


Fig.43 Open drain test circuit; DP0.0 to DP0.7, DP1.5 to DP1.7 and P1.0 to P1.4



(1) T_{amb} = 25°C

Fig.44 Typical open drain sink capability as a function of V_O; VOW3 and VOB0

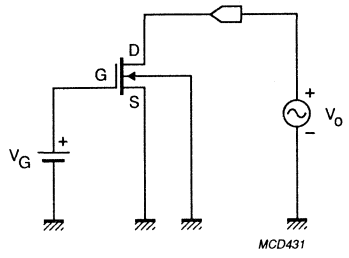


Fig.45 Open drain test circuit; VOW3 and VOB

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

8-bit microcontrollers PCA84C122

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATASHEET

FEATURES

- 84Cxxx CPU
- 1 K bytes of ROM
- 32 bytes of RAM
- 12 (PCA84C122B) or 16 (PCA84C122A) quasi-bidirectional I/O lines (standard port option)
- two test inputs T0, T1
- 3 single level vectored interrupt sources: external (T0/$\overline{INT}$ and Port 1, for keypad press wake up function), timer/counter (TI) and hardware modulator interrupt
- 8-bit programmable timer with 5-bit pre-scaler
- on-board oscillator 1 MHz to 5 MHz
- single supply voltage from 2.0 V to 5.5 V
- Operating temperature range: –20 to +70 °C
- Power saving modes: idle and stop modes are provided to save power consumption when no key is pressed for a period of time
- "Hardware Modulator" that provides pulse bursts of which the 'on' time and 'off' time of each pulse (i.e. duty cycle) and the number of pulses are programmable
- One output line from the "Hardware Modulator" to control the driver transistor for the IR-LED. Capable of sink 30 mA at V_{DD} = 2.0 V, $V_{\overline{OUT}}$ = 1.0 V
- Watchdog timer to keep the transmitter from being locked or malfunction. Automatic system reset is generated by the WDT if the timer is not reset, before overflow from counting within a certain period of time
- Packages: 20 lead SOT163A (PCA84C122B), 24 lead SOT137A (PCA84C122A).

GENERAL DESCRIPTION

The P84C122 is a stand-alone microcontroller designed for use in a remote control transmitter for TV, audio equiptment etc. The P84C122 device provides a number of dedicated hardware functions for remote controller applications. These include the following additional blocks to the 84Cxxx core (for further reference see, "Data Handbook IC14" and, data sheet "PCF84C12"):

- Interrupt Gate
- Hardware Modulator
- Output Driver.
- Watchdog Timer

In Fig.1 the block diagram of the P84C122 is shown. The 84Cxxx core plus 1 Kbytes ROM and 32 bytes RAM has the same function as described in the data sheets of the 84Cxxx and 84C12.
When the transmitter is not in use the microcontroller is in STOP mode and the scan lines (port 0) are set to '0'. When a key is depressed an interrupt is generated by means of the 8–input AND–gate. The Watchdog Timer will reset the P84C122 when it has not been reloaded (reset) in time, because the program has run out of sequence (endless loop, continuous IDLE mode etc). During normal program execution the counter should be reloaded at least once for each RC–word that is transmitted. During STOP mode the oscillator is halted, so then the Watchdog Timer is not running.

The Hardware Modulator produces pulse bursts according to the required protocol. By software the 'ON-time' and the 'OFF-time' of each pulse and the number of pulses are controlled. The output driver can handle sufficient current to drive a single transistor, and this can provide the required current for the LED.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCA84C122A	24	DIL	plastic	SOT137A
PCA84C122B	20	DIL	plastic	SOT163A

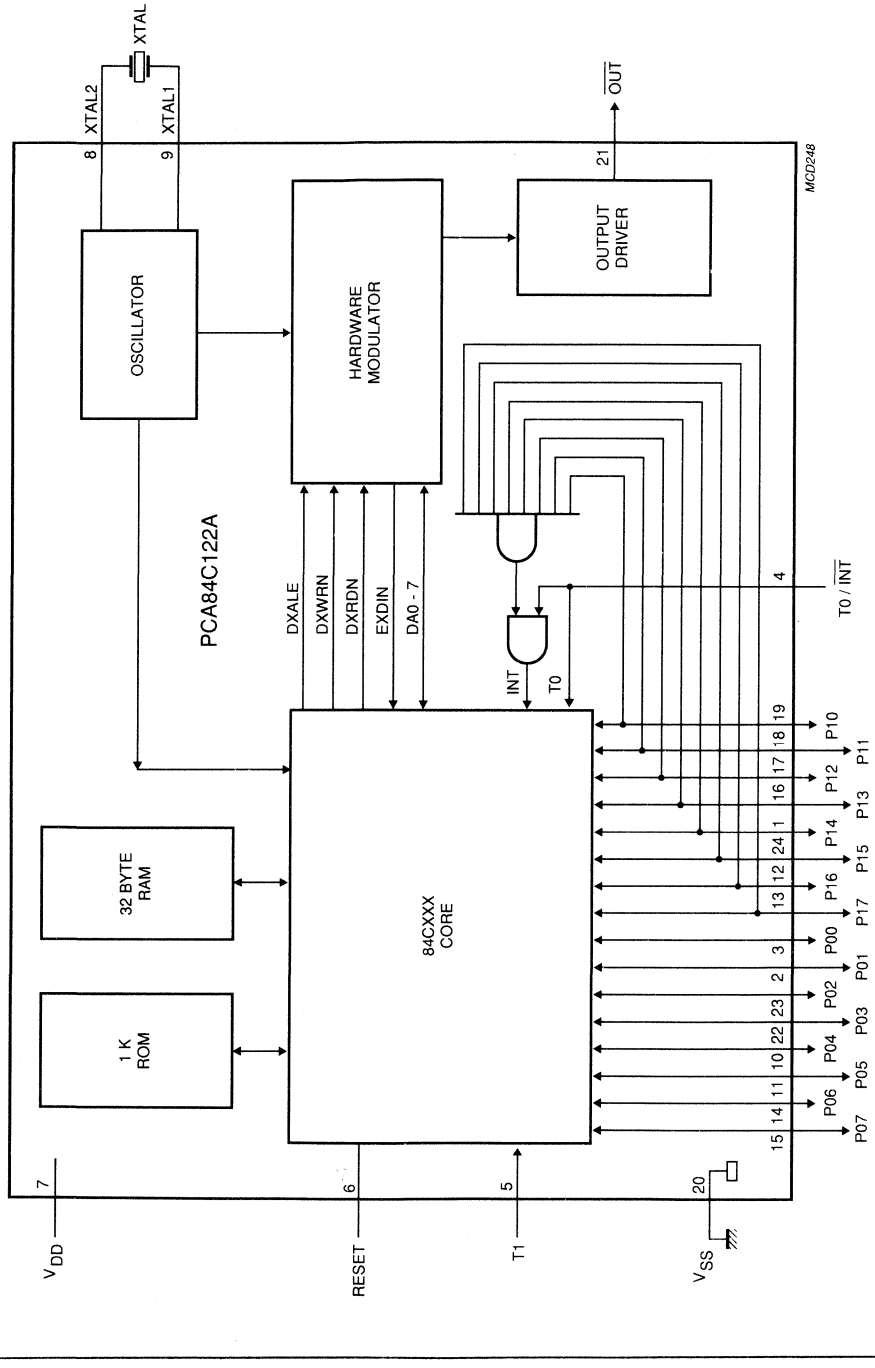


Fig.1 PCA84C122A Block diagram.

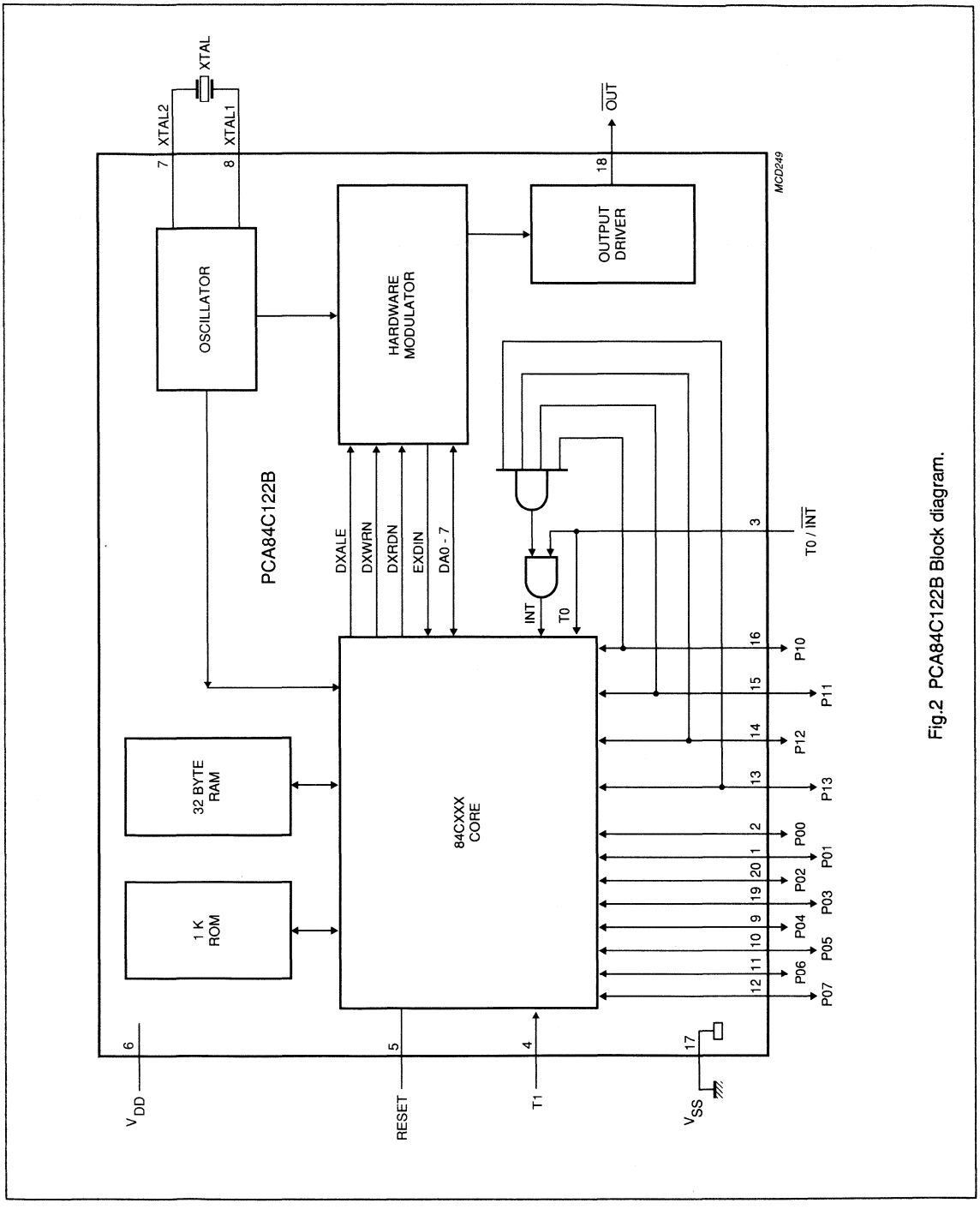


Fig.2 PCA84C122B Block diagram.

8 K x 8-bit static CMOS EEPROM with PAGE-ERASE option

PCF29F64

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC10 OR DATASHEET

FEATURES

- Low Power CMOS
  - maximum active current 10 mA
  - maximum standby current 200 µA
- Access time 200 ns
- Fast Erase cycle time
  - 32-byte Erase operation (PAGE-Erase)
  - 256-byte Erase operation (BLOCK-Erase)
  - complete Memory Erase operation
- Fast Write cycle time
- $\overline{\text{Data}}$ Polling allows user to minimize Write cycle time
- Simple Write operation
  - single TTL-level $\overline{\text{WE}}$ signal
  - internally latched address and data
  - automatic Write timing
- Endurance 10 000; T_{amb} = 85 °C
- 10 years non-volatile data retention time

GENERAL DESCRIPTION

The PCF29F64 is an 8 K x 8-bit floating gate electrically erasable programmable read only memory (EEPROM), fabricated in a 1.2 micron n-channel floating gate CMOS technology.

Power consumption is very low and reliability is high due to the full CMOS technology used, as that for the PC.8582 family.

Three different Erase-operation modes are performed by the PCF29F64:

- 32-byte Erase operation (PAGE)
- 256-byte Erase operation (BLOCK)
- Complete Memory Erase operation

A write operation is performed in approximately 1.0 ms, which allows the entire memory to be written in less than 10 s.

The PCF29F64 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

Philips EPROMs and PAGE-EEPROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	-	5.5	V
I_{DDR}	supply current READ (CMOS inputs)	-	-	5	mA
I_{DDW}	supply current WRITE/ERASE (CMOS inputs)	-	-	10	mA
I_{DDO}	standby supply current	-	-	200	µA

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
TYPE NUMBER	PINS	PIN POSITION	MATERIAL	CODE
PCF29F64P	28	DIL	plastic	SOT117
PCF29F64T	28	mini-pack	plastic	SO28; SOT136A

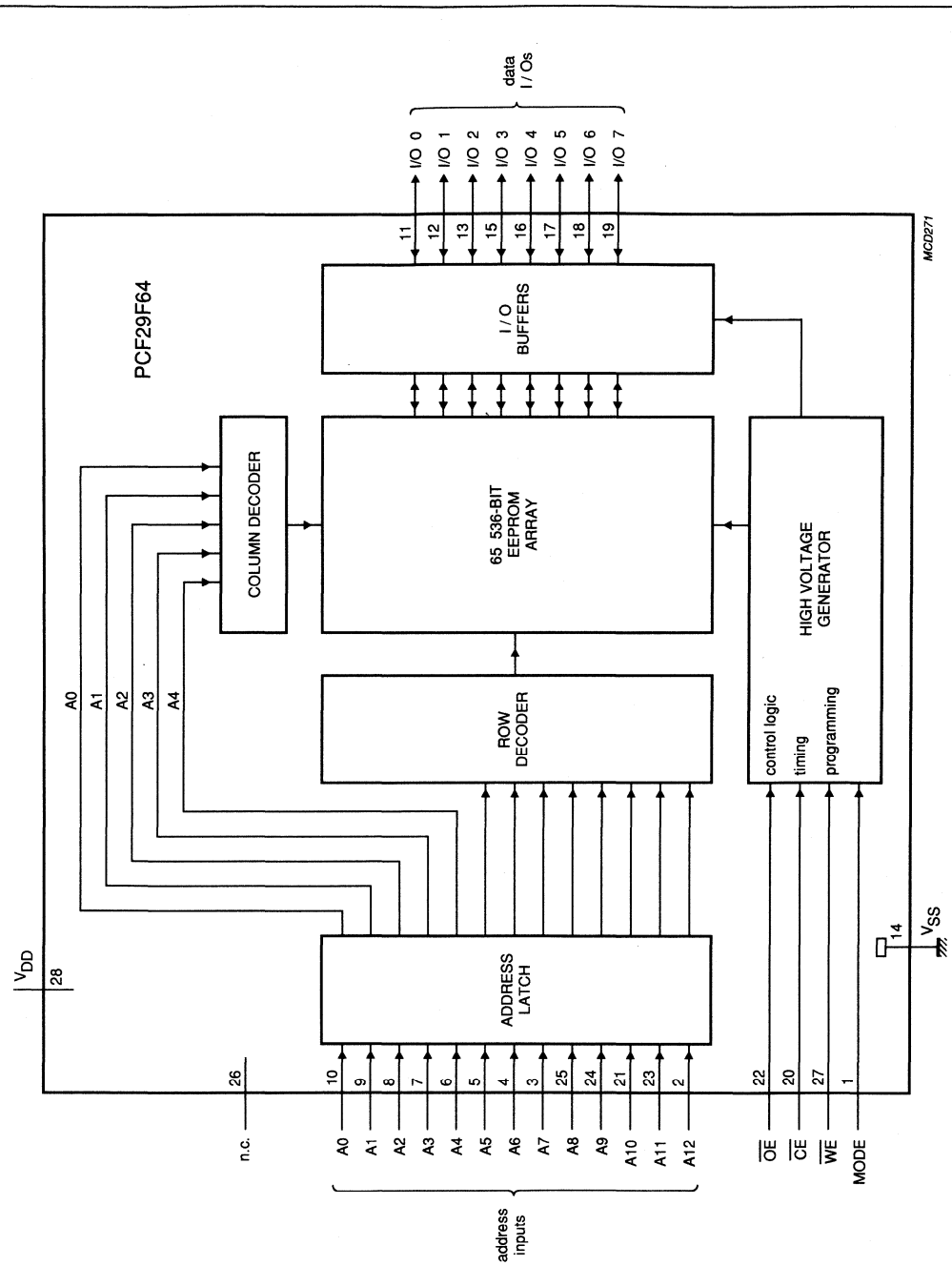


Fig.1 Block diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

18-ELEMENT BAR GRAPH LCD DRIVER

GENERAL DESCRIPTION

The PCF1303T is an 18-element bar graph LCD driver with linear relation to control voltage (V_c) when in pointer or thermometer mode.

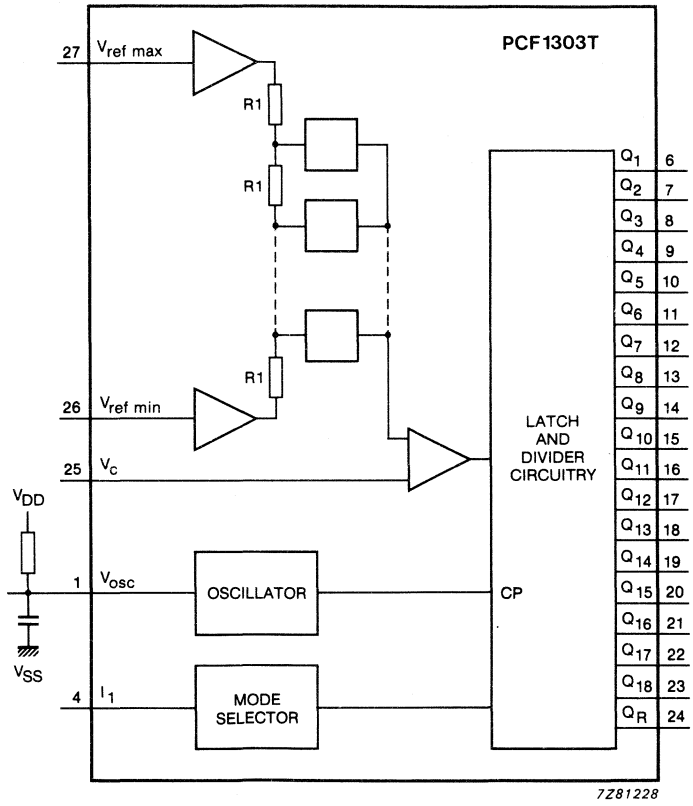
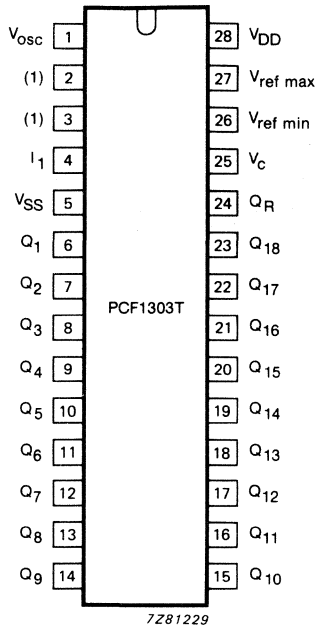


Fig. 1 Block diagram.

PACKAGE OUTLINE

PCF1303T: 28-lead mini-pack; plastic (SO28; SOT136A).



(1) Pins 2 and 3 should be connected to V_{SS}.

Fig. 2 Pin configuration.

PIN DESCRIPTION

pin no.	symbol	name and function
1	V_{osc}	oscillator pin
4	I_1	mode select input
5	V_{SS}	ground (0 V)
6 to 23	Q_1 to Q_{18}	segment outputs
24	Q_R	back-plane output
25	V_c	control voltage
26 27	$V_{ref\ min}$ $V_{ref\ max}$	reference voltage inputs
28	V_{DD}	positive supply voltage

FUNCTION TABLE

I_1	mode
L	pointer
H	thermometer

H = HIGH voltage level
L = LOW voltage level

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

LCD DRIVER

GENERAL DESCRIPTION

The members of the PCF21XX family are single chip, silicon gate CMOS circuits. A three-line bus (CBUS) structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- Supply voltage 2,25 to 6,5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possibility
- Power-on reset clear

	PCF2100	PCF2110	PCF2111	PCF2112
• LCD segments	40	60	64	32
• LED segments	–	2	–	–
• Multiplex rate	1:2	1:2	1:2	1:1
• Word length	22 bit	34 bit	34 bit	34 bit

PACKAGE OUTLINES

PCF2100P: 28-lead DIL; plastic (SOT117).

PCF2110P:
PCF2111P: 40-lead DIL; plastic (SOT129).
PCF2112P:

PCF2100T: 28-lead mini-pack; plastic (SO28; SOT136A).

PCF2110T:
PCF2111T: 40-lead mini-pack; plastic (VSO40; SOT158A).
PCF2112T:

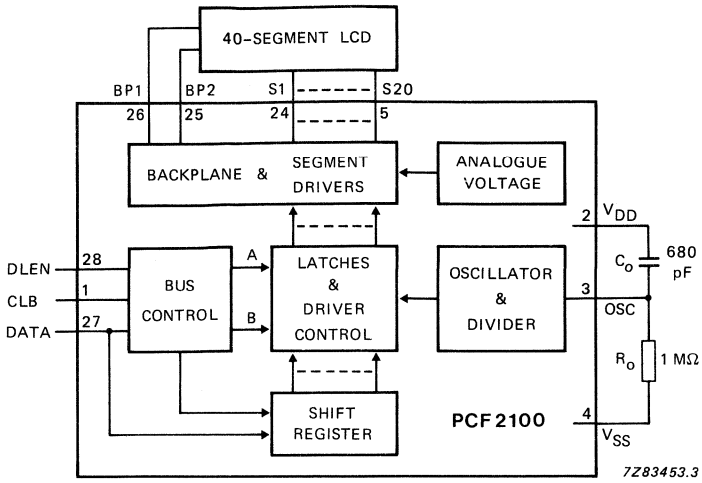


Fig. 1 Block diagram; PCF2100

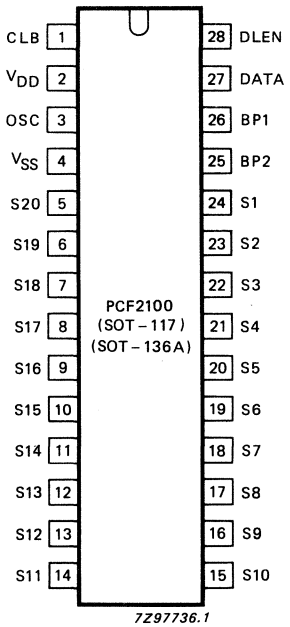


Fig. 2 Pinning diagram; PCF2100

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)
3	OSC	oscillator input
27	DATA	data line (CBUS)
28	DLEN	data line enable (CBUS)

Outputs

5 to 24	S20 to S1	LCD driver outputs
25	BP2	backplane drivers (commons of LCD)
26	BP1	backplane drivers (commons of LCD)

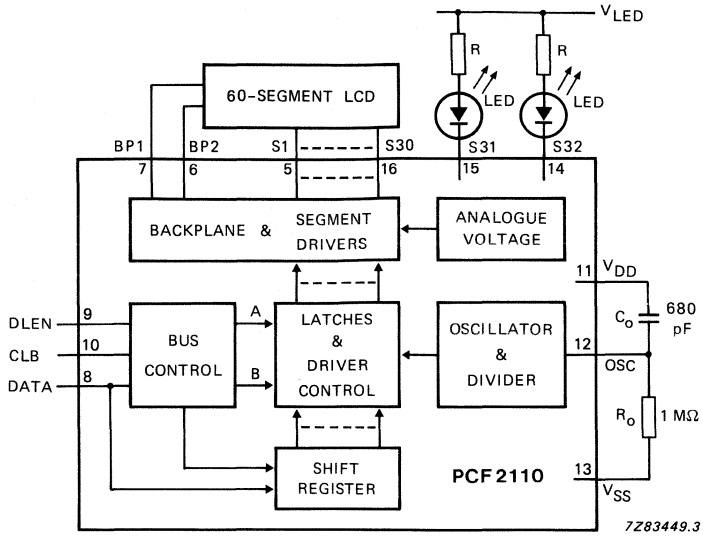


Fig. 3 Block diagram; PCF2110 (SOT-129).

DEVELOPMENT DATA

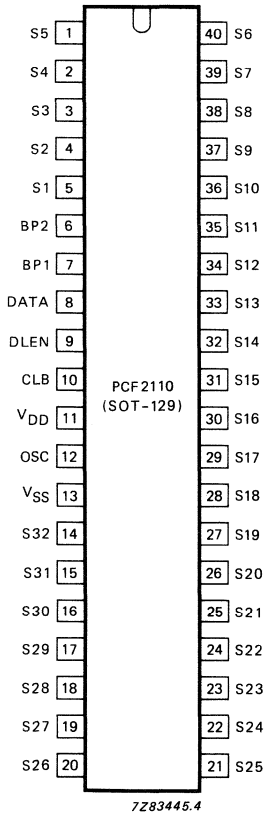


Fig. 4 Pinning diagram; PCF2110

PINNING (SOT-129)

Supply

11	V_{DD}	positive supply
13	V_{SS}	negative supply

Inputs

8	DATA	data line	CBUS
9	DLEN	data line enable	CBUS
10	CLB	clock burst	CBUS
12	OSC	oscillator input	

Outputs

1 to 5	S5 to S1	LCD driver outputs
6	BP2	backplane drivers (commons of LCD)
7	BP1	backplane drivers (commons of LCD)
14	S32	LED driver outputs
15	S31	LED driver outputs
16 to 40	S30 to S6	LCD driver outputs

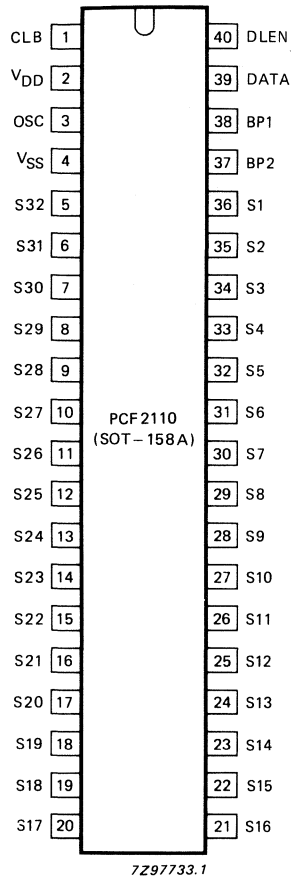


Fig. 5 Pinning diagram; PCF2110

PINNING (SOT-158A)

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)
3	OSC	oscillator input
39	DATA	data line (CBUS)
40	DLEN	data line enable (CBUS)

Outputs

5	S32	LED driver outputs
6	S31	LED driver outputs
7 to 36	S30 to S1	LCD driver outputs
37	BP2	backplane drivers (commons of LCD)
38	BP1	backplane drivers (commons of LCD)

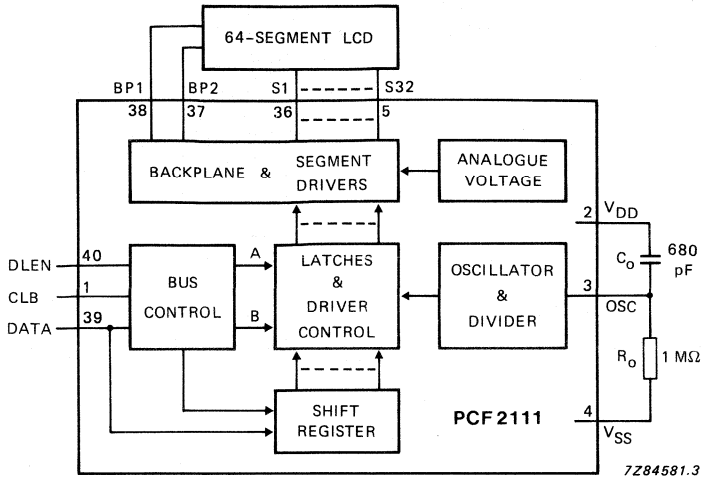


Fig. 6 Block diagram; PCF2111

DEVELOPMENT DATA

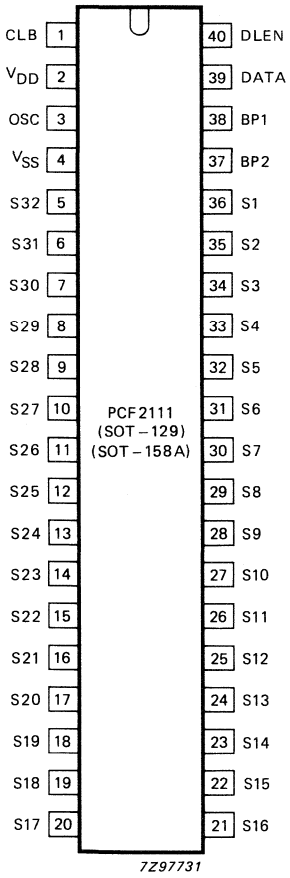


Fig. 7 Pinning diagram; PCF2111

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)	
3	OSC	oscillator input	
39	DATA	data line	} CBUS
40	DLEN	data line enable	} CBUS

Outputs

5 to 36	S32 to S1	LCD driver outputs
38	BP1	} backplane drivers
37	BP2	} (commons of LCD)

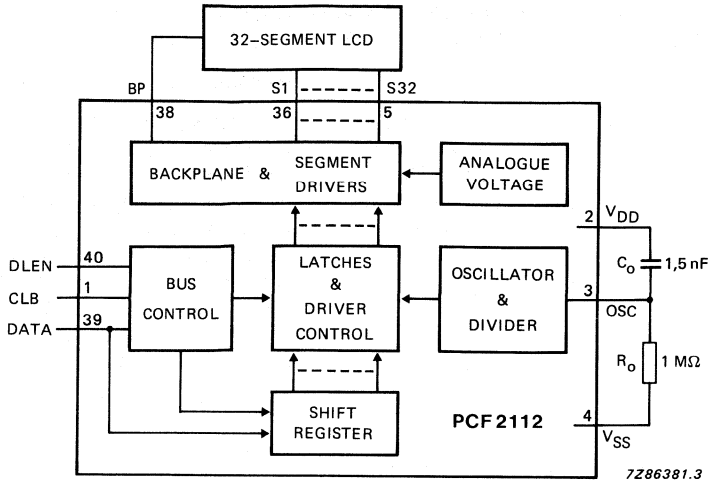


Fig. 8 Block diagram; PCF2112

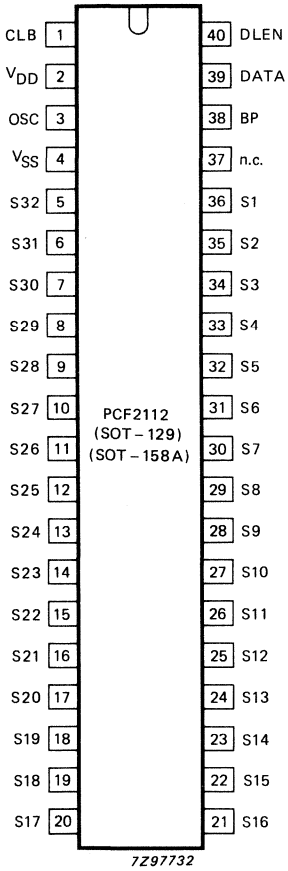


Fig. 9 Pinning diagram; PCF2112

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)
3	OSC	oscillator input
39	DATA	data line (CBUS)
40	DLEN	data line enable (CBUS)

Outputs

5 to 36	S32 to S1	LCD driver outputs
38	BP	backplane driver (common of LCD)
37	n.c.	not connected

Single-chip 8-bit microcontroller PCF84CXXXA Family

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATASHEET

INTRODUCTION

This datasheet describes the shared properties of the PCF84CXXXA family of microcontrollers and its quickly growing number of derivative microcontrollers. For a particular microcontroller, this datasheet should be read in conjunction with the individual datasheet of the specific device.

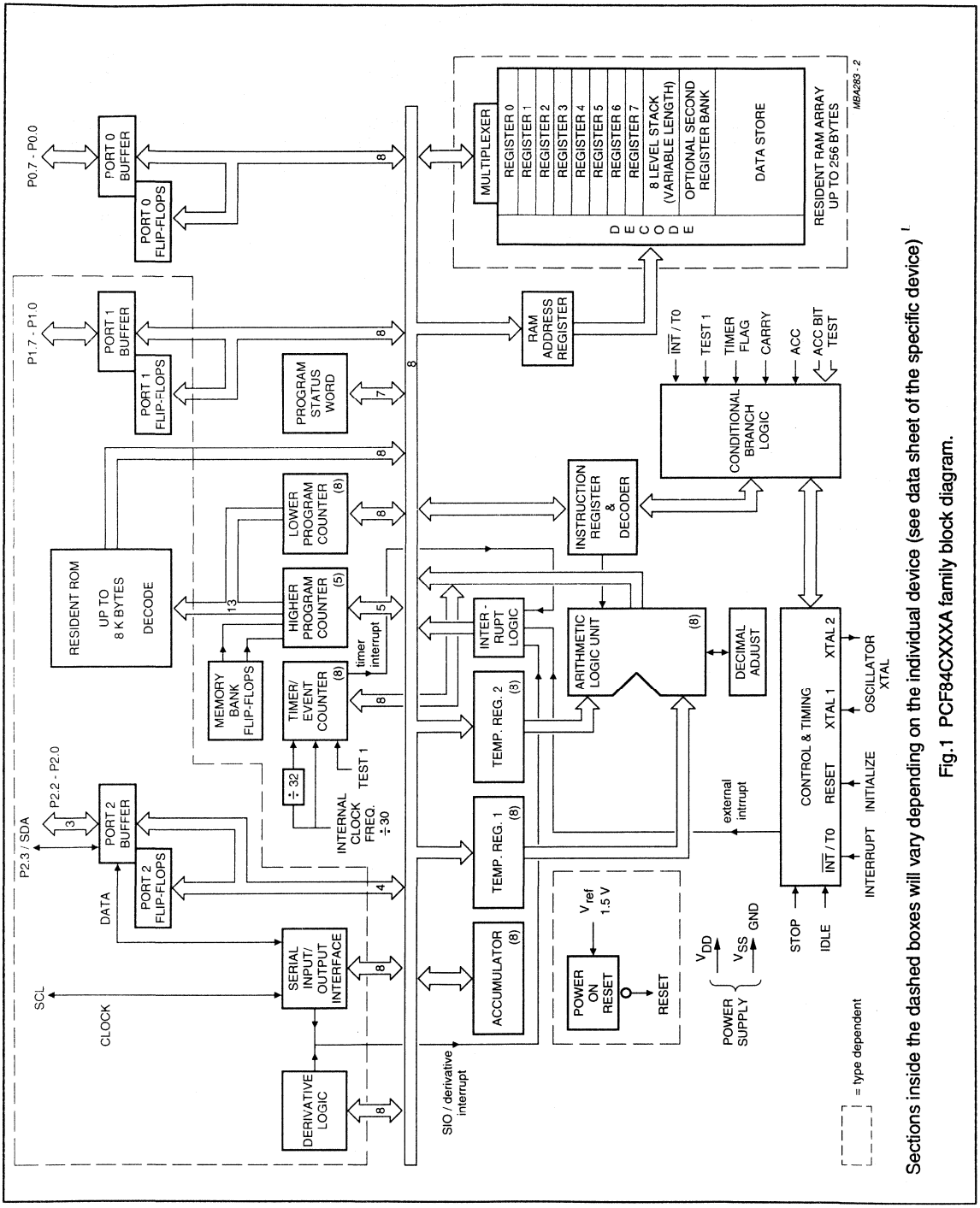
FEATURES

- 8-bit CPU, ROM, RAM, I/O all in one package
- Up to 8K ROM bytes
- Up to 256 RAM bytes
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 8 or more quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- 3 single-level vectored interrupts: external, timer/event counter, SIO/derivative
- Two test inputs, one of which also serves as the external interrupt input
- Serial I/O interface (some devices only)
- Power-on-reset, stop and idle modes
- Supply range V_{DD}: 2.5 V to 6 V
- Clock frequency: 1 MHz to 16 MHz
- Operating temperature range: –40 °C to +85 °C
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

The PCF84CXXXA family of microcontrollers provide up to 8k bytes of program memory and up to 256 bytes of RAM. All devices include flexible I/O ports, an 8-bit programmable timer/event counter and a choice of single-level vectored interrupts. The instruction set is based on that of the well-known MAB8048. Being similar to the MAB8400 family of NMOS controllers, some devices can serve as CMOS replacements, especially where the lower power consumption and higher speed provide advantages.

A range of prototyping devices with external program memory and 'piggy backs', as well as emulation probes and prototyping systems are available.



Sections inside the dashed boxes will vary depending on the individual device (see data sheet of the specific device) [1]

Fig.1 PCF84CXXXA family block diagram.

Telecom Microcontroller

PCF84C21A, PCF84C41A, PCF84C81A

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC03 OR DATASHEET

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead package
- 2k ROM bytes, 64 RAM bytes (PCF84C21A)
- 4k ROM bytes, 128 RAM bytes (PCF84C41A)
- 8k ROM bytes, 256 RAM bytes (PCF84C81A)
- Serial I/O interface with multi-master capability
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O Port lines
- High sink current capability on the 8 lines of Port 1
- 8-bit programmable timer/event counter 1
- 3 single-level vectored interrupts: external, 8-bit programmable timer/event counter 1, SIO
- Two test inputs, one of which also serves as the external interrupt input
- Stop and Idle modes
- Positive supply V_{DD}: 2.5 V to 5.5 V
- Clock frequency: 1 MHz to 16 MHz - Operating temperature range: –40 °C to 85 °C
- Manufactured in silicon gate CMOS process

GENERAL DESCRIPTION

This data sheet details the specific properties of the PCF84C21A, PCF84C41A and PCF84C81A. The shared characteristics of the PCF84CXXXA family of microcontrollers are described in the PCF84CXXXA family data sheet, which should be read in conjunction with this publication.

The PCF84C21A, PCF84C41A and PCF84C81A are general purpose CMOS microcontrollers with 2k, 4k and 8k bytes of program memory and 64, 128 and 256 bytes of RAM, respectively. In addition to 20 I/O port lines, the microcontrollers provide an on-chip serial I/O interface. This two-line serial bus extends the microcontroller capabilities when implemented with the powerful I²C bus devices of the PCF85XX, PCD33XX and "Clips" peripheral families. These include liquid crystal display drivers, telecom circuits, AD/DA converters, clock/calendar circuits, EEPROM and RAM. The instruction set is based on that of the MAB8048 and is software compatible with the PCF84CXXXA family.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF84C21AP	28	DIL	plastic	SOT117
PCF84C41AP	28	DIL	plastic	SOT117
PCF84C81AP	28	DIL	plastic	SOT117
PCF84C21AT	28	mini-pack	plastic	SOT136A
PCF84C41AT	28	mini-pack	plastic	SOT136A
PCF84C81AT	28	mini-pack	plastic	SOT136A

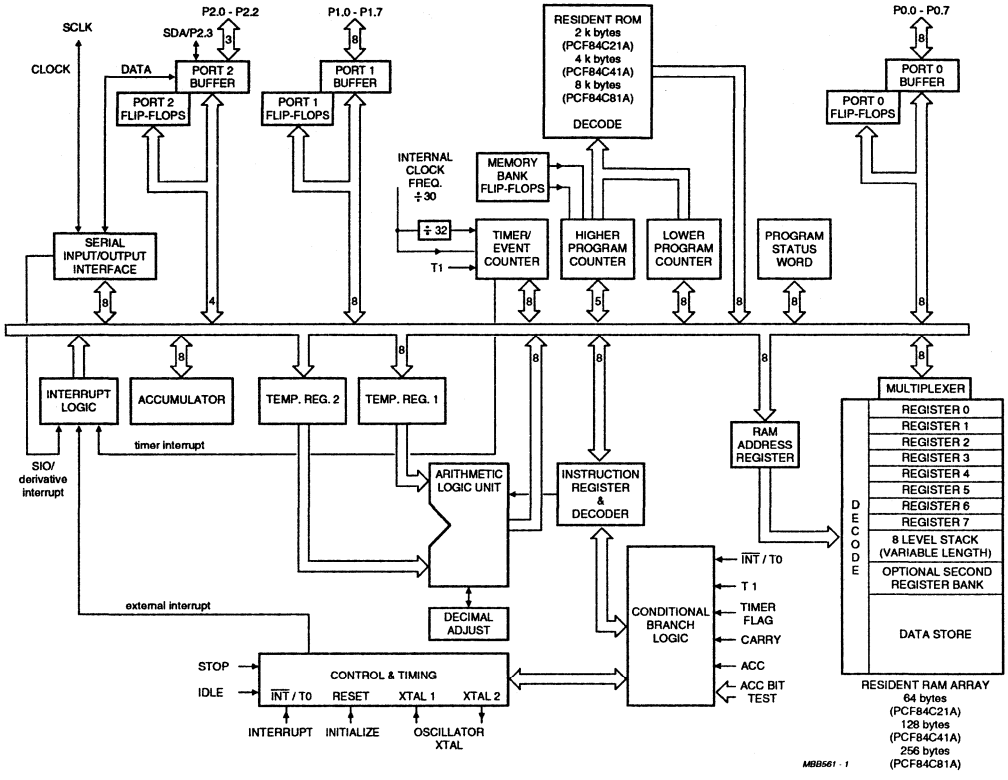


Fig.1 PCF84C21A/41A/81A block diagram.

8-Bit Microcontroller

PCF84C12A, PCF84C22A, PCF84C42A

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATASHEET

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 20-lead package
- 1k ROM bytes (PCF84C12A)
- 2k ROM bytes (PCF84C22A)
- 4k ROM bytes (PCF84C42A)
- 64 RAM bytes
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 13 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- Two single-level vectored interrupts: external, 8-bit programmable timer/event counter 1
- Two test inputs, one of which also serves as the external interrupt input
- Stop and idle modes
- Logic supply V_{DD}: 2.5 V to 5.5 V
- Clock frequency: 1 MHz to 16 MHz - Operating temperature range: –40 °C to 85 °C
- Manufactured in silicon gate CMOS process

GENERAL DESCRIPTION

This data sheet details the specific properties of the PCF84C12A, PCF84C22A and PCF84C42A. The shared characteristics of the PCF84CXXXA family of microcontrollers are described in the PCF84CXXXA family data sheet, which should be read in conjunction with this publication.

The PCF84C12A, PCF84C22A and PCF84C42A are general purpose CMOS microcontrollers with 1k, 2k and 4k bytes of program memory, respectively. They include 64 bytes of RAM and 13 I/O port lines. The instruction set is based on that of the MAB8048 and is software compatible with the PCF84CXXXA family.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF84C12AP/22AP/42AP	20	DIL	plastic	SOT146
PCF84C12AT/22AT/42AT	20	mini-pack	plastic	SOT163A

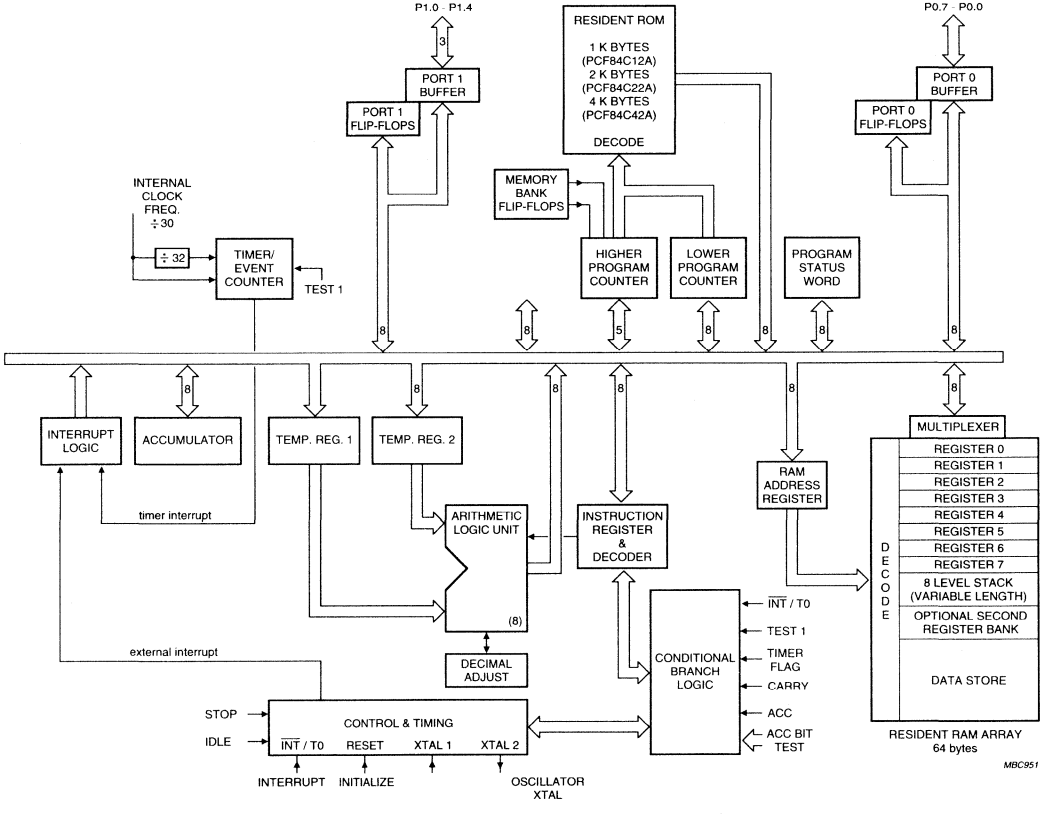


Fig.1 PCF84C12A/22A/42A Block diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATASHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 32 I/O LINES

DESCRIPTION

The PCF84C85 microcontroller is manufactured in CMOS, and is designed to be an efficient controller as well as an arithmetic processor. The instruction set is based on that of the MAB8048 and is software compatible with the 84CXXX family. The PCF84C85 has two additional derivative ports and the microcontroller has bit handling abilities and facilities for both binary and BCD arithmetic.

For detailed information see the 84CXXX family specification.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 40-lead DIL or mini-pack package
- 8 K ROM
- 256 RAM bytes
- 32 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- I^2C hardware interface for two-line serial data transfer (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Clock frequency 100 kHz to 10 MHz
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single supply voltage from 2,5 V to 5,5 V
- STOP and IDLE mode
- Power-on-reset circuit
- Operating temperature range: −40 to +85 °C

PACKAGE OUTLINES

PCF84C85P: 40-lead DIL; plastic (SOT129).
PCF84C85T: 40-lead; mini-pack (VSO40; SOT158A).

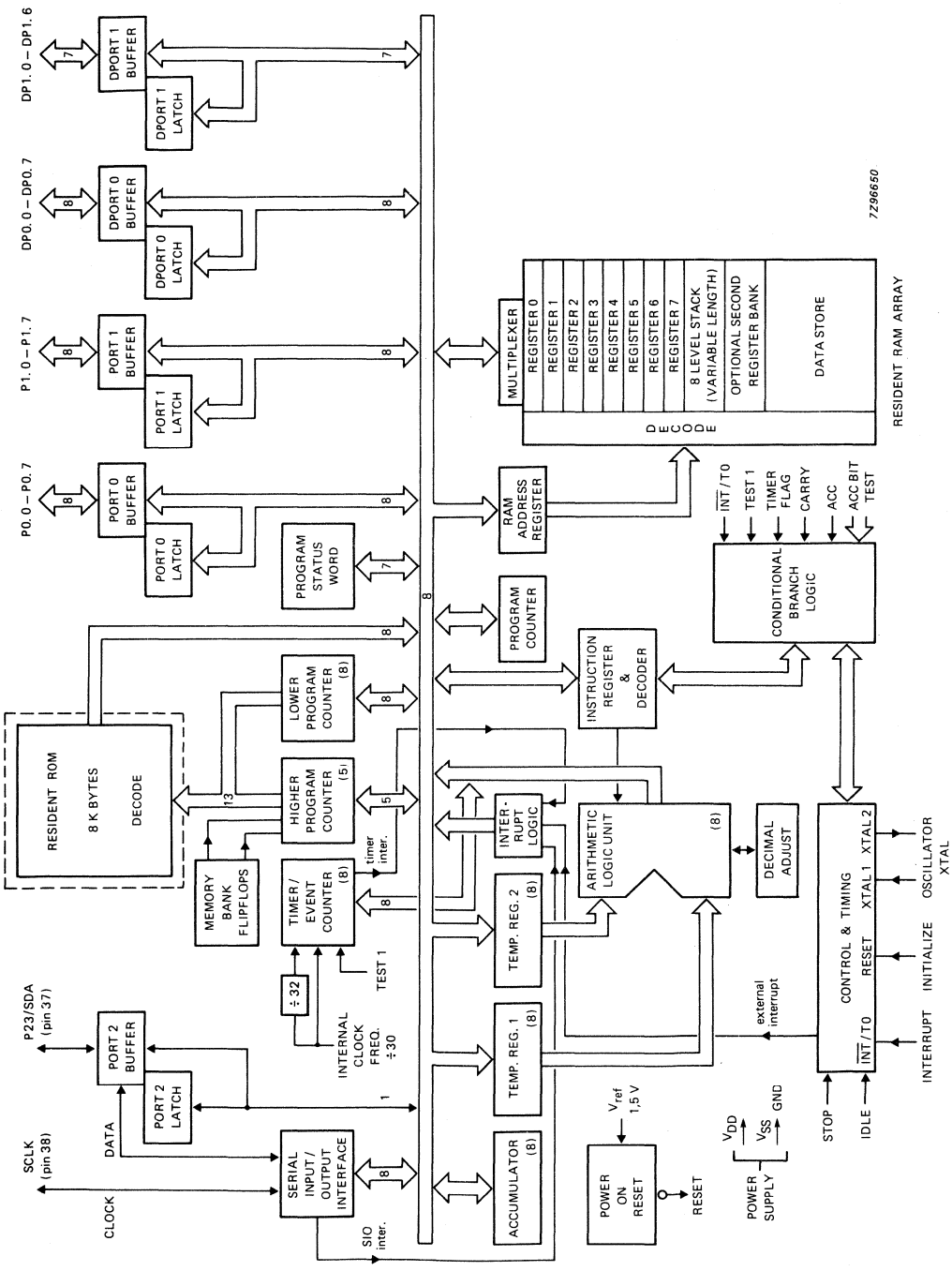


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATASHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 8 BYTES EEPROM

DESCRIPTION

An advanced CMOS process is used to manufacture the PCF84C121. The PCF84C121 has 13 quasi-bidirectional I/O port lines, three single-level vectored interrupts (one external and two timer), 8 bytes of EEPROM, two 8-bit timer counters and on-chip clock oscillator and clock circuits.

This efficient microcontroller also performs well as an arithmetic processor. The PCF84C121 is pin- and instruction set compatible with the PCF84C12. The PCF84C121 has bit handling abilities and facilities for both binary and BCD arithmetic.

This microcontroller is a member of the 84CXXX family. For detailed information, consult the 84CXXX family specification.

Features

- 8-bit CPU, ROM, RAM, EEPROM, I/O in a single 20-lead DIL or SO package
- 1 K x 8 ROM
- 64 x 8 RAM
- 8 x 8 EEPROM, designed for 10000 erase/write cycles per byte minimum
- 2 timers (8-bit programmable)
- 13 quasi-bidirectional I/O port lines
- 3 single-level, vectored interrupts: external, Timer 1 and Timer 2
- Two test inputs: one of which is also the external interrupt input
- 8-bit programmable timer/event counter
- Clock frequency range: 450 kHz to 10 MHz
- Over 80 instructions (similar to those of the MAB8048) all of 1 or 2 cycles
- Single supply voltage
- STOP and IDLE modes
- Power-on-reset circuit
- Operating temperature range: −40 to +85 °C; 0 to +55 °C for programming

PACKAGE OUTLINES

PCF84C121P: 20-lead DIL; plastic (SOT146).
PCF84C121T: 20-lead mini-pack; plastic (SO20; SOT163A).

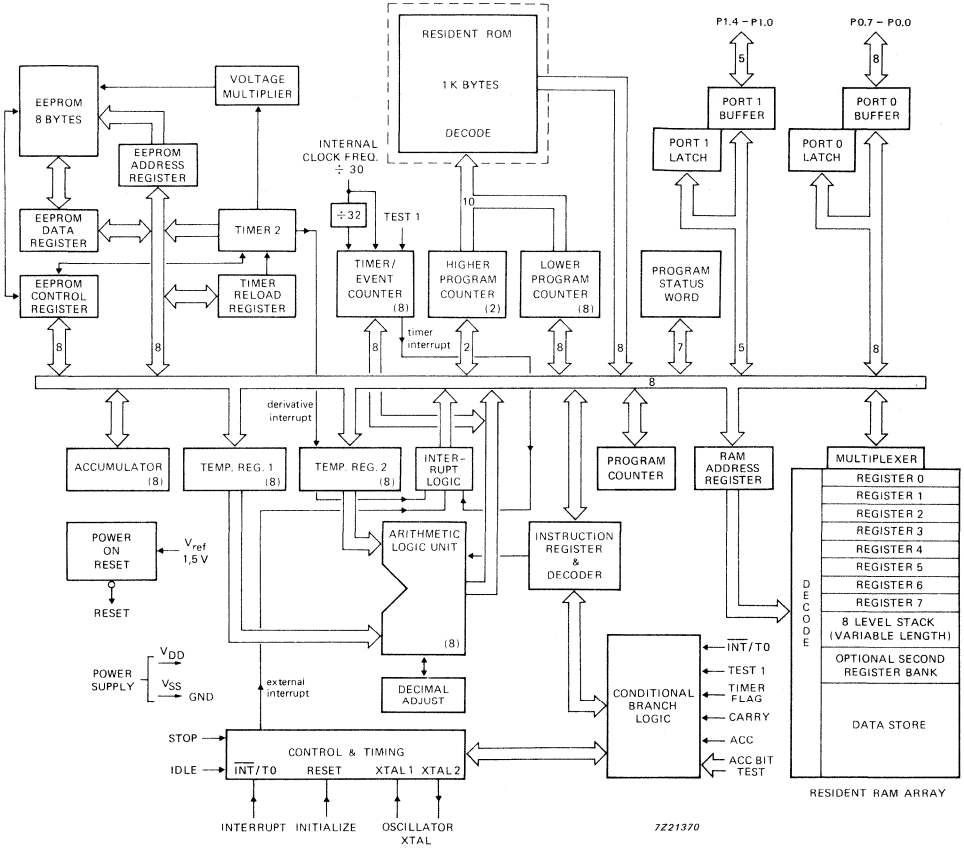


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATASHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH LCD DRIVER

GENERAL DESCRIPTION

The PCF84C230 is a single-chip 8-bit microcontroller manufactured in CMOS technology, and is a member of the 84CXXX family. For detailed information see the 84CXXX family specification.

The PCF84C230 provides 12 general purpose quasi-bidirectional I/O port lines, a line that is directly testable (T1), one external interrupt line, and an LCD driver for up to 64 graphic elements. The IC is mask-programmable and is designed for control in small systems with LCD displays.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 40-lead DIL package
- 2 K ROM bytes
- 64 RAM bytes
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- 12 quasi-bidirectional I/O port lines
- Configuration of I/O lines can be individually selected by mask (pull-up, open drain, push-pull)
- LCD drive circuit with 16 segment drivers and selectable backplane drive configuration: static or 2/3/4 multiplex, to drive up to 64 graphic elements
- LCD possible during STOP mode
- Single-level vectored interrupts: external and timer/event counter
- Power-on reset and low voltage detector
- Single supply voltage from 2.5 V to 5.5 V
- STOP and IDLE modes
- Clock frequency 100 kHz to 10 MHz
- Operating ambient temperature range: −40 to + 85 °C

PACKAGE OUTLINES

40-lead DIL; plastic (SOT129).
40-lead mini-pack; plastic (VS040; SOT158A).

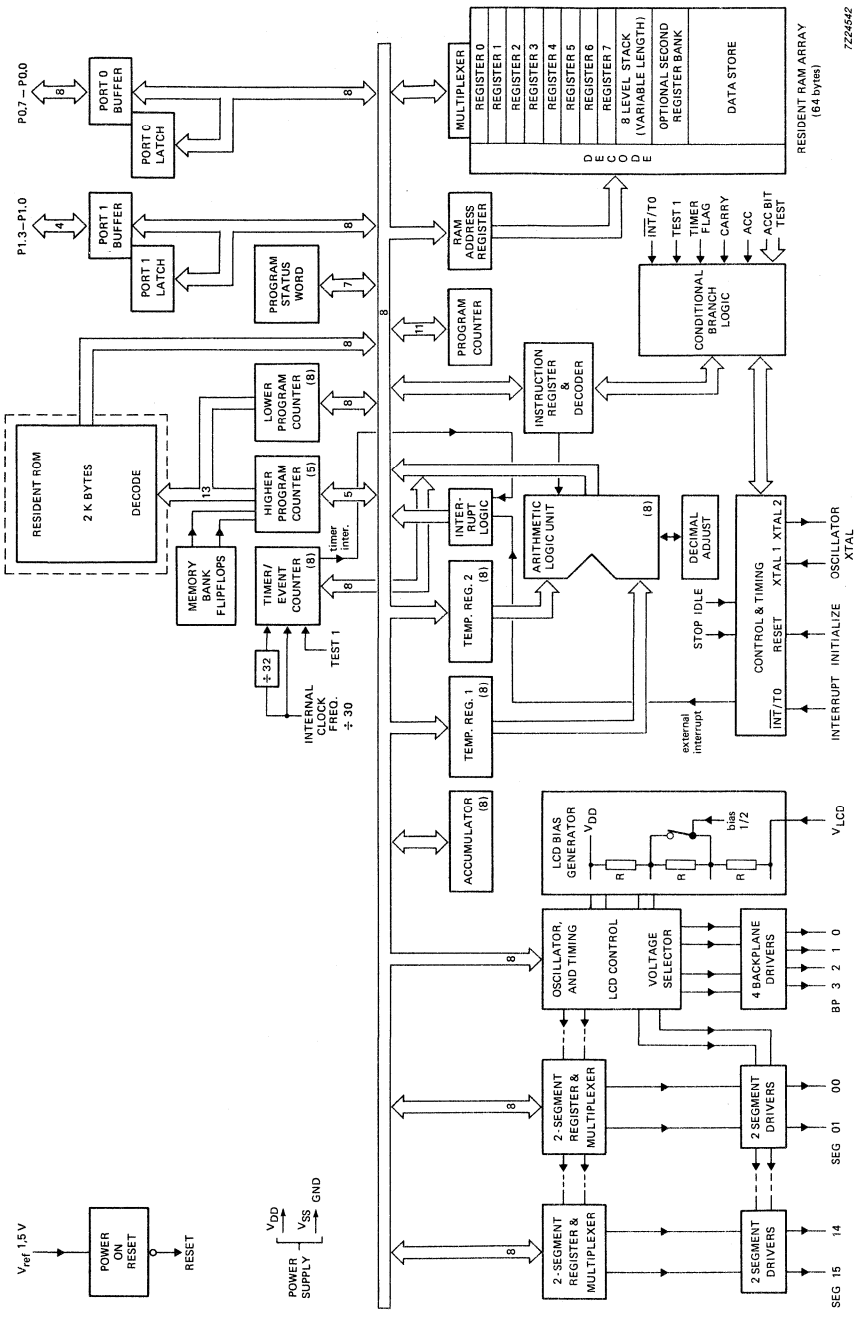


Fig.1 Block diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATASHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH LCD DRIVER

DESCRIPTION

The PCF84C430 microcontroller is a derivative of the 84CXXX family of microcontrollers and is manufactured in CMOS technology. For detailed information see the 84CXXX family specification.

The PCF84C430 contains a PCF84CXX core CPU and is completely software compatible. In addition, the PCF84C430 contains an LCD driver supporting four back planes and a maximum driving capacity of up to 96 segments.

The PCF84C430 has 16 quasi-bidirectional I/O port lines, plus a derivative 8-bit port, a serial I/O interface, a single-level vectored interrupt circuit, an 8-bit timer/event counter and on-board clock oscillator and clock circuits.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 64-lead QFP package
- 4 K ROM bytes
- 128 RAM bytes
- On-chip LCD driver with 24 outputs (max. 96 segments)
- LCD multiplexing rates at 1:1 (static), 1:2, 1:3 and 1:4
- Low-power oscillator for LCD driver during STOP mode
- 25 quasi-bidirectional I/O port lines are configured as two 8-bit ports, a 1-bit port (shared with SDA) and an 8-bit derivative port
- Two test inputs: one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- I^2C-bus hardware interface for serial data transfer on two separate lines
- 8-bit programmable timer/event counter
- Clock frequency 100 kHz to 10 MHz
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single supply voltage from 2,5 V to 5,5 V ($V_{SS} \leqslant V_{LCD} < V_{DD}$)
- STOP and IDLE mode
- Power-on-reset circuit
- Operating temperature range: −40 to + 85 °C

PACKAGE OUTLINE

PCF84C430H: 64-lead quad flat-pack; plastic (SOT208).

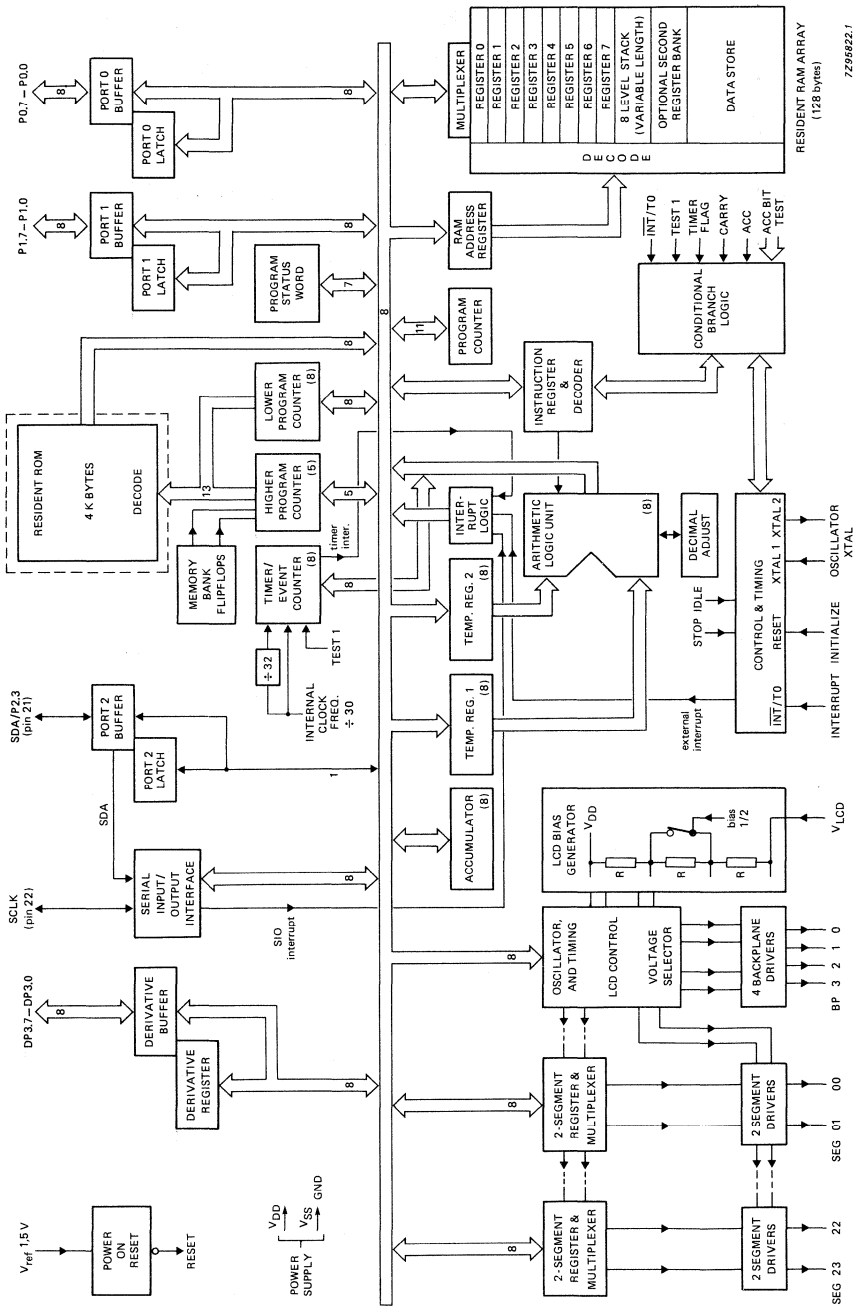


Fig. 1 Block diagram; PCF84C430.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2,5 V to 6 V power supply range
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40-lead plastic mini-pack (VSO-40; SOT-158A)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8566P: 40-lead DIL; plastic (SOT129).
PCF8566T: 40-lead mini-pack (VSO40; SOT158A).

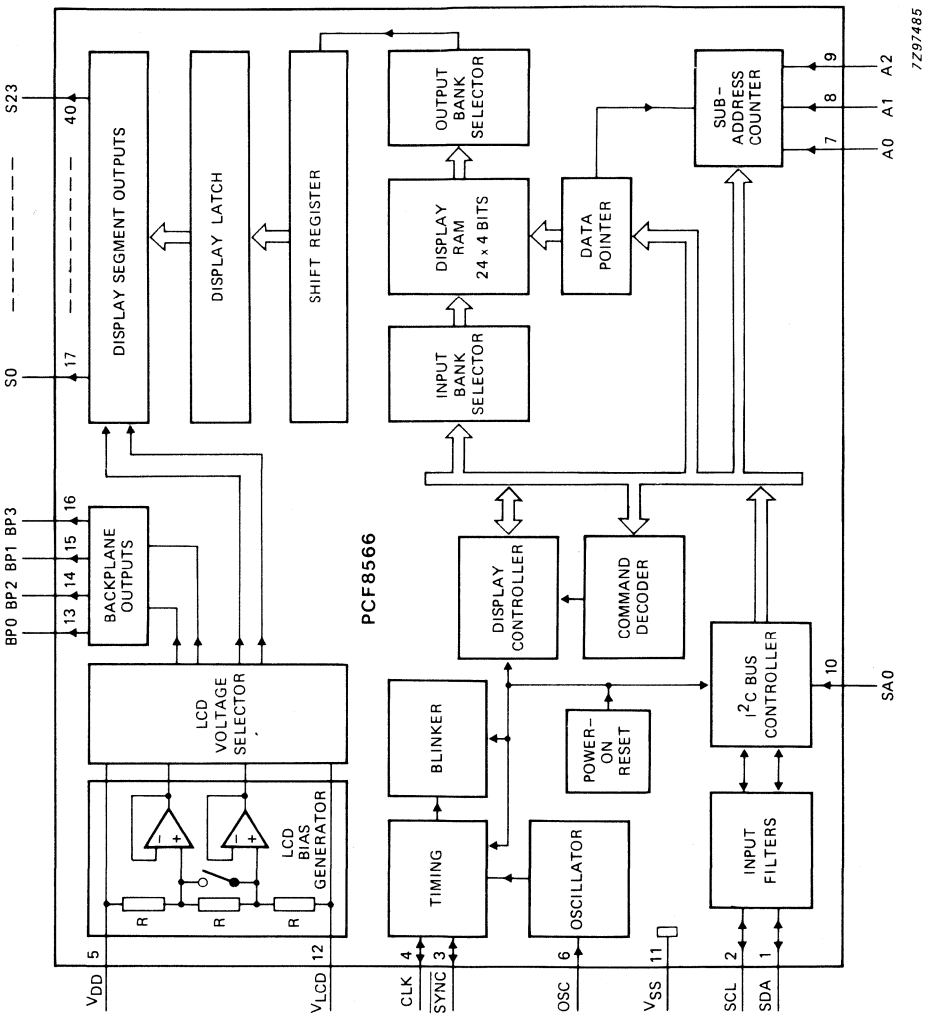


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

LCD DIRECT MODE DRIVER WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8567C is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing and hardware subaddressing..

Features

- Direct drive mode with up to 32 LCD-segment drive capability per device
- Operating supply voltage: 2.5 to 6 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- May be used as I²C-bus output expander
- System expansion up to 256 segments
- Power-on reset blanks display

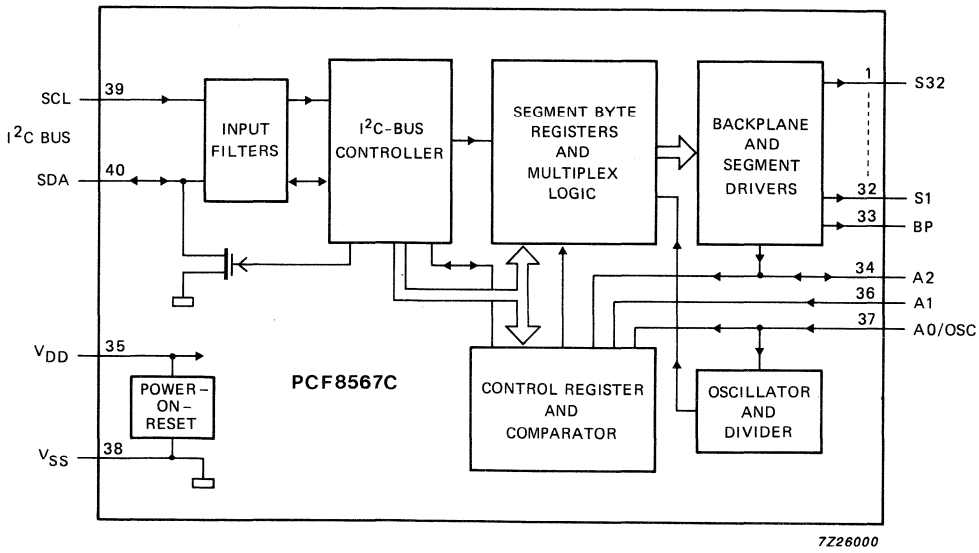


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8567CP: 40-lead DIL; plastic (SOT129).
PCF8567CT: 40-lead mini-pack; plastic (VSO40; SOT158A).

LCD row driver for dot matrix displays

PCF8568

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

FEATURES

- Single chip LCD row driver with 16 outputs
- Low power consumption
- Selectable multiplex rate 1:8, 1:16, 1:24, 1:32
- Cascadable to 1:24 or 1:32 multiplex rates
- Internally generated intermediate LCD bias voltages
- LCD column bias voltages available at pins VO3 and VO4
- Minimizes display system power requirements
- On-chip oscillator, requires only one external resistor
- Power-on reset blanks display
- Logic voltage range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9.0 V
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring
- Available in 28-lead plastic DIL or space saving mini-pack
- Compatible with chip-on-glass technology.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- General instrumentation
- Consumer products.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range	+2.5	-	+6.0	V
V_{LCD}	LCD supply voltage range voltage	V_{DD} −9	-	V_{DD} −3.5	V
I_{DD2}	supply current with internal clock (R_{OSC} = 330 kΩ)	-	67	150	µA
T_{amb}	operating ambient temperature range	−40	-	+85	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8568P	28	DIL	plastic	SOT117
PCF8568T	28	SO28	plastic	SOT136A
PCF8568U/7	(28 pads)	die: bumped chip on tape	-	-

GENERAL DESCRIPTION

The PCF8568 is a low power LCD row driver, designed to drive dot matrix graphic displays with multiplex rates of 1:8 or 1:16. The device has 16 row outputs. Two devices may be cascaded to drive displays with multiplex rates of 1:24 or 1:32. The PCF8568 is optimised for use with the PCF8569 and PCF8579 LCD dot matrix column drivers. Intermediate LCD bias voltages are internally generated. LCD column bias voltages are available at pins VO3 and VO4 for connection to the column drivers. The PCF8568 is compatible with most microcontrollers and communicates via a two- line bidirectional bus (I²C).

LCD row driver for dot matrix displays

PCF8568

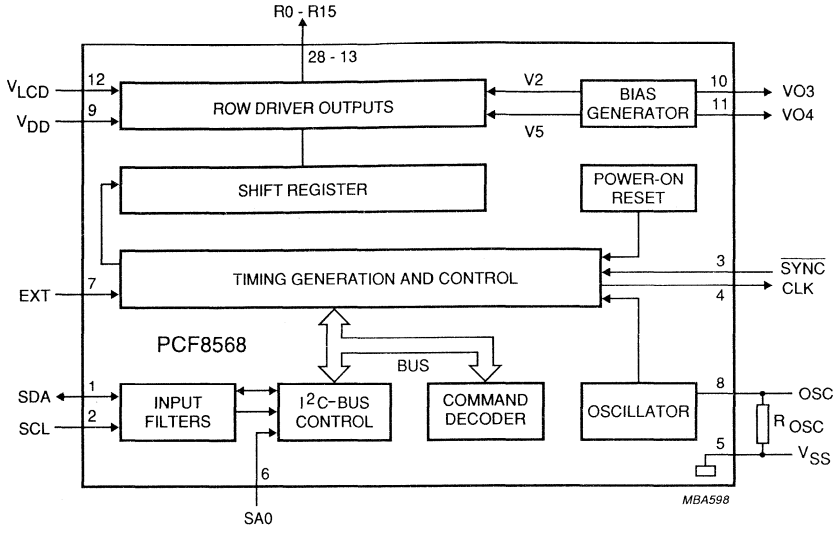


Fig.1 Block diagram.

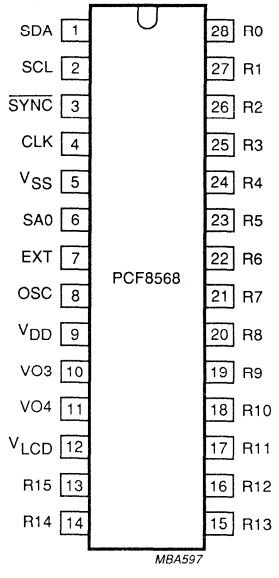


Fig.2 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus serial data line
SCL	2	I²C-bus serial clock line
$\overline{SYNC}$	3	cascade synchronization input/output
CLK	4	clock output
V_{SS}	5	ground (logic)
SA0	6	I²C-bus slave address input (bit 0)
EXT	7	external clock select pin
OSC	8	oscillator or external clock input pin
V_{DD}	9	positive supply voltage
VO3	10	LCD bias voltage output (V3)
VO4	11	LCD bias voltage output (V4)
V_{LCD}	12	LCD supply voltage
R15 to R0	13 to 28	LCD row driver outputs

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

LCD COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8569 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8 or 1:16. The device has 40 outputs and can drive 16 x 40 dots in a 16 row multiplexed LCD. Up to 16 PCF8569s can be cascaded and up to 32 devices may be used on the same I^2C-bus (using the two slave addresses). The device is optimized for use with the PCF8568/78/79 family of LCD row/column drivers. Together the PCF8568, PCF8578 and PCF8569 form a general LCD dot matrix driver chip set, capable of driving displays of up to 20 480 dots. The PCF8569 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

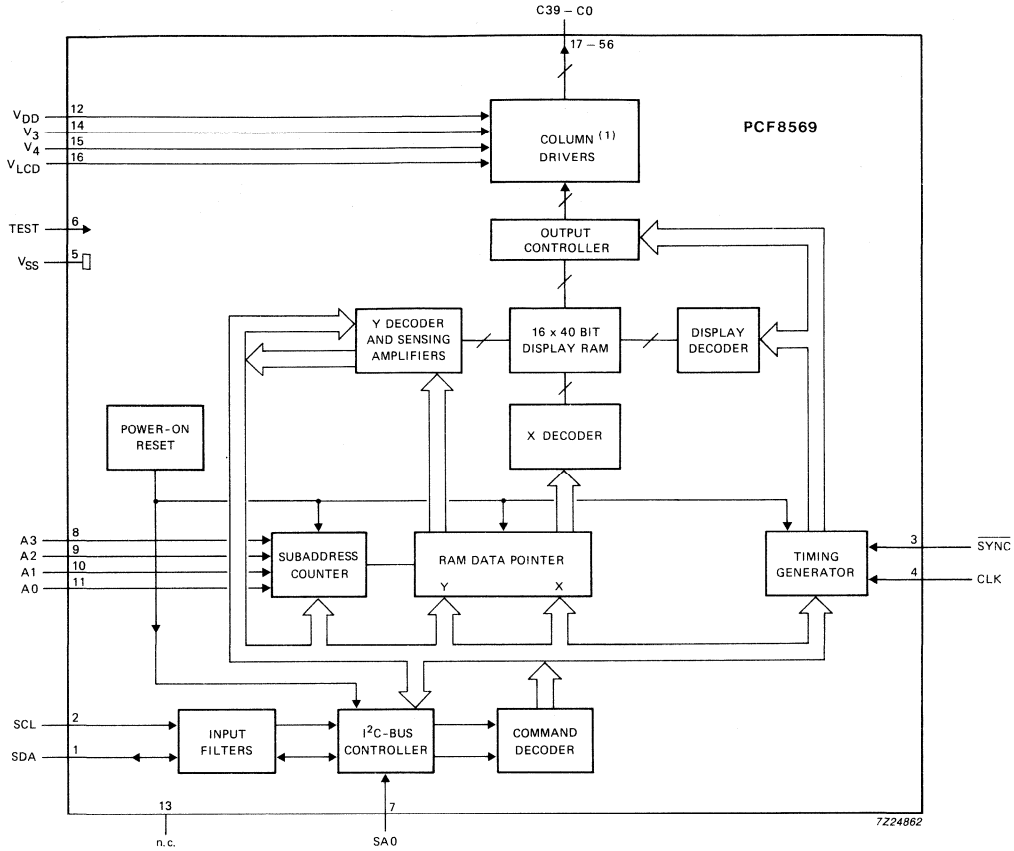
- LCD column driver
- Used in conjunction with the PCF8568 or PCF8578, this device forms part of a chip set capable of driving up to 20 480 dots.
- 40 column outputs
- Selectable multiplex rates; 1:8 or 1:16
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications
- 640-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack or 64-lead tab module

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8569T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8569V: 64-lead tape-automated-bonding (tab) module (SOT267).



(1) LCD voltage levels, all other blocks operate at logic levels.

Fig.1 Block diagram (pin numbers shown for VSO56; SOT190).

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC10 OR DATASHEET

128 X 8-BIT/256 X 8-BIT STATIC RAMS WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8570, PCF8570C and PCF8571 are low-power static CMOS RAMs. The PCF8570 and PCF8570C are organized as 256 words by 8-bits and the PCF8571 is organized as 128 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1 and A2 are used for hardware address, allowing the use of up to eight devices connected to the bus without additional hardware. For system expansion over 8 devices the PCF8570/71 can be used in conjunction with the PCF8750C which has an alternative slave address for memory extension up to 16 devices.

Features

- Operating supply voltage 2.5 V to 6 V
- Low data retention voltage min. 1.0 V
- Low standby current max. 15 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony — RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications)
- Radio and television — channel presets
- Video cassette recorder — channel presets
- General purpose — RAM expansion for the microcontroller families MAB8400, PCF84CXX and most other microcontrollers

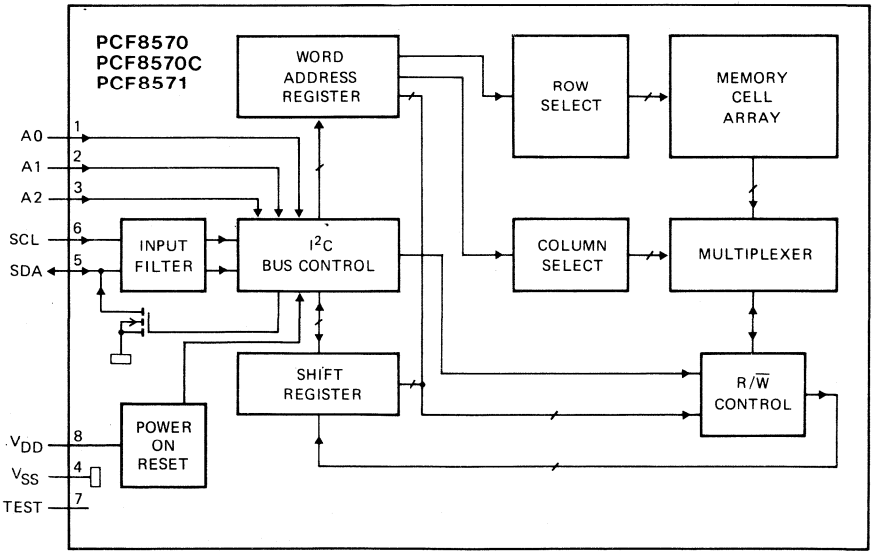


Fig.1 Block diagram. 7Z90775.3

PACKAGE OUTLINES

PCF8570/PCF8570C/PCF8571/P: 8-lead DIL; plastic (SOT97).
PCF8570/PCF8570C/PCF8571/T: 8-lead mini-pack (SO8L; SOT176C)

PINNING

1 to 3	A0 to A2	address inputs
4	V_{SS}	negative supply
5	SDA	serial data line (I²C-bus)
6	SCL	serial clock line (I²C-bus)
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Figs 12 and 13)
8	V_{DD}	positive supply

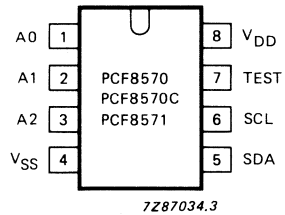


Fig.2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.8	+8.0	V
Input voltage range	V_I	−0.8	V_{DD} + 0.8	V
DC input current	$\pm I_I$	–	10	mA
DC output current	$\pm I_O$	–	10	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; $\pm I_{SS}$	–	50	mA
Total power dissipation	P_{tot}	–	300	mW
Power dissipation per output	P_O	–	50	mW
Operating ambient temperature range	T_{amb}	−40	+85	°C
Storage temperature range	T_{stg}	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC03 OR DATASHEET

CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCF8573 is a low threshold, CMOS circuit that functions as a real time clock/calendar with an I^2C-bus interface.
The IC incorporates an addressable time counter and an addressable alarm register for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred via a serial two-line bidirectional bus (I^2C). Back-up for the clock during supply interruptions is provided by a 1.2 V nickel cadium battery. The time base is generated from a 32.768 kHz crystal-controlled oscillator.

Features

- Serial input/output I^2C-bus interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32.768 kHz)

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range					
clock (pin 16 to pin 15)	$V_{DD}-V_{SS1}$	1.1	–	6.0	V
I^2C interface (pin 16 to pin 8)	$V_{DD}-V_{SS2}$	2.5	–	6.0	V
Crystal oscillator frequency	f_{osc}	–	32.768	–	kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT38).
PCF8573T: 16-lead mini-pack; plastic (SO16L; SOT162A).

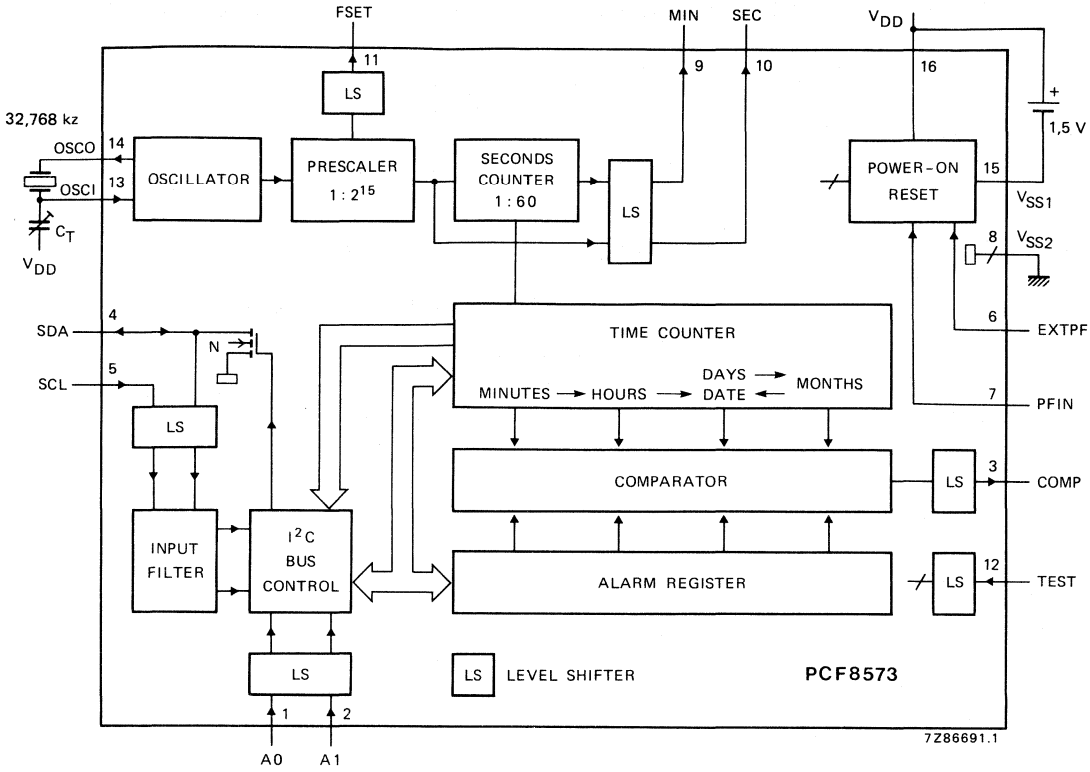


Fig.1 Block diagram.

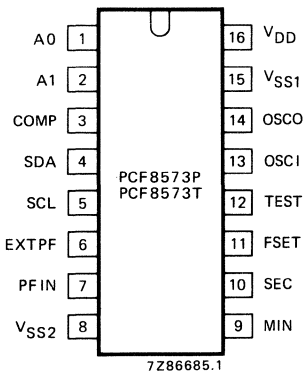


Fig.2 Pinning diagram.

PINNING

1	A0	address input	
2	A1	address input	
3	COMP	comparator output	
4	SDA	serial data line	I^2C-bus
5	SCL	serial clock line	I^2C-bus
6	EXTPF	enable power fail flag input	
7	PFIN	power fail flag input	
8	V_{SS2}	negative supply 2 (I^2C interface)	
9	MIN	one pulse per minute output	
10	SEC	one pulse per second output	
11	FSET	oscillator tuning output	
12	TEST	test input; must be connected to V_{SS2} when not in use	
13	OSCI	oscillator input	
14	OSCO	oscillator input/output	
15	V_{SS1}	negative supply 1 (clock)	
16	V_{DD}	common positive supply	

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC03 OR DATASHEET

REMOTE 8-BIT I/O EXPANDER FOR I²C-BUS

GENERAL DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF84CXX microcontroller families via the two-line serial bidirectional bus (I²C).
It can also interface microcomputers without a serial interface to the I²C-bus (as a slave function only).
The device consists of an 8-bit quasi-bidirectional port and an I²C interface.
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I²C-bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I²C-bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and the PCF8574A versions differ only in their slave address as shown in Fig.9.

Features

- Operating supply voltage — 2.5 V to 6 V
- Low stand-by current consumption — max. 10 μA
- Bidirectional expander
- Open drain interrupt output
- 8-bit remote I/O port for the I²C-bus
- Peripheral for the MAB8400 and PCF84CXX microcontroller families
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)

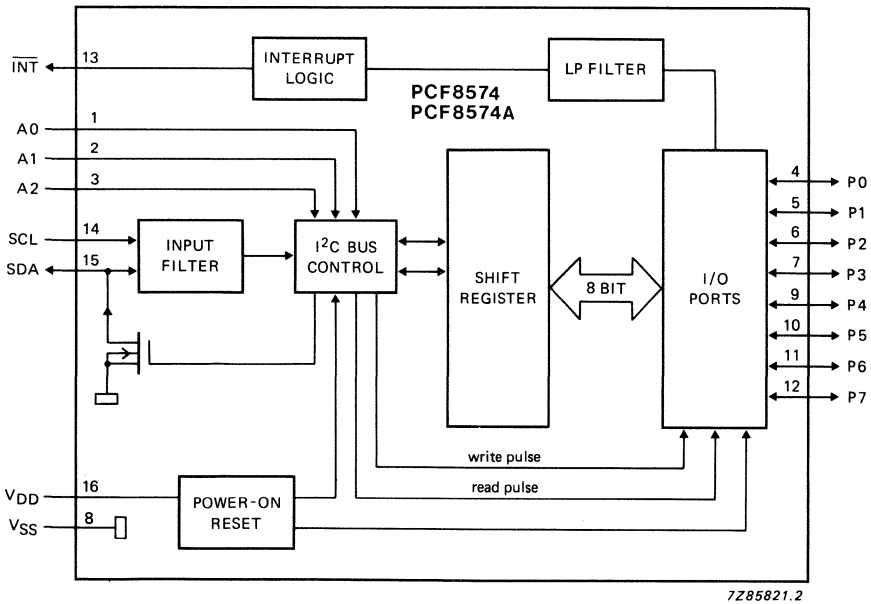


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8574P, PCF8574AP: 16-lead DIL; plastic (SOT38).
PCF8574T, PCF8574AT: 16-lead mini-pack; plastic (SO16L; SOT162A).

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with the 24-segment LCD driver PCF8566
- Optimized pinning for single plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic mini-pack (VSO56) or 64-lead tape-automated-bonding (TAB) module (SOT267A)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8576T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8576U: uncased chip in tray.
PCF8576U/10: chip-on-film frame carrier (FFC).
PCF8576V: 64-lead tape-automated-bonding module (SOT267A).

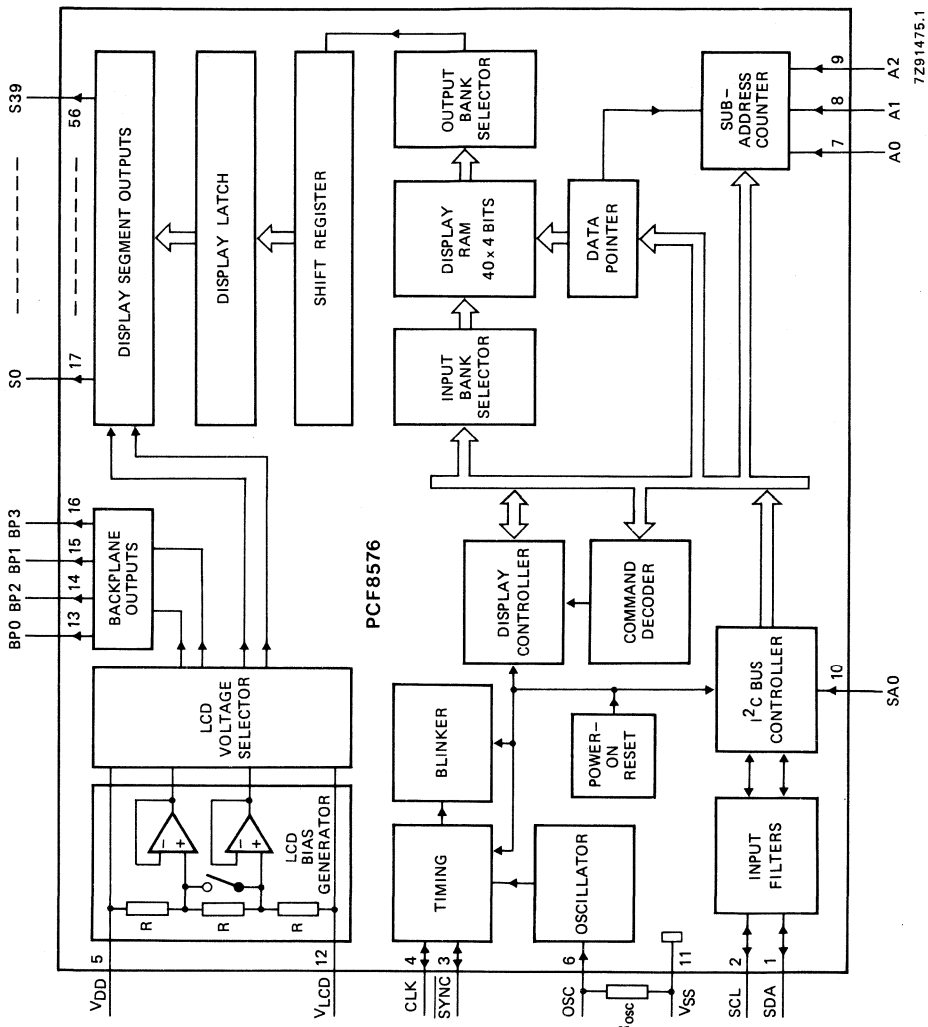


Fig.1 Block diagram; VSO56; SOT190.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

LCD DIRECT / DUPLEX DRIVER WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8577 is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing and display memory switching (direct drive mode).
The PCF8577 and PCF8577C differ from the PCF8577A and PCF8577CA only in their slave addresses.
The PCF8577C/77CA is a low-voltage version of the PCF8577/77A.

Features

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Opering supply voltage:
  PCF8577/77A: 2.5 to 9 V
  PCF8577C/77CA: 2.5 to 6 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- Display memory switching in direct drive mode
- May be used as I²C-bus output expander
- System expansion up to 256 segments (512 segments with PCF8577A/CA)
- Power-on reset blanks display

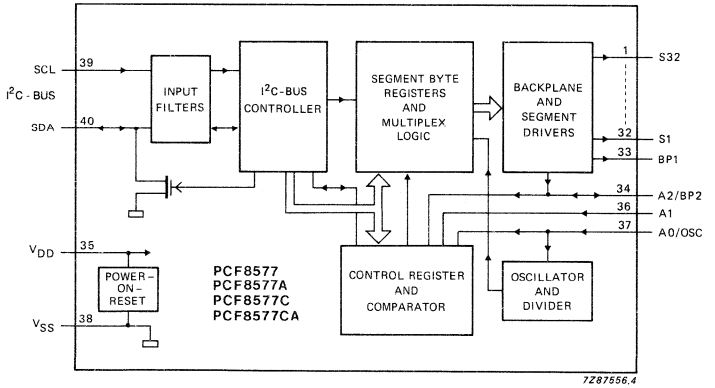


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8577P, PCF8577AP PCF8577CP, PCF8577CAP	40-lead DIL; plastic (SOT129).
PCF8577T, PCF8577AT PCF8577CT, PCF8577CAT	40-lead mini-pack; plastic (VSO40; SOT158A).
PCF8577T, PCF8577AT PCF8577CT, PCF8577CAT	in blister tape.
PCF8577U/5 PCF8577CU/5	wafer unsawn.
PCF8577U/10 PCF8577CU/10	chip on film-frame-carrier (FFC).

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

LCD ROW/COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8, 1:16, 1:24 or 1:32. The device has 40 outputs, of which 24 are programmable, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (40,960 dots possible)
- 40 driver outputs, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns
- Selectable multiplex rates; 1:8, 1:16, 1:24 or 1:32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8578T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8578V: 64-lead tape-automated-bonding module (SOT267A).
PCF8578U: chip with bumps on-tape.

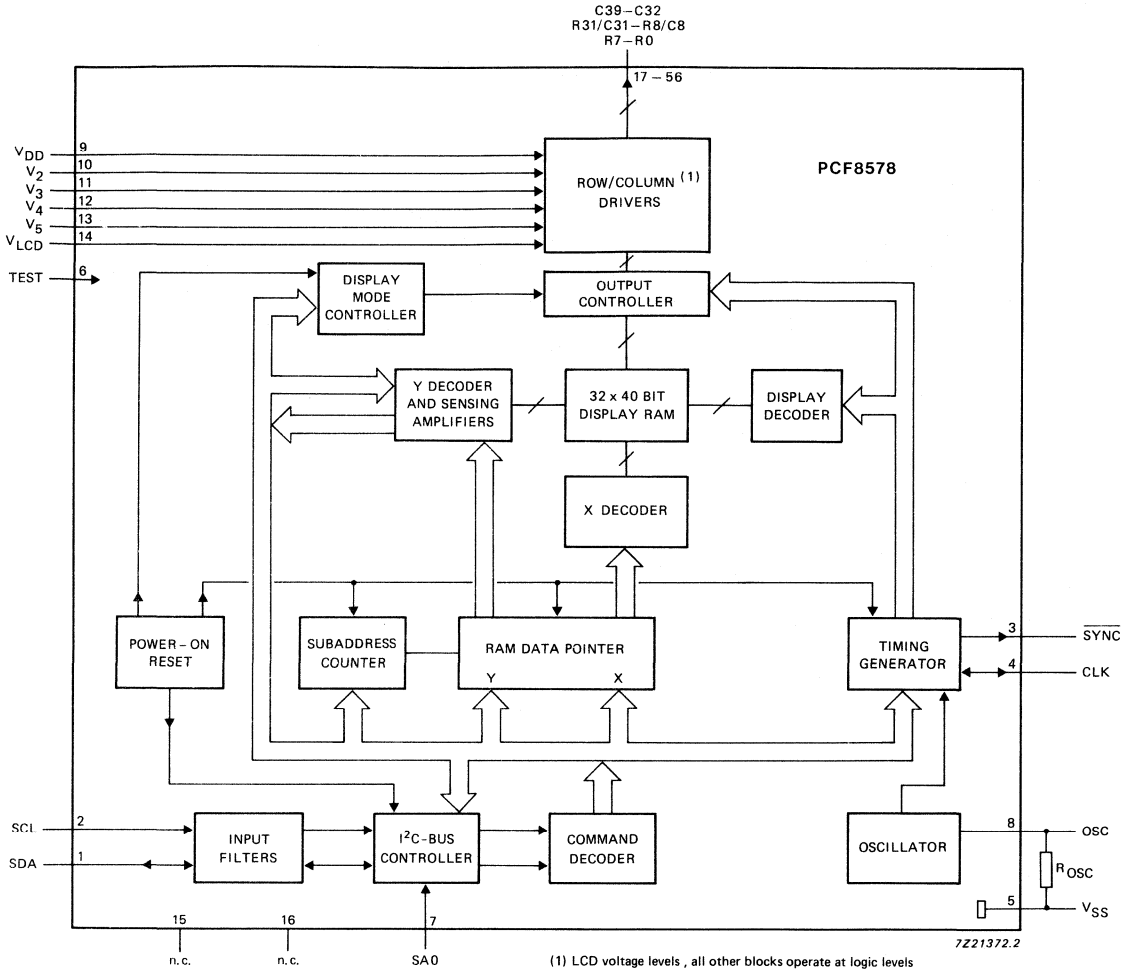


Fig.1 Block diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

LCD COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8, 1:16, 1:24 or 1:32. The device has 40 outputs and can drive 32 x 40 dots in a 32 row multiplexed LCD. Up to 16 PCF8579s can be cascaded and up to 32 devices may be used on the same I^2C-bus (using the two slave addresses). The device is optimized for use with the PCF8578 LCD row/column driver. Together these two devices form a general LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40,960 dots
- 40 column outputs
- Selectable multiplex rates; 1:8, 1:16, 1:24 or 1:32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8579T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8579V: 64-lead tape-automated-bonding module (SOT267A).
PCF8579U: chip with bumps on-tape.

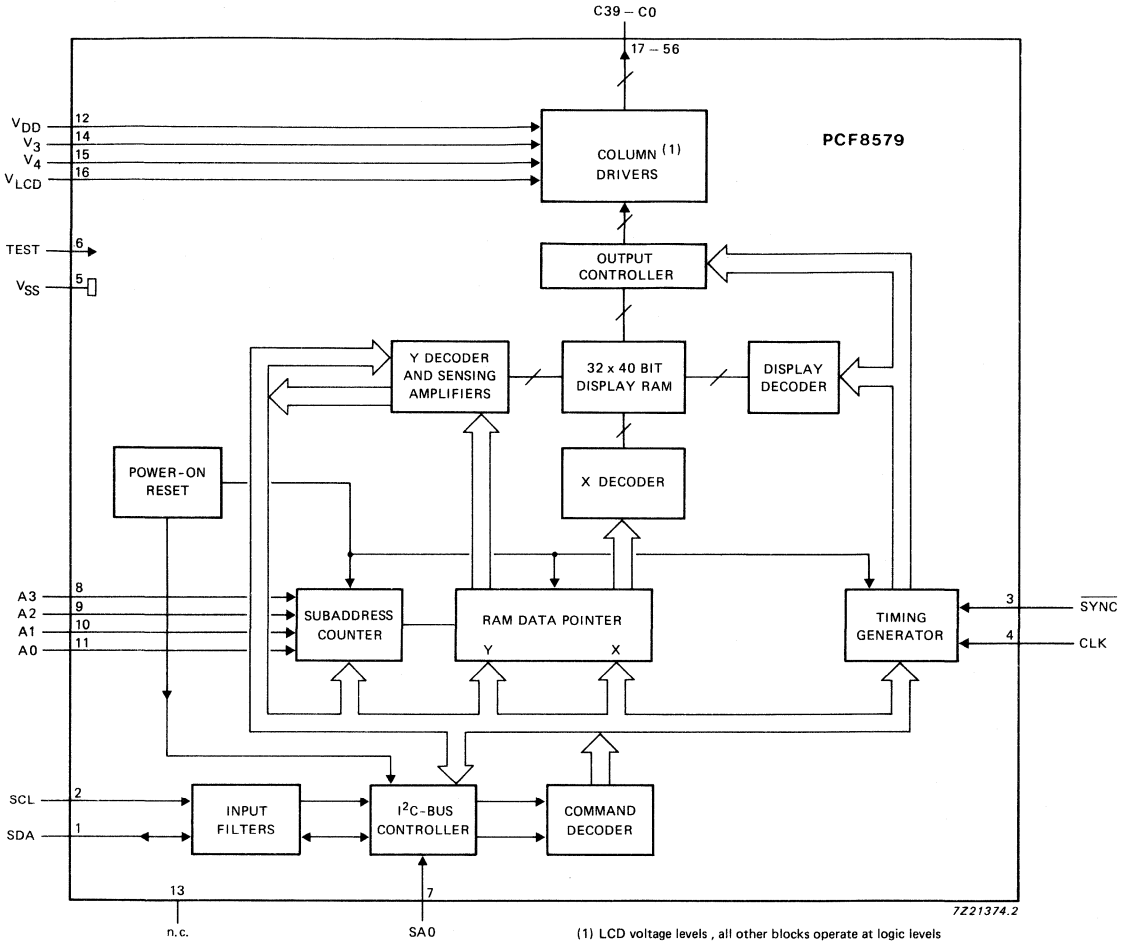


Fig.1 Block diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC10 OR DATASHEET

128 x 8-BIT EEPROM WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8581 and PCF8581C are low-power CMOS EEPROMs with standard and wide operating voltage:
4.5 to 5.5 V (PCF8581); 2.5 to 6.0 V (PCF8581C).

In the following text, the generic term "PCF8581" is used to refer to both types in all packages except where specified.

The PCF8581 is organized as 128 words by 8-bits.

Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. All bytes can be read in a single operation. Up to eight bytes can be written in one operation, reducing the total write time per byte. Three address pins A0, A1 and A2 are used to define the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

Features

- Operating supply voltage: 4.5 to 5.5 V (PCF8581); 2.5 to 6.0 V (PCF8581C)
- Integrated voltage multiplier and timer for writing (no external components required)
- Automatic erase before write
- Low standby current max. 10 μA
- Eight-byte page write mode
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Designed for 10 000 write cycles per byte minimum
- 10 years minimum non-volatile data retention
- Infinite number of read cycles
- Pin and address compatibility to PCF8570, PCF8571 and PCF8582

PACKAGE OUTLINES

PCF8581P/PCF8581CP: 8-lead DIL; plastic (SOT97).
PCF8581T/PCF8581CT: 8-lead mini-pack (SO8L; SOT176C).

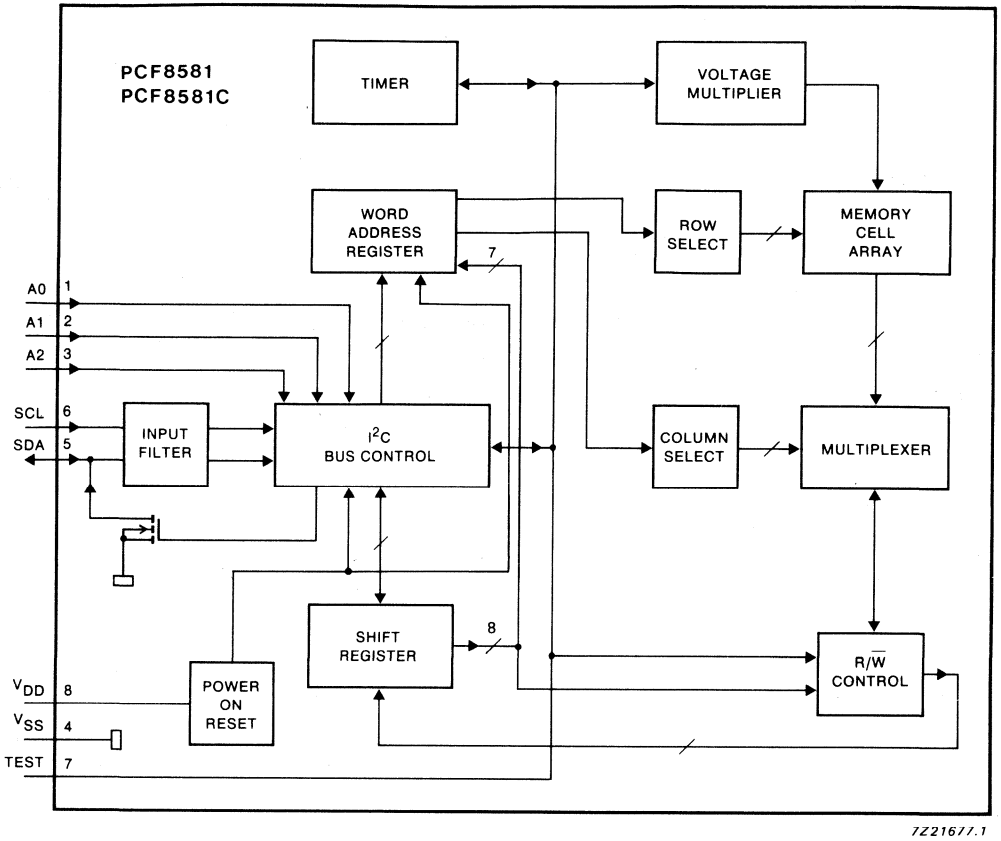


Fig.1 Block diagram.

Clock Calendar with 256 x 8-bit Static RAM

PCF8583

FEATURES

- I²C-bus interface operating supply voltage: 2.5 V to 6 V
- Clock operating supply voltage (0 to +70 °C): 1.0 V to 6.0 V
- Data retention voltage: 1.0 V to 6 V
- Operating current (f_{scl} = 0 Hz): max. 50 A
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Slave address, READ: A1 or A3, WRITE: A0 or A2.

GENERAL DESCRIPTION

The PCF8583 is a low power 2048-bit static CMOS RAM organized as 256 words by 8 bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. One address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware. The built-in 32.768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
V_{DD}	supply voltage operating range	I²C-bus active	2.5	6.0	V
V_{DD}	supply voltage operating range	I²C-bus inactive	1.0	6.0	V
I_{DD}	supply current operating mode	f_{scl} =100 kHz	-	200	µA
I_{DDO}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 5 V	-	50	µA
		f_{scl} = 0 Hz; V_{DD} = 1 V	-	10	µA
T_{amb}	operating ambient temperature range		–40	+85	°C
T_{stg}	storage temperature range		–65	+150	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8583P	8	DIL	plastic	SOT97
PCF8583T	8	mini-pack	plastic	SO8L; SOT176C

Clock Calendar with 256 x 8-bit Static RAM

PCF8583

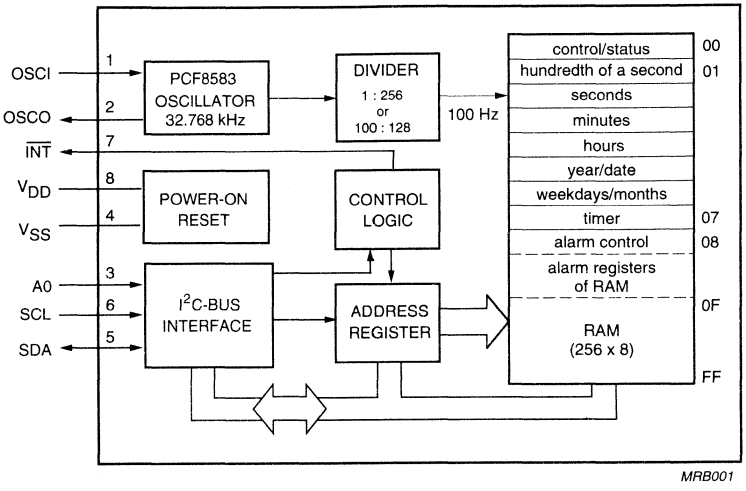


Fig.1 Block diagram.

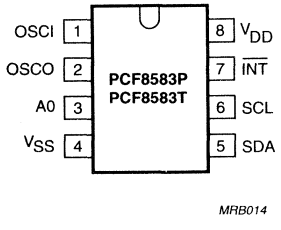


Fig.2 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input, 50 Hz or event-pulse input
OSCO	2	oscillator output
A0	3	address input
V_{SS}	4	negative supply
SDA	5	serial data line
SCL	6	serial clock line
$\overline{INT}$	7	open drain interrupt output (active LOW)
V_{DD}	8	positive supply

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC03 OR DATASHEET

8-BIT A/D AND D/A CONVERTER

GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I^2C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I^2C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I^2C bus.

Features

- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I^2C bus
- Address by 3 hardware address pins
- Sampling rate given by I^2C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P:16-lead DIL; plastic (SOT38).
PCF8591T:16-lead mini-pack; plastic (SO16L; SOT162A).

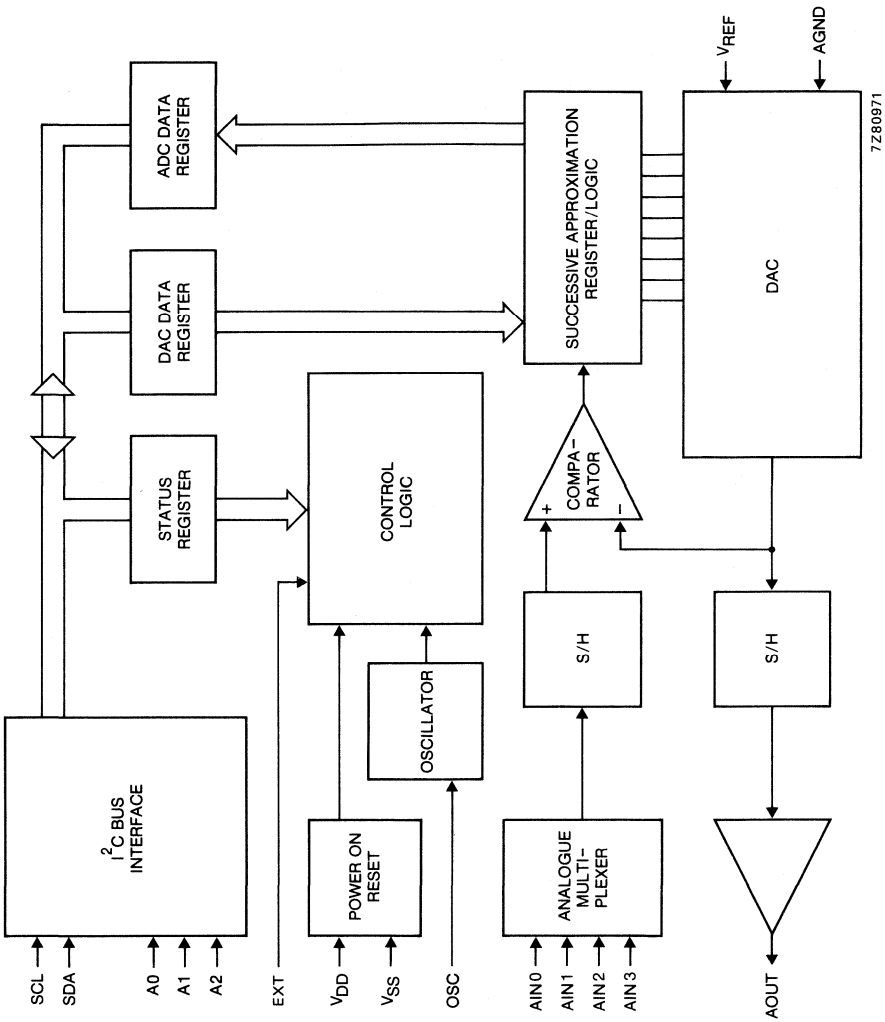


Fig. 1 Block diagram.

256 x 8-BIT CMOS EEPROMS with I²C-bus interface

PCx8582x-2 Family

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

FEATURES

- Non-volatile storage of 2 Kbits organized as 256 x 8-bits
- Only one power supply required
- On chip voltage multiplier
- Serial input/output bus (I²C)
- Low power CMOS; maximum active current 2 mA, maximum standby current 10 µA
- Power-on reset
- 10 years non-volatile data retention time
- Pin and address compatible to PCF8570, PCF8571, PCF8572 and PCF8581
- Write operations

  byte write mode

  8-byte page write mode (minimizes total write time per byte)
- Read operations

  sequential read and random read
- Extended supply voltage range (2.5 to 6.0 V)
- Internal timer for writing (no external components)
- High reliability by using a redundant storage code
- Endurance 100 k; T_{amb} = +85 °C

GENERAL DESCRIPTION

The 2 Kbit (256 x 8-bit) CMOS EEPROMS are floating gate electrically erasable programmable read only memories. By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability compared to conventional EEPROM memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to eight PCx8582x-2 devices can be connected to the I²C-bus.
Chip select is accomplished by the three address inputs.

Timing of the Erase/Write cycle is achieved internally, thus no external components are required. Pin 7 must be connected to either V_{DD} or left open-circuit.

An option exists for using an external clock for timing the length of an Erase/Write cycle.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive suppy voltage		2.5	–	6.0	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz				
		V_{DD} = 3 V	–	–	60	µA
		V_{DD} = 6 V	–	–	200	µA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz				
		V_{DD} = 3 V	–	–	0.5	mA
		V_{DD} = 6 V	–	–	2.0	mA
I_{DDO}	supply current STANDBY					
		V_{DD} = 3 V	–	–	3.5	µA
		V_{DD} = 6 V	–	–	10	µA

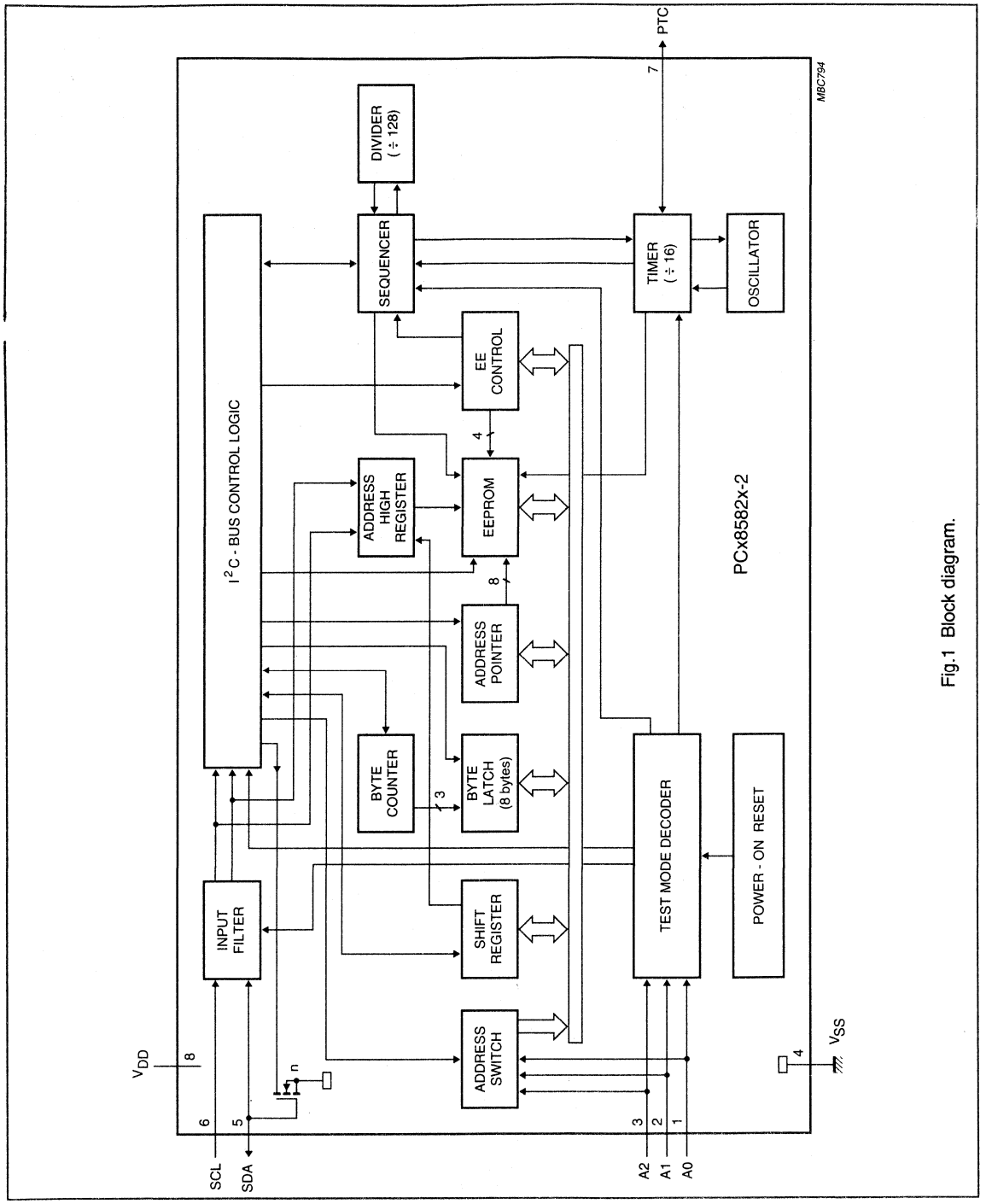


Fig.1 Block diagram.

512 x 8-bit CMOS EEPROMS with I²C-bus interface

PCx8594x-2 Family

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

FEATURES

- Low Power CMOS
  - maximum active current 2.5 mA
  - maximum standby current 10 µA
- Non-volatile storage of 4-Kbits organized as two pages
  - each 256 x 8-bits
- Only one power supply required
- On-chip voltage multiplier
- Serial input/output bus (I²C)
- Write operations
  - byte write mode
  - 8-byte page write mode (minimizes total write time per byte)
- Write-protection input
- Read operations
  - sequential read
  - random read
- Extended supply voltage range (2.5 to 6.0 V)
- Internal timer for writing (no external components)
- Power-on reset
- High reliability by using a redundant storage code (single bit error correction)
- Endurance
  - 100 k; T_{amb} = 85 °C
- 10 years non-volatile data retention time
- Pin and Address compatible to
  - PCx8582x-2 Family and PCx8589x2 Family

GENERAL DESCRIPTION

The PCx8594x-2 is a 4-Kbit (512 x 8-bit) floating gate electrically erasable programmable read only memory (EEPROM). By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability compared to conventional EEPROM memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip, using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to four PCx8594x-2 devices may be connected to the I²C-bus. Chip select is accomplished by two address inputs.

Timing of the Erase/Write cycle is done internally, thus no external components are required. Pin 7 must be connected to either V_{DD} or left open-circuit.

There is an option of using an external clock for timing the length of an Erase/Write cycle.

A write protection input (pin 1) allows disable of write-commands from the master by a hardware signal. When pin 1 is HIGH and one of the upper 256 EEPROM cells is addressed, then the data bytes will not be acknowledged by the PCx8594x-2 and the EEPROM contents are not changed.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCx8594x-2P	8	DIL	plastic	SOT97
PCx8594x-2T	8	SO8	plastic	SOT96A

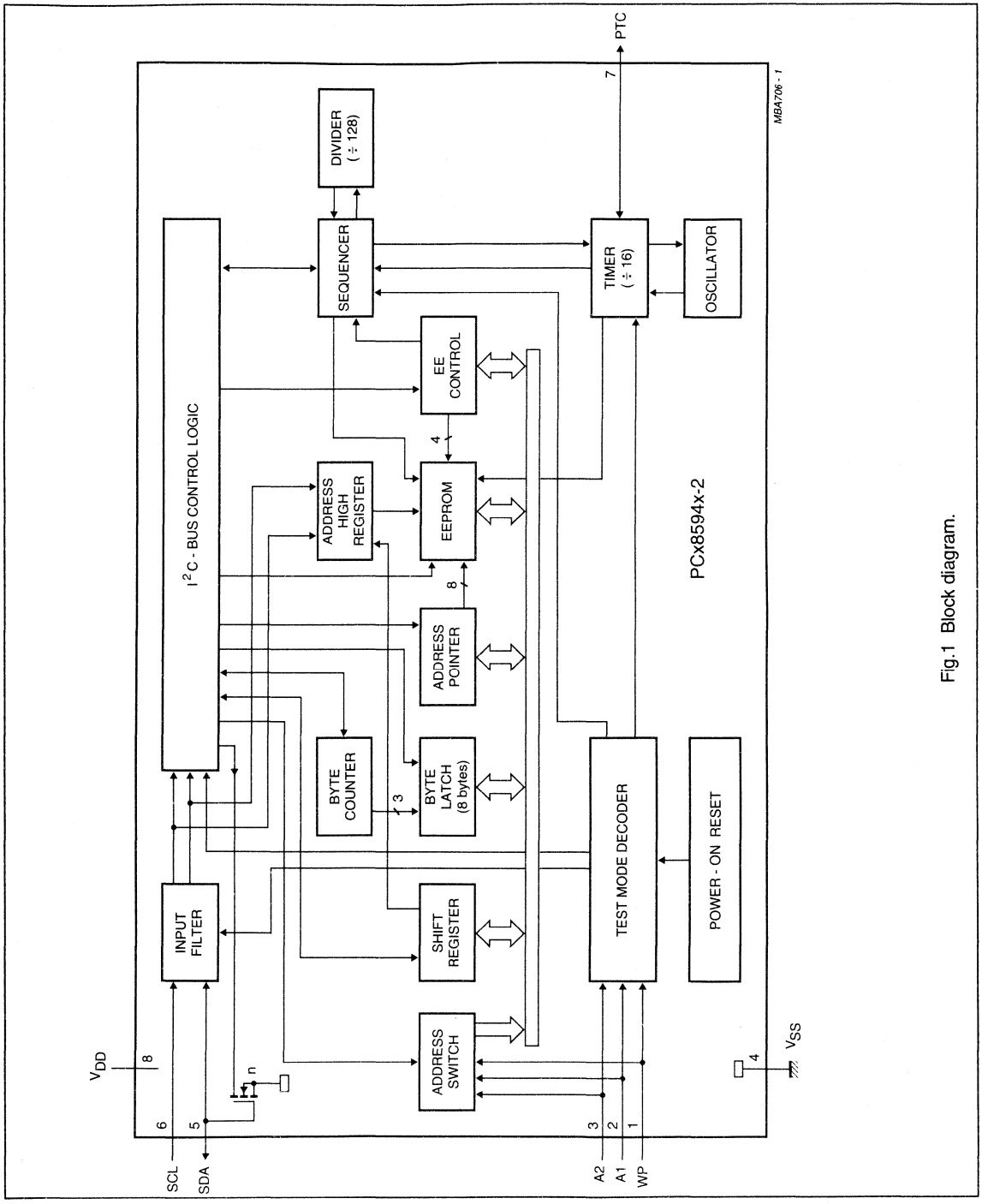


Fig.1 Block diagram.

1024 x 8-bit CMOS EEPROMS with I²C-bus interface

PCx8598x-2 Family

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF A HANDBOOK IC01 OR DATASHEET

FEATURES

- Low Power CMOS
  - maximum active current 2.5 mA
  - maximum standby current 10 µA
- Non-volatile storage of 8-Kbits organized as four pages
  - each 256 x 8 bits
- Only one power supply required
- On-chip voltage multiplier
- Serial input/output bus (I²C)
- Write operations
  - byte write mode
  - 8-byte page write mode (minimizes total write time per byte)
- Write-protection input
- Read operations
  - sequential read
  - random read
- Extended supply voltage range (2.5 to 6.0 V)
- Internal timer for writing (no external components)
- Power-on reset
- High reliability by using a redundant storage code
  - (single bit error correction)
- Endurance
  - 100 k; T_{amb} = 85 °C
- 10 years non-volatile data retention time
- Pin and Address compatible to
  - PCx8582x-2 Family and PCx8589x2 Family

GENERAL DESCRIPTION

The PCFx8598x-2 is a 8-Kbit (1024 x 8-bit) floating gate electrically erasable programmable read only memory (EEPROM). By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability compared to conventional EEPROM memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip, using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to two PCx8598x-2 devices may be connected to the I²C-bus.

Chip select is accomplished by one address input.

Timing of the Erase/Write cycle is done internally, thus no external components are required. Pin 7 must be connected to either V_{DD} or left open-circuit.

There is an option of using an external clock for timing the length of an Erase/Write cycle.

A write protection input (pin 1) allows disable of write-commands from the master by a hardware signal. When pin 1 is HIGH and one of the upper 512 EEPROM cells is addressed, then the data bytes will not be acknowledged by the PCx8598x-2 and the EEPROM contents are not changed.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCx8598x-2P	8	DIL	plastic	SOT97
PCx8598x-2T	8	SO8L	plastic	SOT176C

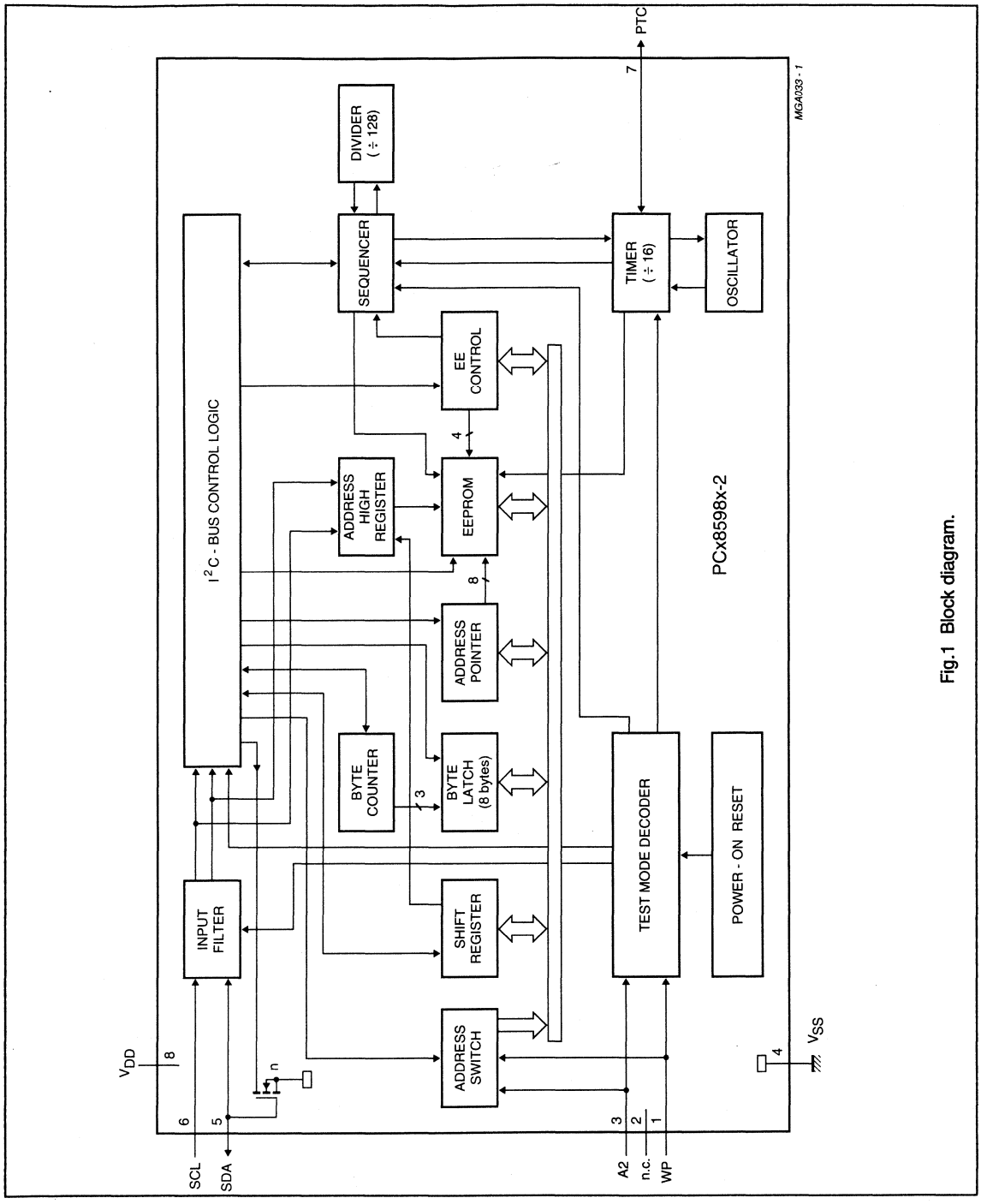


Fig.1 Block diagram.

UNIVERSAL SYNC GENERATOR

GENERAL DESCRIPTION

The SAA1043 generates the synchronizing waveforms required in all types of video source equipment (video cameras, film-scanners, video games, computer displays and similar applications). The device is programmable to suit standards SECAM1, SECAM2, PAL/CCIR, NTSC1, NTSC2 and PAL-M; the video game 624 and 524-line standards; and can be synchronized to an external sync signal. Inputs and outputs are CMOS compatible.

Features

- Programmable to eight standards
- Horizontal frequency manipulation for application in non-standard systems
- Oscillator functions with LC or crystal elements
- Additional outputs to simplify camera signal processing
- Can be synchronized to an external sync signal
- Vertical reset for fast vertical lock
- Subcarrier lock in combination with subcarrier coupler SAA1044
- Very low power consumption

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 28)	V_{DD}	5.7	–	7.5	V
Supply current range (quiescent)	I_{DD}	–	–	10	μA
Oscillator frequency	f_{OSC}	–	–	5.1	MHz
Operating ambient temperature range	T_{amb}	−25	–	+ 70	°C

PACKAGE OUTLINES

SAA1043 : 28-lead DIL; plastic (SOT117).
SAA1043T: 28-lead mini-pack; plastic (SO28; SOT136A).

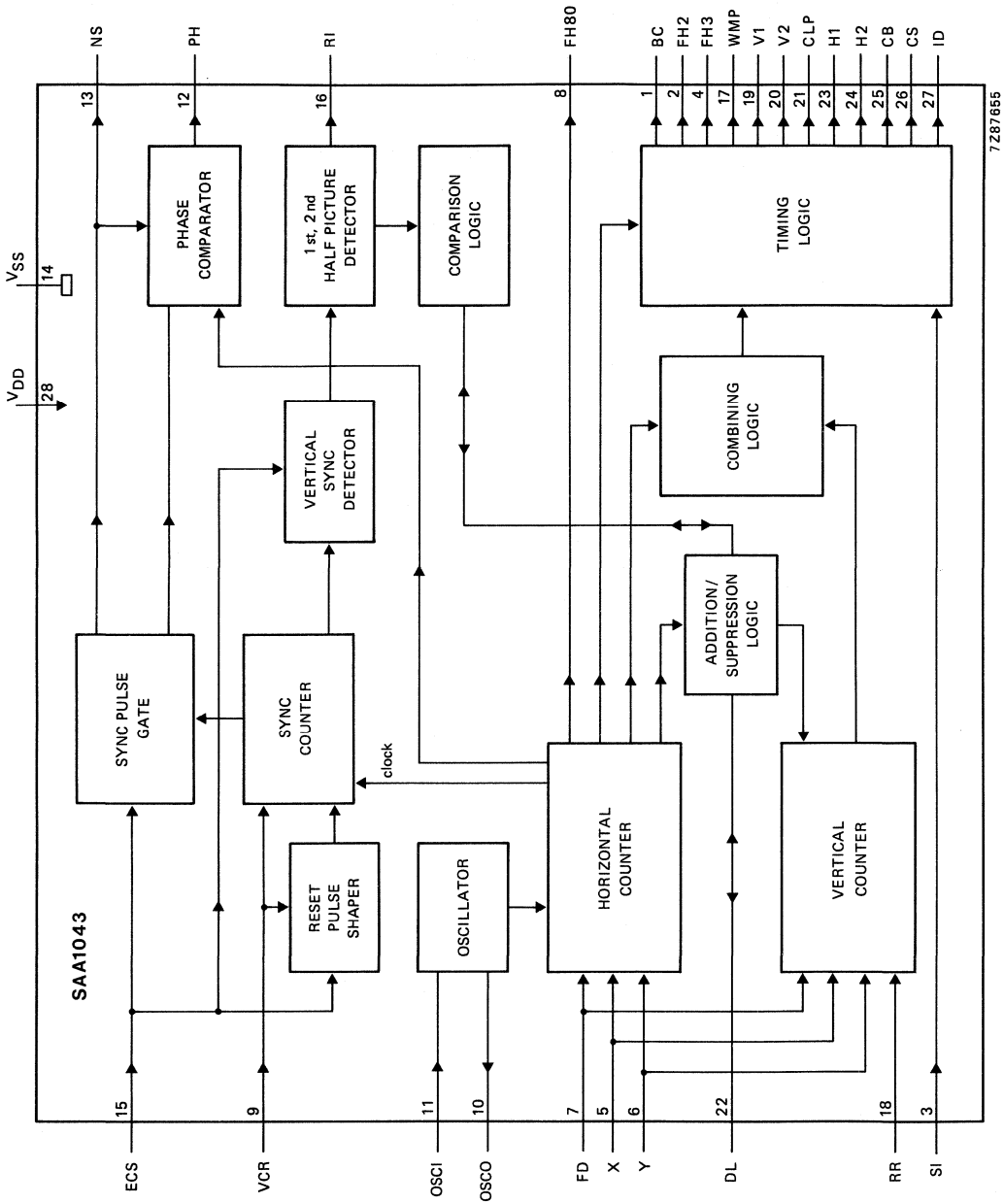


Fig. 1 Block diagram.

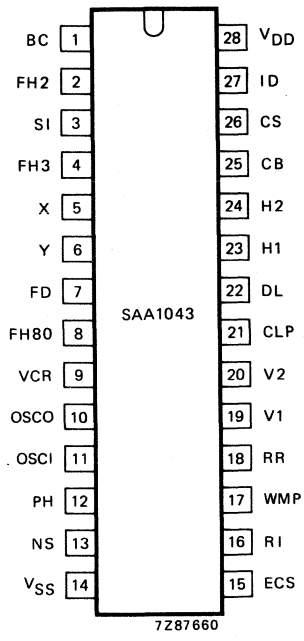


Fig. 2 Pinning diagram.

PINNING

1	BC	burst flag/chrominance blanking (SECAM) output
2	FH2	PAL identification output
3	SI	set identification input (SECAM, PAL, PAL-M)
4	FH3	400 Hz (PAL); 360 HZ (NTSC, PAL-M) and $f_H/3$ (SECAM)
5	X	standard programming input
6	Y	standard programming input
7	FD	standard programming input
8	FH80	80 x f_H output (1.25 MHz)
9	VCR	VCR standard input
10	OSCO	oscillator output
11	OSCI	oscillator input
12	PH	phase detector output
13	NS	no-sync detector output
14	V_{SS}	negative supply voltage (ground)
15	ECS	external composite sync input
16	RI	vertical identification output
17	WMP	white measurement pulse output
18	RR	vertical reset input
19	V1	vertical drive output
20	V2	vertical drive output
21	CLP	clamp pulse output
22	DL	2 x f_H input/output
23	H1	horizontal drive output
24	H2	horizontal drive output
25	CB	composite blanking output
26	CS	composite sync output
27	ID	SECAM identification output
28	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Sync pulse generation

Programming of operating standard

The standard required for operation is programmed using the inputs X, Y and FD as shown in Table 1. The FD input selects 525 or 625-line working of the vertical counter (524 or 624-lines for video game standards) and also influences the choice of oscillator frequency as shown in Table 2.

Table 1 Programming of operating standard

standard	FD	X	Y
SECAM 1	0	0	0
SECAM 2	0	0	1
624	0	1	0
PAL/CCIR	0	1	1
NTSC 1	1	0	0
NTSC 2	1	0	1
524	1	1	0
PAL-M	1	1	1

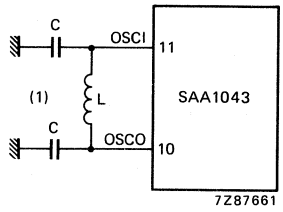
positive logic: 1 = HIGH; 0 = LOW

Oscillator

The built-in oscillator of the SAA1043 functions with an external LC-circuit (Fig. 3) or with a crystal of the parallel resonance type (Fig. 4). For operation in the VCR mode the LC oscillator circuit is recommended. The frequencies required for the operating standards are shown in Table 2.

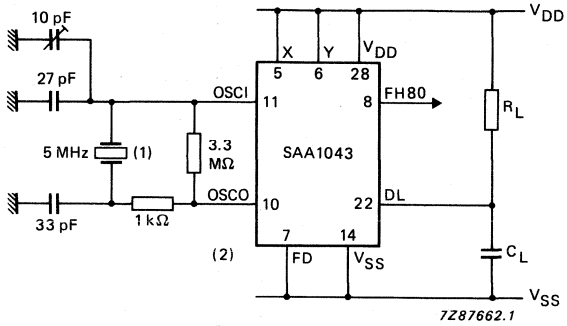
Table 2 Oscillator input frequencies

operating standard	osc. frequency (f_{OSCI}) MHz	vertical divider (FD)	vertical frequency (f_V) Hz	horizontal frequency (f_H) Hz
PAL, SECAM, 624	5.0	0	50	15625
NTSC, PAL-M, 524	5.034964	1	59.94	15734.26
PAL, SECAM, 624	2.5	H2 (pin 24)	50	15625
NTSC, PAL-M, 524	2.51782	H1 (pin 23)	59.94	15734.26



(1) Component values can be calculated from the formula $f_{OSCI} = 1/2\pi\sqrt{LC_V}$ where $C_V = C/2 + C_p$ and C_p = parasitic capacitance of typically 5 pF.

Fig. 3 LC oscillator circuit.



(1) Catalogue number of crystal: 8222 298 40760.

(2) All inputs not shown are at V_{SS}.

Fig. 4 Crystal oscillator circuit showing test set-up for oscillator frequency measurement.

Synchronization to an external sync signal

Use is made of the phase comparator output PH to lock the internally generated sync pulses to an external sync signal. Reset pulses derived at each falling edge of the external sync signal (ECS) reset the the sync counter which is clocked at the internal horizontal frequency by the horizontal counter. At each horizontal scan period the sync counter opens the sync pulse gate and allows the ECS to be applied to the phase comparator where it is compared with the phase of the internally generated horizontal sync pulse. When the two signals are in phase the output PH is in a high impedance state. When a phase difference exists PH is pulled towards V_{DD} or V_{SS} depending on the direction of the error (Fig. 5). The phase-analogue voltage on PH is used to correct the frequency at OSCI via a voltage-controlled oscillator and null the phase error between internal and external signals. Pulses occurring on the ECS outside of the sync pulse gating time (serration and equalization pulses) do not effect the phase comparator.

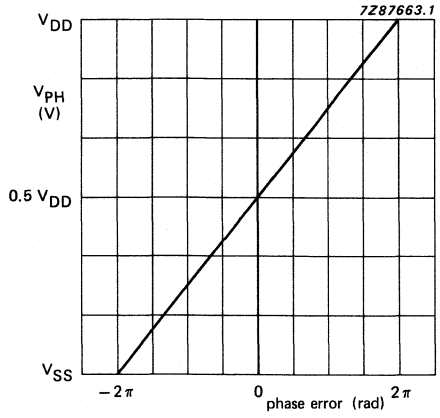


Fig. 5 Phase comparator characteristic.

FUNCTIONAL DESCRIPTION (continued)

Synchronization to an external sync signal (continued)

The circuit will lock to standard and non-standard sync signals. With standard signals the resetting of the sync counter is permitted after 3/4 of the horizontal scan period and if one reset pulse is missed the next pulse will reset the counter. With non-standard signals a narrow reset window is imposed to avoid disturbances which would otherwise be visible on the screen during vertical blanking time. The width of this window is $64 - 15.2 <$ reset time $< 64 + 15.2$ μs. If a reset pulse does not occur within this window the same window timing is specified for the next horizontal scan.

A no-sync signal is generated by the sync pulse gate if the sync counter is not reset from the ECS. The no-sync signal (NS) occurs 6.4 μs after the time of the missing reset pulse.

Detection of the vertical sync in the ECS is performed using a double sampling method which minimizes detection failures. Vertical lock is performed by comparing the internal vertical sync with a pulse derived from the ECS and using the result to modify the period of the vertical counter. This is achieved by manipulating the DL ($2 \times f_H$) input to the vertical counter via the addition/subtraction logic. The DL pulses are added or suppressed to bring the circuit into lock in the shortest possible time; the direction taken is determined by a logic decision based on the half picture in which the ECS derived pulse occurred.

Vertical reset input (RR)

The RR is used when external synchronization runs on separate vertical (V) and horizontal (H) pulses instead of composite sync (CS) pulses.

- RR = LOW : no external sync or external CS to ECS input
- RR = V-pulses: external sync with H and V requires H-pulses to ECS input
  duration of H-pulse < 5 μs
  duration of V-pulse 1 μs $< t_V < 3$ μs

VCR standard input (VCR)

The VCR input sets the synchronization standard for VCRs.

- VCR = HIGH: normal mode

Then the ECS input expects a 64 μs ± 16 μs H-part of the CS pulse.
If the pulse fits inside the window, the SAA1043 will continue to take synchronizing pulses only inside the window.
If the pulse does not occur inside the window, the synchronizing circuit will take off the window and accept pulses at any time.

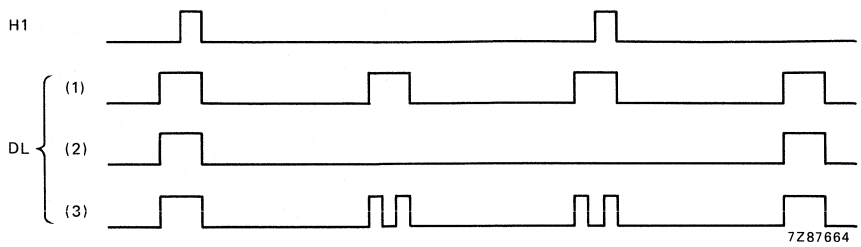
- VCR = LOW: VCR mode

The window ± 16 μs is always applied.

If the colour burst is not present in the correct position, or FH2 is not in phase with the incoming signal, the set identification input (SI) must be set to logic HIGH on line 2 for the duration of 1 line.

Use in non-standard systems

For systems requiring a non-standard horizontal frequency the number of horizontal scans per picture can be manipulated using the open drain input/output DL. The addition or suppression of pulses during the high ohmic period of DL modifies the vertical counter value. The suppression of two DL pulses per half picture will give one extra horizontal scan and the addition of two DL pulses will remove one horizontal scan from the half picture (see Fig. 6).



(1) Normal waveform at DL; $f_{DL} = 2 \times f_H$.

(2) Waveform at DL with two pulses suppressed increases the number of horizontal scans per half picture by 1.

(3) Waveform at DL with two additional pulses decreases the number of horizontal scans per half picture by 1.

Fig. 6 Manipulation of the horizontal frequency for non-standard systems.

Output waveforms

The output waveforms for the different modes of operation are shown in Figs 7 and 8.

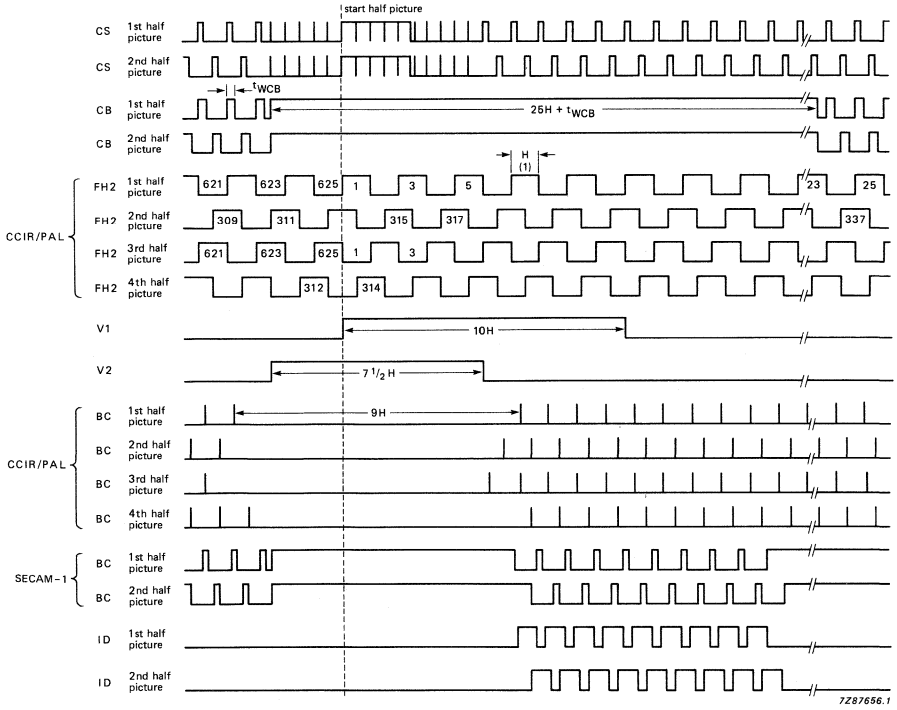
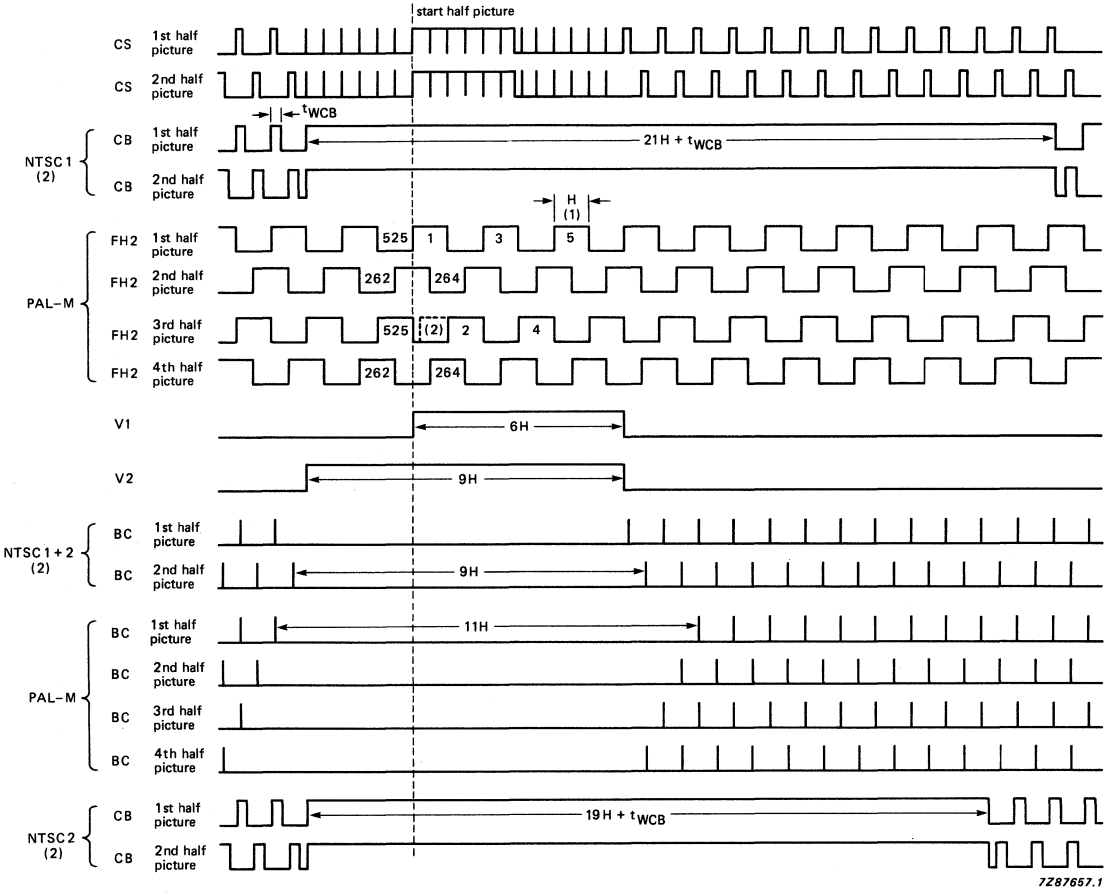


Fig. 7 Typical output waveforms for PAL/CCIR and SECAM. In the 624-line mode the output waveforms are identical to the 1st half picture of PAL/CCIR and are not interlaced (0.5 H subtracted from the waveform timing).



(1) H = 1 horizontal scan.

(2) NTSC mode reset; the 4th half picture is identical to the 2nd half picture for NTSC.

Fig. 8 Typical output waveforms for NTSC and PAL-M. In the 524-line mode the output waveforms are identical to the 1st half picture of NTSC and are not interlaced (0.5 H subtracted from the waveform timing).

WAVEFORM TIMING (Table 3, Figs 9 and 10)

The waveform timing depends on the frequency of the oscillator input (f_{OSCI}). This is shown in Table 3 as the number (n) of oscillations at OSCI. The timings given are derived from $n \times t_{OSCI} \pm 100$ ns. One horizontal scan (H) = $320 \times t_{OSCI} = 1/f_H$. Note that the number of horizontal scans per half picture can be modified for non-standard systems using input/output DL as shown in Fig. 6.

Table 3 Waveform timing

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
CS							
Horizontal sync pulse width	t_{WSC1}	4.8	4.77	4.77	4.8	µs	24
Equalizing pulse width	t_{WSC2}	2.4	2.38	2.38	2.4	µs	8
Serration pulse width	t_{WSC3}	4.8	4.77	4.77	4.8	µs	24
Duration of pre-equalizing pulses		2.5	3	3	2.5	H	
Duration of post-equalizing pulses		2.5	3	3	2.5	H	
Duration of serration pulses		2.5	3	3.5	2.5	H	
CB							
Horizontal blanking pulse width							
PAL/SECAM/PAL-M	t_{WCB}	12	–	11.12	12	µs	60
NTSC 1	t_{WCB}	–	11.12	–	–	µs	56
NTSC 2	t_{WCB}	–	10.53*	–	–	µs	53
Front porch	t_{PCBCS}	1.6	1.59	1.59	1.6	µs	8
Duration of vertical blanking							
PAL/SECAM/PAL-M		25H+t_{WCB}	–	21H+t_{WCB}	25H+t_{WCB}		
NTSC 1		–	21H+t_{WCB}	–	–		
NTSC 2		–	19H+t_{WCB}	–	–		
BC (PAL)							
Burst key pulse width	t_{WBC}	2.4	2.38	2.38	–	µs	12
Sync to burst delay	t_{PCSBC}	5.6	5.56	5.76	–	µs	28
Burst suppression		9	9	11	–	H	
Position of burst suppression: 1st half picture		H623 to H6	H523 to H6	H523 to H8	– –		
2nd half picture		H310 to H318	H261 to H269	H260 to H270	– –		
3rd half picture		H622 to H5	H523 to H6	H522 to H7	– –		
4th half picture		H311 to H319	H261 to H269	H259 to H269	– –		

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
BC (SECAM)							
Chrominance pulse width	t_{WBC}	–	–	–	7.2	µs	36
Chrominance to sync delay	t_{PBCCS}	–	–	–	1.6	µs	8
Duration of vertical blanking: SECAM 1	1st half picture : 25H + t_{WBC} except H320 to H328 2nd half picture: 24.5H + t_{WBC} except H7 to H15						
SECAM 2	1st half picture : 25H + t_{WBC} 2nd half picture: 24.5H + t_{WBC}						
CLP							
Clamp pulse width	t_{WCLP}	2.4	2.38	2.38	2.4	µs	12
Sync to clamp delay	t_{PCSCLP}	2.4	2.38	2.38	2.4	µs	12
DL							
Frequency	f_{DL}	$2 \times f_H$	$2 \times f_H$	$2 \times f_H$	$2 \times f_H$		
Pulse width	t_{WDL}	9.6	9.53	9.53	9.6	µs	48
DL to sync delay	t_{PCLCS}	5.6	5.56	5.56	5.6	µs	28
FH80							
Frequency	f_{FH80}	$80 \times f_H$	$80 \times f_H$	$80 \times f_H$	$80 \times f_H$		
Sync to FH80 delay		0.2	0.2	0.2	0.2	µs	1
H1, H2							
H1 pulse width	t_{WH1}	7.2	7.15	7.15	7.2	µs	36
H2 pulse width	t_{WH2}	7.2	7.15	7.15	7.2	µs	36
H1 to sync delay	t_{PH1CS}	0.8	0.79	0.79	0.8	µs	4
Sync to H2 delay	t_{PCSH2}	0.8	0.79	0.79	0.8	µs	4
Repetition period		64	63.56	63.56	64	µs	
V1, V2							
V1 duration		10	6	6	10	H	
V2 duration		7.5	9	9	7.5	H	
V1 to sync delay	t_{PV1CS}	1.6	1.59	1.59	1.6	µs	8
Sync to V2 delay	t_{PV2CS}	1.6	1.59	1.59	1.6	µs	8
FH2							
Frequency	f_{FH2}	$f_H/2$	$f_H/2$	$f_H/2$	$f_H/2$		
Sync to FH2 delay		0	0	0	0	µs	
FH3							
Frequency	f_{FH3}	400	360	360	$f_H/3$		
Sync to FH3 delay		–	–	–	0	µs	

WAVEFORM TIMING (continued)

Table 3 (continued)

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
WMP							
WMP pulse width		2.4	2.38	2.38	2.4	μs	12
Sync to WMP delay		34.4	34.16	34.16	34.4	μs	172
Duration of WMP		10	9	9	10	H	
Position of WMP							
1st half picture:		H163 to H173	H134 to H143	H134 to H143	H163 to H173		
2nd half picture:		H475 to H485	H396 to H405	H396 to H405	H475 to H485		
RI							
Frequency		$f_V/2$	$f_V/2$	$f_V/2$	$10f_H$		
Position of edges		H6 and H318	H7 and H269	H7 and H269	–		
ID							
ID pulse width	t_{WID}	12.0	11.12	11.12	12.0	μs	60
ID to sync delay	t_{PIDCS}	1.6	1.59	1.59	1.6	μs	8
Position of ID							
1st half picture:		H7 to H15	H8 to H22	H8 to H22	H7 to H15		
2nd half picture:		H320 to H328	H271 to H285	H271 to H285	H320 to H328		

* Horizontal blanking pulse width for NTSC 2 can be 11.12 μs maximum.

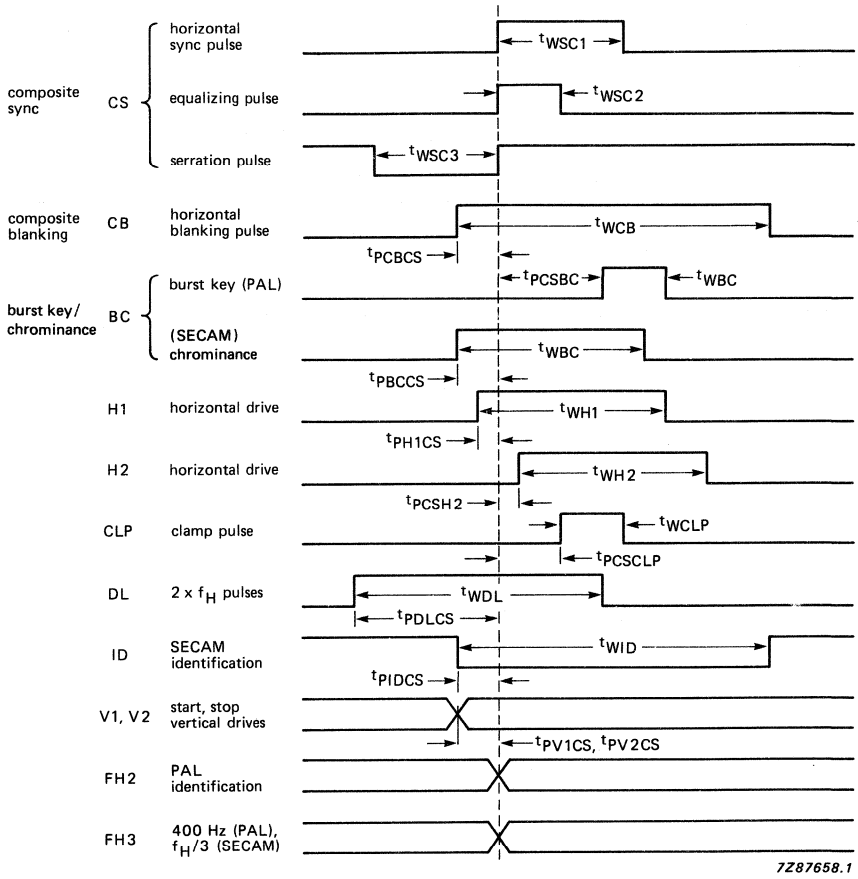


Fig. 9 Waveform timings; PAL/CCIR; SECAM; 624-line modes.

WAVEFORM TIMING (continued)

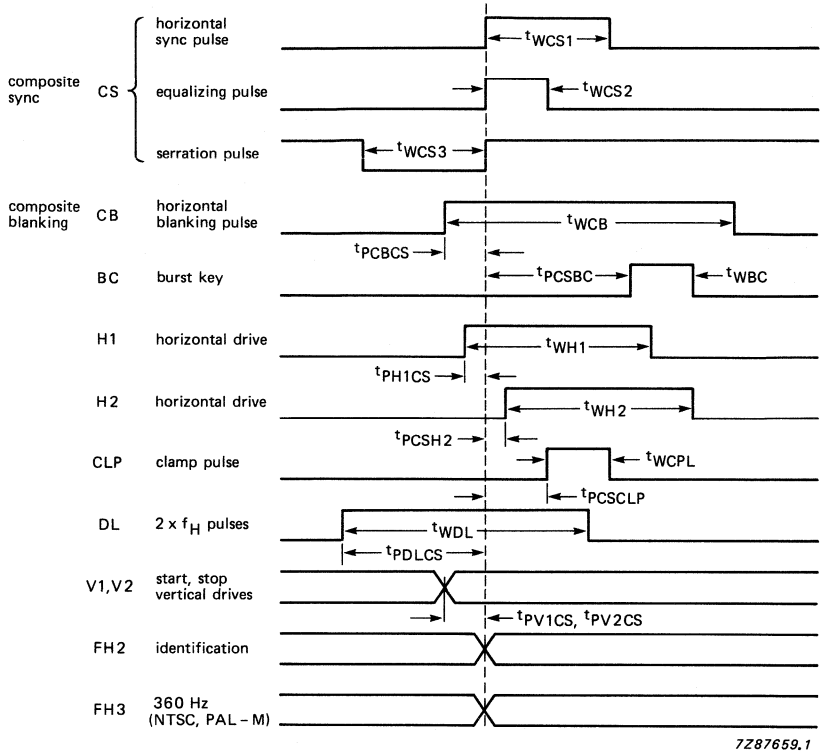


Fig. 10 Waveform timings: NTSC; PAL-M; 524-line modes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range with respect to V_{SS}	V_{DD}	−0.5	+ 15	V
Input voltage range	V_I	−0.5	V_{DD} + 0.5*	V
Input current	$\pm I_I$	–	10	mA
Output voltage range	V_O	−0.5	V_{DD} + 0.5*	V
Output current	$\pm I_O$	–	10	mA
Total power dissipation per package	P_{tot}	–	200	mW
Power dissipation per output	P_O	–	100	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* V_{DD} + 0.5 V not to exceed 15 V.

CHARACTERISTICS

V_{DD} = 5.7 to 7.5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	V_{DD}	5.7	–	7.5	V
Supply current (quiescent) at I_O = 0 mA at all outputs; V_{DD} = 7.5 V; T_{amb} = 25 °C	I_{DD}	–	–	10	μA
Inputs					
Input voltage HIGH	V_{IH}	$0.7V_{DD}$	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	$0.3V_{DD}$	V
Input leakage current at V_I = 7.5 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	I_{LI}	–	–	1	μA
Input leakage current at V_I = 0 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	$-I_{LI}$	–	–	1	μA
Outputs (except PH and OSC0)					
Output voltage HIGH at $-I_{OH}$ = 0.5 mA	V_{OH}	$V_{DD} - 0.5$	–	–	V
Output voltage LOW at I_{OL} = 0.5 mA	V_{OL}	–	–	0.4	V
Output PH					
Output voltage HIGH at $-I_{OH}$ = 0.9 mA	V_{OH}	$V_{DD} - 0.5$	–	–	V
Output voltage LOW at I_{OL} = 1.0 mA	V_{OL}	–	–	0.4	V
Output leakage current at V_O = 7.5 V; V_{DD} = 7.5 V	I_{LO}	–	–	5	μA
Output leakage current at V_O = 7.5 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	I_{LO}	–	–	1	μA
Output leakage current at V_O = 0 V; V_{DD} = 7.5 V	$-I_{LO}$	–	–	5	μA
Output leakage current at V_O = 0 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	$-I_{LO}$	–	–	1	μA
Output OSCO					
Output voltage HIGH at V_{OSCI} = 0 V; $-I_{OH}$ = 0.9 mA	V_{OH}	$V_{DD} - 0.5$	–	–	V
Output voltage LOW at V_{OSCI} = V_{DD}; I_{OL} = 1.0 mA	V_{OL}	–	–	0.4	V

parameter	symbol	min.	typ.	max.	unit
Input/output DL (open drain)*					
Output voltage LOW at I_{OL} = 1.0 mA	V_{OL}	–	–	0.4	V
Output leakage current at V_O = 7.5 V; V_{DD} = 7.5 V	I_{LO}	–	–	5	μA
Output leakage current at V_O = 7.5 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	I_{LO}	–	–	1	μA
Load resistance (Fig. 4)					
at V_{DD} = 5.7 V	R_L	1.4	–	–	kΩ
at V_{DD} = 7.5 V	R_L	0.82	–	–	kΩ
Time constant (Fig. 4)					
at V_{DD} = 5.7 V	R_LC_L	–	–	19	ns
at V_{DD} = 7.5 V	R_LC_L	–	–	13	ns
Oscillator frequency (Fig. 4)					
Maximum oscillator frequency at V_{DD} = 5.7 V	f_{OSC}	5.1	–	–	MHz

* An external pull-up resistor (3.9 kΩ) must be connected between DL and V_{DD}. The time constant R_LC_L must not exceed the values given.

APPLICATION INFORMATION

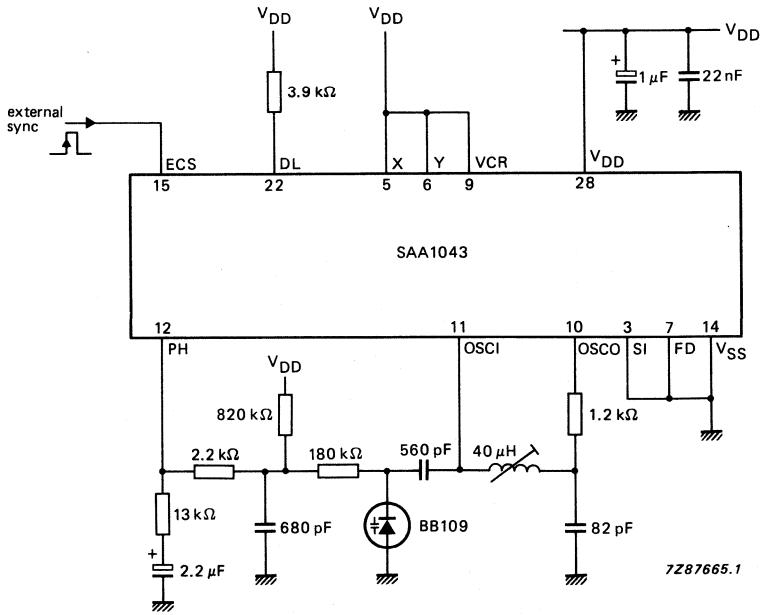


Fig. 11 Synchronizing circuit using passive filter network.

SUBCARRIER COUPLER

GENERAL DESCRIPTION

The SAA1044 maintains the correct relationship between subcarrier and horizontal scan frequencies when an exact coupling is required. It is for use in combination with sync generator SAA1043 for application in colour video sources (cameras, film-scanners and similar equipments).

Features

- Provides exact relationship between subcarrier and horizontal scan frequencies
- Accommodates all standard frequencies
- Facilitates GENLOCK (general locking) applications

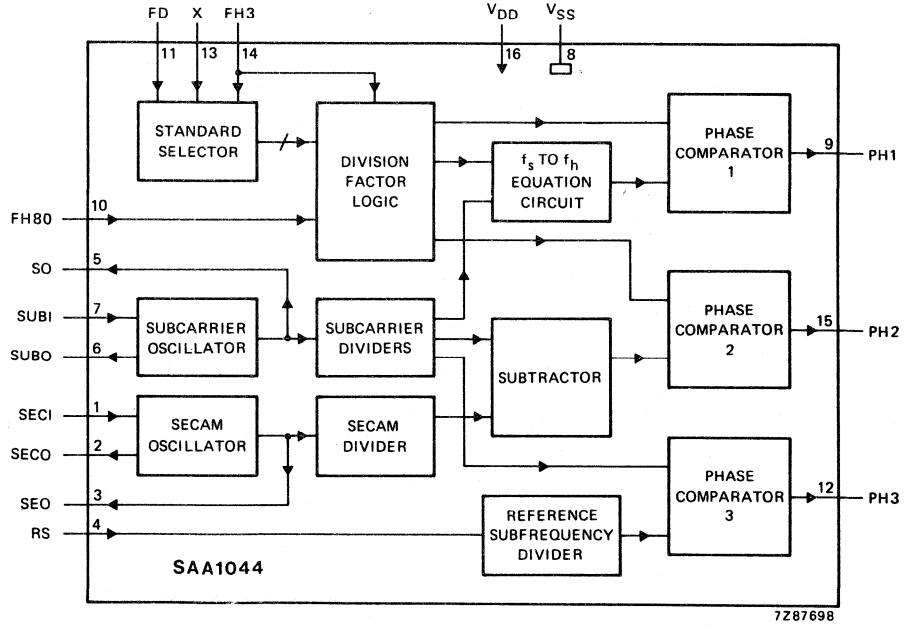


Fig.1 Block diagram.

PACKAGE OUTLINES

SAA1044: 16-lead DIL; plastic (SOT38).
SAA1044T: 16-lead mini-pack; plastic (SO16L; SOT162A).

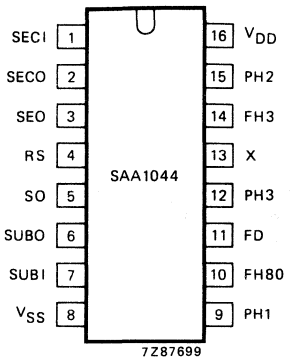


Fig. 2 Pinning diagram.

PINNING

1	SECI	SECAM oscillator input ($272f_H$)
2	SECO	SECAM oscillator output ($272f_H$)
3	SEO	inverted SECAM oscillator output
4	RS	reference subfrequency
5	SO	inverted subcarrier oscillator output
6	SUBO	subcarrier oscillator output
7	SUBI	subcarrier oscillator input
8	V_{SS}	negative supply voltage (ground)
9	PH1	phase comparator 1 output (FH80/SUBI)
10	FH80	1.25 MHz input (from SAA1043)
11	FD	standard programming input
12	PH3	phase comparator 3 output (RS/SUBI)
13	X	standard programming input
14	FH3	standard programming input (from SAA1043)
15	PH2	phase comparator 2 output (SECI/FH80)
16	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Programming of operating standard

The standard required for operation is programmed using the inputs FD, X and FH3 as shown in Table 1.

Table 1 Programming of operating standard

standard	FD	X	FH3	relationship of subcarrier frequency (f_S) to horizontal scan frequency (f_H)
PAL	0	1	400 Hz	$f_S = 283.7516f_H$
SECAM	0	0	don't care	$f_S = 282f_H$
PAL-N	1	1	400 Hz	$f_S = 229.2516f_H$
PAL-M	1	0	1	$f_S = 227.25f_H$
NTSC	1	0	0	$f_S = 227.5f_H$

Positive logic: 1 = HIGH; 0 = LOW

Subcarrier/horizontal scan frequency relationship

The input FH80 from SAA1043 is the reference for horizontal scan frequency (f_H). This frequency is reduced by a factor determined by the selected operating standard to give a value of $8f_H$ (PAL, SECAM) or $10f_H$ (PAL-N, PAL-M, NTSC) to phase comparator 1. The subcarrier frequency (f_S) is manipulated to provide a comparable value at the second input to the phase comparator. When the frequencies of the two inputs to phase comparator 1 are equal, the relationship between f_H and f_S is as shown in Table 1.

Phase comparator 1 functions with an exclusive-OR phase detector circuit and provides an output which may be used to control a voltage-controlled oscillator (VCO) via a low-pass filter. The VCO reference can be the subcarrier or the horizontal scan frequency and the filter can be active or passive, depending on application.

A second subcarrier oscillator circuit is provided for SECAM operation. The operating frequency of this is centred on $272f_H$ to give, when $f_S = 282f_H$, comparable values of $5f_H$ at the two inputs to phase comparator 2. A second VCO loop can be used to control the SECAM oscillator frequency.

The high degrees of accuracy and stability required for GENLOCK applications are met by phase comparator 3. This compares the internal subcarrier and external reference frequencies. To adjust the phase over 2π, this comparator has a linear characteristic over 4π. The output signal PH3 has a period time of $f_S/4$ and a duty factor of between 12.5% and 62.5% giving a sensitivity of 240 mV/rad. Errors due to temperature variation are minimized by symmetrical circuit and chip design.

RATINGS

parameter	symbol	min.	max.	unit
Supply voltage range with respect to V_{SS}	V_{DD}	−0.5	+ 15	V
Input voltage range	V_I	−0.5	V_{DD} + 0.5*	V
Input current	$\pm I_I$	–	10	mA
Output voltage range	V_O	−0.5	V_{DD} + 0.5*	V
Output current	$\pm I_O$	–	10	mA
Total power dissipation per package	P_{tot}	–	200	mW
Power dissipation per output	P_O	–	100	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

HANDLING

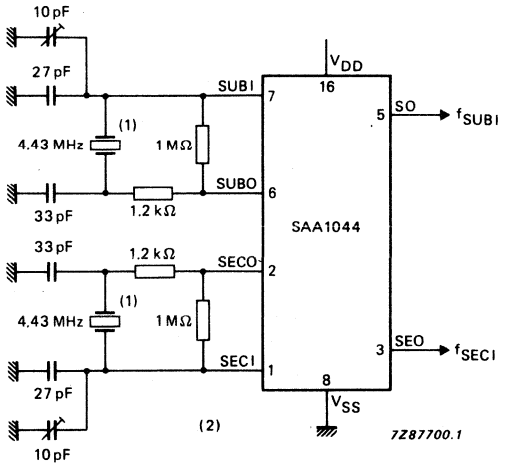
Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* V_{DD} + 0.5 V not to exceed 15 V.

CHARACTERISTICS

V_{DD} = 5.7 to 7.5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C unless otherwise specified

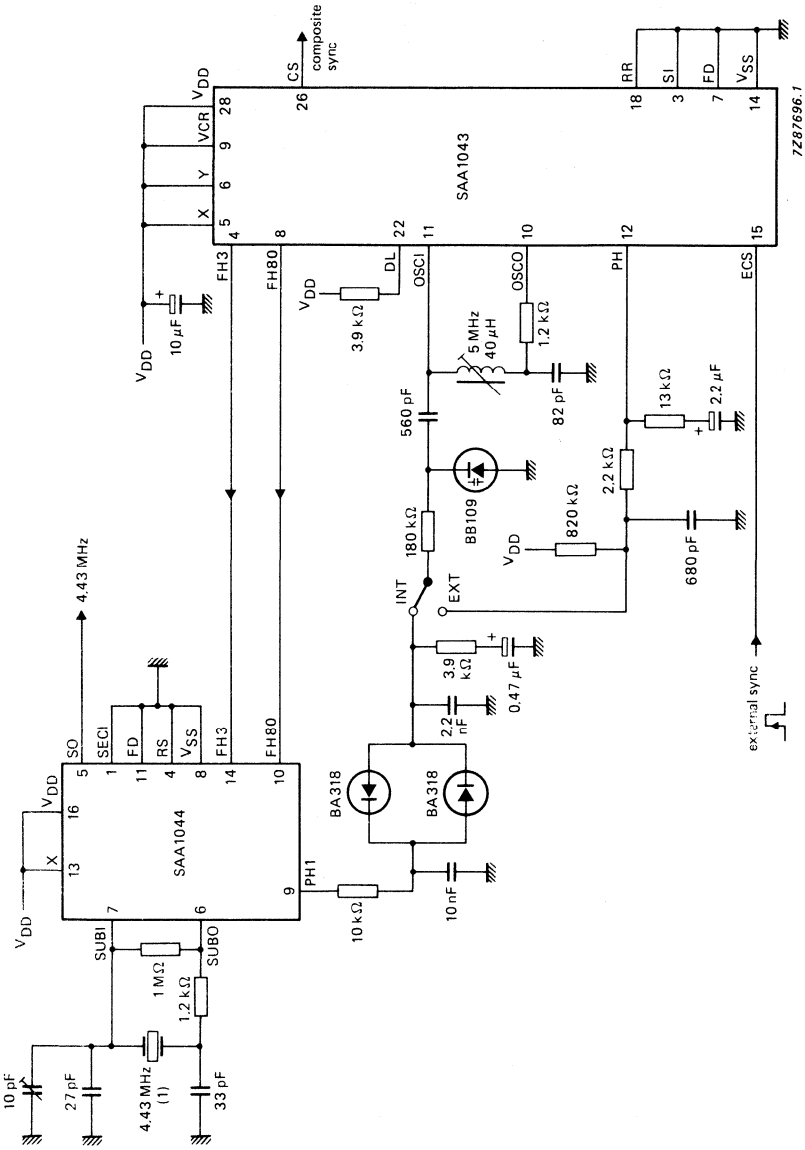
parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	V_{DD}	5.7	–	7.5	V
Supply current (quiescent) at I_O = 0 mA at all outputs; V_{DD} = 7.5 V; T_{amb} = 25 °C	I_{DD}	–	–	10	μA
Inputs					
Input voltage HIGH	V_{IH}	$0.7V_{DD}$	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	$0.3V_{DD}$	V
Input leakage current at V_I = 7.5 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	I_{LI}	–	–	1	μA
Input leakage current at V_I = 0 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	$-I_{LI}$	–	–	1	μA
Outputs (except SECO and SUBO)					
Output voltage HIGH at $-I_{OH}$ = 0.5 mA	V_{OH}	V_{DD} −0.5	–	–	V
Output voltage LOW at I_{OL} = 0.5 mA	V_{OL}	–	–	0.4	V
Outputs SECO and SUBO					
Output voltage HIGH at $-I_{OH}$ = 0.9 mA	V_{OH}	V_{DD} −0.5	–	–	V
Output voltage LOW at I_{OL} = 1.0 mA	V_{OL}	–	–	0.4	V
Oscillator frequency (Fig.3)					
Maximum oscillator frequency at V_{DD} = 5.7 V					
pin 1	f_{SECI}	5.1	–	–	MHz
pin 7	f_{SUBI}	5.1	–	–	MHz



(1) Catalogue number of crystal: 4322 143 04040.
(2) Inputs not shown are don't care.

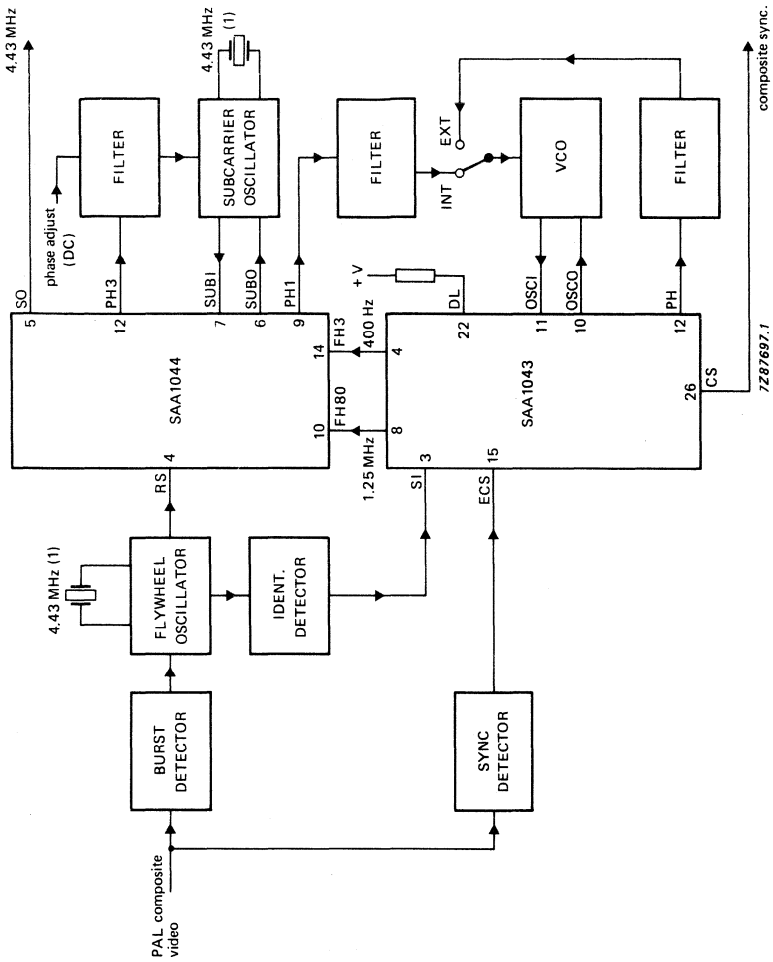
Fig.3 Test set-up for oscillator frequency measurement.

APPLICATION INFORMATION



(1) Catalogue number of crystal: 4322 143 04040.

Fig.4 Subcarrier coupling for PAL application; external synchronization is selected with switch in EXT condition.



(1) Catalogue number of crystal: 4322 143 04040.

Fig.5 Subcarrier coupling for PAL GENLOCK application.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

4-DIGIT LED-DRIVER WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The LED-driver is a bipolar integrated circuit made in an I²L compatible 18 volts process. The circuit is especially designed to drive four 7-segment LED displays with decimal point by means of multiplexing between two pairs of digits. It features an I²C-Bus slave transceiver interface with the possibility to program four different SLAVE ADDRESSES, a POWER RESET flag, 16 current sink OUTPUTS, controllable by software up to 21 mA, two multiplex drive outputs for common anode segments, an on-chip multiplex oscillator, control bits to select static, dynamic and blank mode, and one bit for segment test.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	$V_{EE} = 0$ V	V_{CC}	4.5	5	15	V
Supply current all outputs OFF	$V_{CC} = 5$ V	I_{CC}*	7	9.5	14	mA
Total power dissipation						
24-lead DIL (SOT101B)		P_{tot}	–	–	1000	mW
24-lead DIL SO (SOT137A)		P_{tot}	–	–	500	mW
Operating ambient temperature range		T_{amb}	–40	–	+85	°C

* The positive current is defined as the conventional current flow into a device (sink current).

PACKAGE OUTLINE

SAA1064: 24-lead DIL; plastic with internal heat spreader (SOT101B).
SAA1064T: 24-lead mini-pack; plastic (SO-24; SOT137A).

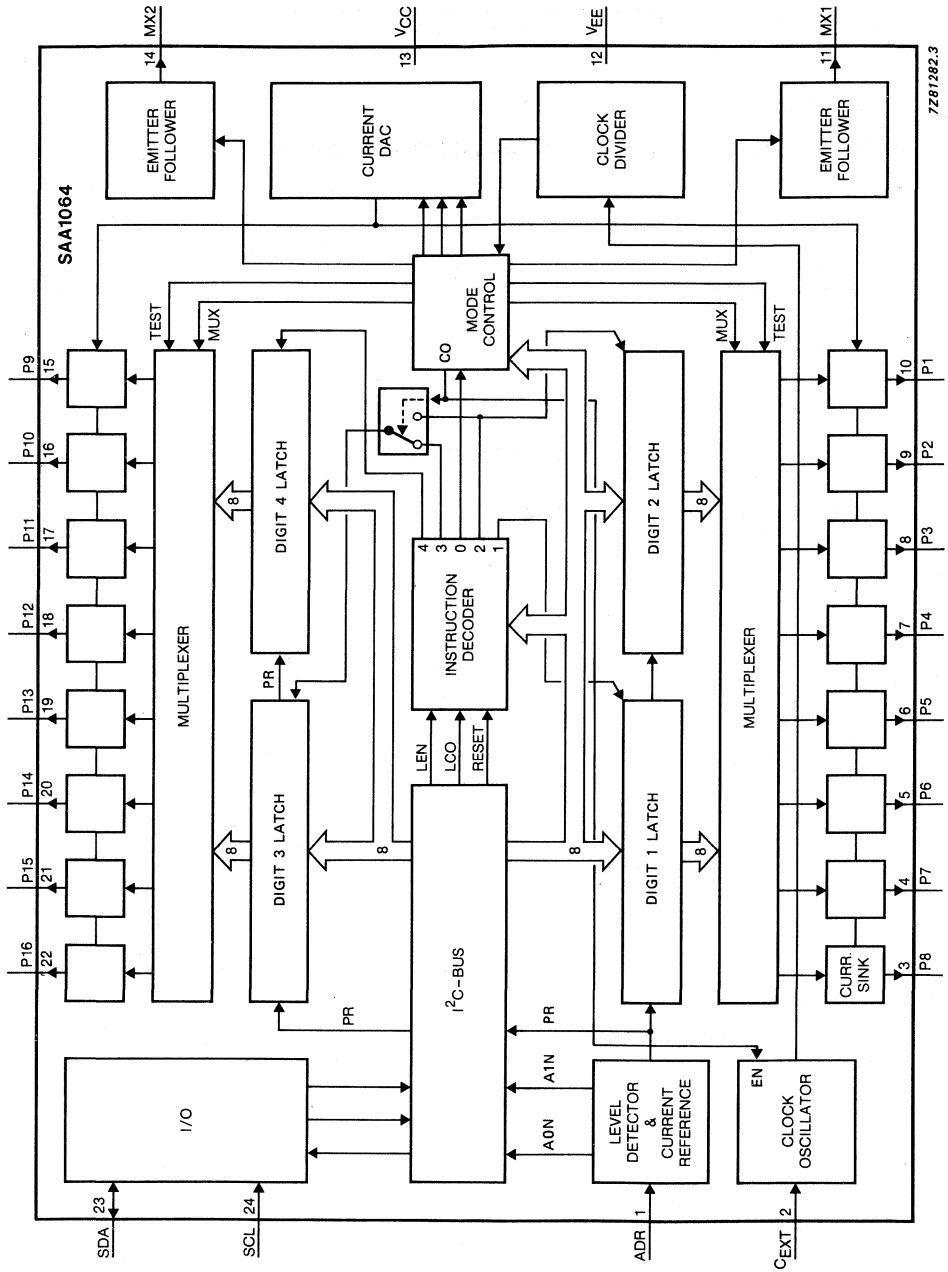


Fig.1 Block diagram.

MICROPROCESSOR CONTROLLED STEREO SOUND GENERATOR FOR SOUND EFFECTS AND MUSIC SYNTHESIS

GENERAL DESCRIPTION

The SAA1099 is a monolithic integrated circuit designed for generation of stereo sound effects and music synthesis.

Features

- Six frequency generators
  - eight octaves per generator
  - 256 tones per octave
- Two noise generators
- Six noise/frequency mixers
- Twelve amplitude controllers
- Two envelope controllers
- Two 6-channel mixers/current sink analogue output stages
- TTL input compatible
- Readily interfaces to 8-bit microcontroller
- Minimal peripheral components
- Simple output filtering

Applications

- Consumer games systems
- Home computers
- Electronic organs
- Arcade games
- Toys
- Chimes/alarm clocks

QUICK REFERENCE DATA

Supply voltage (pin 18)	V_{DD}	typ.	5 V
Supply current (pin 18)	I_{DD}	typ.	70 mA
Reference current (pin 6)	I_{ref}	typ.	250 μA
Total power dissipation	P_{tot}		500 mW
Operating ambient temperature range	T_{amb}		0 to + 70 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

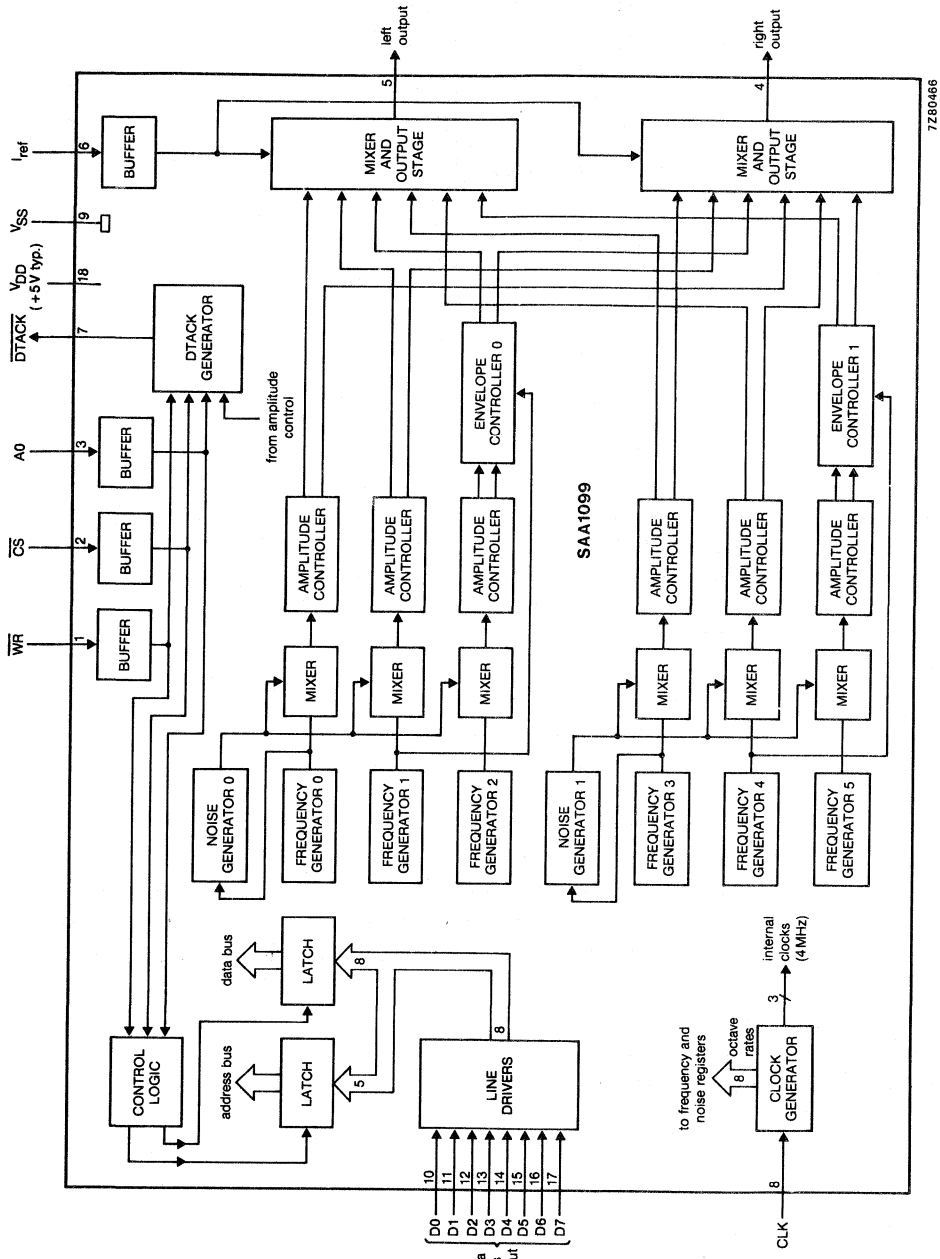


Fig. 1 Block diagram.

PINNING

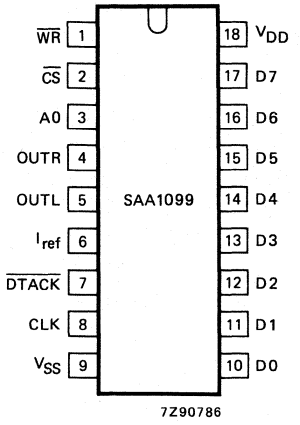


Fig. 2 Pinning diagram.

PIN DESIGNATION

1	$\overline{WR}$	**Write Enable**: active LOW input which operates in conjunction with $\overline{CS}$ and A0 to allow writing to the internal registers.
2	$\overline{CS}$	**Chip Select**: active LOW input to identify valid $\overline{WR}$ inputs to the chip. This input also operates in conjunction with $\overline{WR}$ and A0 to allow writing to the internal registers.
3	A0	**Control/Address select**: input used in conjunction with $\overline{WR}$ and $\overline{CS}$ to load data to the control register (A0 = 0) or the address buffer (A0 = 1).
4	OUTR	**Right channel output**: a 7-level current sink analogue output for the 'right' component. This pin requires an external load resistor.
5	OUTL	**Left channel output**: a 7-level current sink analogue output for the 'left' component. This pin requires an external load resistor.
6	I_{ref}	**Reference current supply**: used to bias the current sink outputs.
7	$\overline{DTACK}$	**Data Transfer Acknowledge**: open drain output, active LOW to acknowledge successful data transfer. On completion of the cycle $\overline{DTACK}$ is set to inactive.
8	CLK	**Clock**: input for an externally generated clock at a nominal frequency of 8 MHz.
9	V_{SS}	**Ground**: 0 V.
10-17	D0-D7	**Data**: Data bus input.
18	V_{DD}	**Power supply**: + 5 V typical.

FUNCTIONAL DESCRIPTION

The following sections provide a detailed functional description of the SAA1099 as shown in the block diagram, Fig. 1.

Frequency generators

Six frequency generators can each select one of 8 octaves and one of 256 tones within an octave. A total frequency range of 31 Hz to 7,81 kHz is available. The outputs may also control noise or envelope generators. All frequency generators have an enable bit which switches them on and off, making it possible to preselect a tone and to make it inaudible when required. The frequency generators may be synchronized using the frequency reset bit.

The frequency ranges per octave are:

Octave	Frequency range
0	31 Hz to 61 Hz
1	61 Hz to 122 Hz
2	122 Hz to 244 Hz
3	245 Hz to 488 Hz
4	489 Hz to 977 Hz
5	978 Hz to 1,95 kHz
6	1,96 kHz to 3,91 kHz
7	3,91 kHz to 7,81 kHz

Noise generators

The two noise generators both have a programmable output. This may be a software controlled noise via one of the frequency controlled generators or one of three pre-defined noises. There is no tone produced by the frequency generator when it is controlling the noise generator. The noise produced is based on double the frequency generator output, i.e. a range of 61 Hz to 15,6 kHz.

In the event of a pre-defined noise being chosen, the output of noise generator 0 can be mixed with frequency generator 0, 1 and 2; and the output of noise generator 1 can be mixed with frequency generator 3, 4 and 5. In order to produce an equal level of noise and tone outputs (when both are mixed) the amplitude of the tone is increased. The three pre-defined noises are based on a clock frequency of 7,8 kHz, 15,6 kHz or 31,25 kHz.

Noise/frequency mixers

Six noise/frequency mixers each with four selections

- Channel off
- Frequency only
- Noise only
- Noise and frequency

Each mixer channel has one of the frequency generator outputs fed to it, three channels use noise generator 0 and the other three use noise generator 1.

Amplitude controllers

Each of the six channel outputs from the mixer is split up into a right and left component giving effectively twelve amplitude controllers. An amplitude of 16 possible levels is assigned to each of the twelve signals. With this configuration a stereo effect can be achieved by varying only the amplitude component. The moving of a sound from one channel to the other requires, per tone, only one update of the amplitude register contents.

When an envelope generator is used, the amplitude levels are restricted. The number of levels available is then reduced to eight. This is achieved by disabling the least significant bit (LSB) of the amplitude control.

Envelope controllers

Two of the six tone generators are under envelope control. This applies to both the left and right outputs from the tone generator.
The envelope has the following eight possible modes:

- Amplitude is zero
- Single attack
- Single decay
- Single attack-decay (triangular)
- Maximum amplitude
- Continuous attack
- Continuous decay
- Continuous attack-decay

The timing of the envelope controllers is programmable using one of the frequency generators (see Fig. 1). When the envelope mode is selected for a channel its control resolution is halved for that channel from 16 levels to 8 levels by rounding down to the nearest even level.
There is also the capability of controlling the 'right' component of the channel with inverse of the 'left' component, which remains as programmed.

A direct enable permits the start of an envelope to be defined, and also allows termination of an envelope at any time. The envelope rate may be controlled by a frequency channel (see Fig. 1), or by the microprocessor writing to the address buffer register. If the frequency channel controlled is OFF (NE = FE = 0) the envelope will appear at the output, which provides an alternative 'non-square' tone capability. In this event the frequency will be the envelope rate, which provided the rate is from the frequency channel, will be a maximum of 1 kHz. Higher frequencies of up to 2 kHz can be obtained by the envelope resolution being halved from 16 levels to 8 levels. Rates quoted are based on the input of a 8 MHz clock.

Six-channel mixers/current sink analogue output stages

Six channels are mixed together by the two mixers allowing each one to control one of six equally weighted current sinks, to provide a seven level analogue output.

Command/control select

In order to simplify the microprocessor interface the command and control information is multiplexed. To select a register in order to control frequencies, amplitudes, etc. the command-register has to be loaded. The contents of this register determines to which register the data is written in the next control-cycle. If a continuous update of the control-register is necessary, only the control-information has to be written (the command-information does not change).
If the command/control select (A0) is logic 0, the byte transfer is control; if A0 is logic 1, the byte transfer is command.

Interface to microprocessor

The SAA1099 is a data bus based I/O peripheral. Depending on the value of the command/control signal (A0) the $\overline{CS}$ and $\overline{WR}$ signals control the data transfer from the microprocessor to the SAA1099. The data-transfer-acknowledge ($\overline{DTACK}$) indicates that the data transfer is completed. When, during the write cycle, the microprocessor recognizes the $\overline{DTACK}$, the bus cycle will be completed by the processor.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 18)	V_{DD}	−0,3 to	+ 7,5	V
Maximum input voltage	V_I	−0,3 to	+ 7,5	V
at V_{DD} = 4,5 to 5,5 V	V_I	−0,5 to	+ 7,5	V
Maximum output current	I_O	max.	10	mA
Total power dissipation	P_{tot}		500	mW
Storage temperature range	T_{stg}	−55 to	+ 125	°C
Operating ambient temperature range	T_{amb}	0 to	+ 70	°C
Electrostatic handling*	V_{es}	−1000 to	+ 1000	V

* Equivalent to discharging a 250 μF capacitor through a 1 kΩ series resistor.

D.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	70	100	mA
Reference current (note 1)	I_{ref}	100	250	400	μA
INPUTS					
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input voltage LOW	V_{IL}	−0,5	–	0,8	V
Input leakage current	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	10	pF
OUTPUTS					
$\overline{DTACK}$ (open drain; note 2)					
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Voltage on pin 7 (OFF state)	V_{7-9}	−0,3	–	6,0	V
Output capacitance (OFF state)	C_O	–	–	10	pF
Load capacitance	C_L	–	–	150	pF
Output leakage current (OFF state)	$-I_{LO}$	–	–	10	μA
Audio outputs (pins 4 and 5)					
With fixed I_{ref} (note 3)					
One channel on	I_{01}/I_{ref}	90	–	120	%
Six channels on	$I_{06}/6xI_{ref}$	85	–	110	%
With I_{ref} = 250 μA; R_L = 1,5 kΩ (± 5%)					
One channel on	I_{01}/I_{ref}	90	–	110	%
Six channels on	$I_{06}/6xI_{ref}$	85	–	105	%
Output current one channel on	I_{01}	225	–	275	μA
Output current six channels on	I_{06}	1,3	–	1,6	mA
With resistor supplying I_{ref} (note 4)					
Output current one channel on	I_{01}	150	–	350	μA
Output current six channels on	I_{06}	0,9	–	1,9	mA
Load resistance	R_L	600	–	–	Ω
D.C. leakage current all channels off	$-I_{LO}$	–	–	10	μA
Maximum current difference between left and right current sinks (note 5)	$\pm I_{Omax}$	–	–	15	%
Signal-to-noise ratio (note 6)	S/N	–	tbf	–	dB

A.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; timing measurements taken at 2,0 V for a logic 1 and 0,8 V for a logic 0 unless otherwise specified (see waveforms Figs 3 and 4)

parameter	symbol	min.	typ.	max.	unit
Bus interface timing (see Fig. 3)					
A0 set-up time to $\overline{CS}$ fall	t_{ASC}	0	–	–	ns
$\overline{CS}$ LOW to $\overline{WR}$ fall	t_{CSW}	30	–	–	ns
A0 set-up time to $\overline{WR}$ fall	t_{ASW}	50	–	–	ns
$\overline{WR}$ LOW time	t_{WL}	100	–	–	ns
Data bus valid to $\overline{WR}$ rise	t_{BSW}	100	–	–	ns
$\overline{DTACK}$ fall delay from $\overline{WR}$ fall (note 7)	t_{DFW}	0	–	85	ns
A0 hold time from $\overline{WR}$ HIGH	t_{AHW}	0	–	–	ns
$\overline{CS}$ hold time from $\overline{WR}$ HIGH	t_{CHW}	0	–	–	ns
Data bus hold time from $\overline{WR}$ HIGH	t_{DHW}	0	–	–	ns
$\overline{DTACK}$ rise delay from $\overline{WR}$ HIGH	t_{DRW}	0	–	100	ns
Bus cycle time (note 8)	t_{CY}	$4t_{CLK}$	–	–	
Bus cycle time (note 9)	t_{CY}	$16t_{CLK}$	–	–	
Clock input timing (see Fig. 4)					
Clock period	t_{CLK}	120	125	255	ns
Clock LOW time	t_{LOW}	55	–	–	ns
Clock HIGH time	t_{HIGH}	55	–	–	ns

Notes to the characteristics

1. Using an external constant current generator to provide a nominal I_{ref} or external resistor connected to V_{DD}.
2. This output is short-circuit protected to V_{DD} and V_{SS}.
3. Measured with I_{ref} a constant value between 100 and 400 μA; load resistance (R_L) allowed to match E12 (5%) in all applications via:

$$R_L = 0{,}6\ [I_{ref}]^{-1} - 16\ [I_{ref}]^{-0{,}5} \pm 12\%$$

4. Measured with R_{ref} = 10 kΩ (± 5%) connected between I_{ref} and V_{DD}; R_L = 1,5 kΩ (± 5%); OUTR and OUTL short-circuit protected to V_{SS}.
5. Left and right outputs must be driven with identical configuration.
6. Sample tested value only.
7. This timing parameter only applies when no wait states are required; otherwise parameter is invalid.
8. The minimum bus cycle time of four clock periods is for loading all registers except the amplitude registers.
9. The minimum bus cycle time of 16 clock periods is for loading the amplitude registers. In a system using $\overline{DTACK}$ it is possible to achieve minimum times of 500 ns. Without $\overline{DTACK}$ the parameter given must be used.

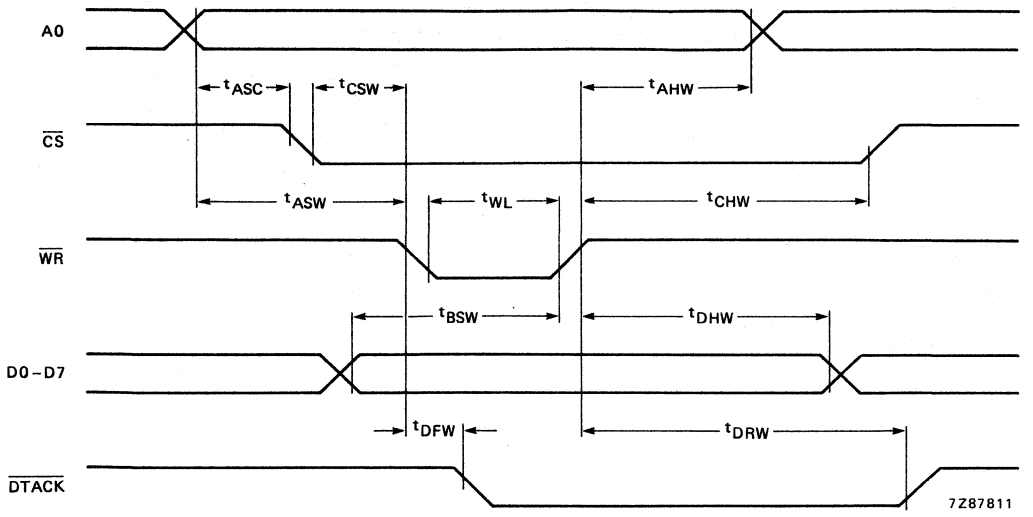


Fig. 3 Bus interface waveforms.

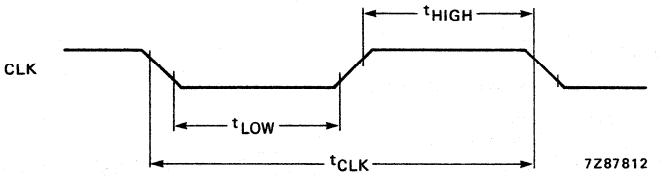


Fig. 4 Clock input waveform.

APPLICATION INFORMATION

Device operation

The SAA1099 uses pulse width modulation to achieve amplitude and envelope levels. The twelve signals are mixed in an analogue format (6 'left' and 6 'right') before leaving the chip. The amplitude and envelope signals chop the output at a minimum rate of 62,5 kHz, compared with the highest tone output of 7,81 kHz. Simple external low-pass filtering is used to remove the high frequency components.

Rates quoted are based on the input of a 8 MHz clock.

A data bus based write only structure is used to load the on-board registers. The data bus is used to load the address for a register, and subsequently the data to that register. Once the address is loaded multiple data loads to that register can be performed.

The selection of address or data is made by the single address bit A0, as shown in register maps Table 1 and Table 2.

The bus control signals $\overline{WR}$ and $\overline{CS}$ are designed to be compatible with a wide range of microprocessors, a $\overline{DTACK}$ output is included to optimise the interface with an S68000 series microprocessor. In most bus cycles $\overline{DTACK}$ will be returned immediately, this applies to all register address load cycles and all except amplitude data load cycles. With respect to amplitude data, a number of wait cycles may need to be performed, depending on the time since the previous amplitude load. $\overline{DTACK}$ will indicate the number of required waits.

Register description (see Tables 2 and 3)

The amplitudes are assigned with 'left' and 'right' components in the same byte, on a channel by channel basis. The spare locations that are left between blocks of registers is to allow for future expansion, and should be written as zero's. The tone within an octave is defined by eight bits and the octave by three bits. Note that octaves are paired (0/1, 2/3 etc.). The frequency and noise enables are grouped together for ease of programming. The controls for noise 'colour' (clock rate) are grouped in one byte.

The envelope registers are positioned in adjacent locations. There are two types of envelope controls, direct acting controls and buffered controls. The direct acting controls always take immediate effect, and are:

- Envelope enable (reset)
- Envelope resolution (16/8 level)

The buffered controls are acted upon only at the times shown in Fig. 5 and control selection of:

- Envelope clock source
- Waveform type
- Inverted/non-inverted 'right' component

Table 1 External memory map

select	data bus inputs								operations
A0	D7	D6	D5	D4	D3	D2	D1	D0	
0	D7	D6	D5	D4	D3	D2	D1	D0	data for internal registers
1	X	X	X	A4	A3	A2	A1	A0	internal register address

Where X = don't care state.

Table 2 Internal register map

register address	data bus inputs D7	D6	D5	D4	D3	D2	D1	D0	operations
00	AR03	AR02	AR01	AR00	AL03	AL02	AL01	AL00	amplitude 0 right channel; left channel
01	1	1	1	1	1	1	1	1	amplitude 1 right/left
02	2	2	2	2	2	2	2	2	amplitude 2 right/left
03	3	3	3	3	3	3	3	3	amplitude 3 right/left
04	4	4	4	4	4	4	4	4	amplitude 4 right/left
05	5	5	5	5	5	5	5	5	amplitude 5 right/left
06	X	X	X	X	X	X	X	X	
07	X	X	X	X	X	X	X	X	
08	F07	F06	F05	F04	F03	F02	F01	F00	frequency of tone 0
09	1	1	1	1	1	1	1	1	frequency of tone 1
0A	2	2	2	2	2	2	2	2	frequency of tone 2
0B	3	3	3	3	3	3	3	3	frequency of tone 3
0C	4	4	4	4	4	4	4	4	frequency of tone 4
0D	F57	F56	F55	F54	F53	F52	F51	F50	frequency of tone 5
0E	X	X	X	X	X	X	X	X	
0F	X	X	X	X	X	X	X	X	
10	X	012	011	010	X	002	001	000	octave 1; octave 0
11	X	032	031	030	X	022	021	020	octave 3; octave 2
12	X	052	051	050	X	042	041	040	octave 5; octave 4
13	X	X	X	X	X	X	X	X	
14	X	X	FE5	FE4	FE3	FE2	FE1	FE0	frequency enable
15	X	X	NE5	NE4	NE3	NE2	NE1	NE0	noise enable
16	X	X	N11	N10	X	X	N01	N00	noise generator 1; noise generator 0
17	X	X	X	X	X	X	X	X	
18	E07	X	E05	E04	E03	E02	E01	E00	envelope generator 0
19	E17	X	E15	E14	E13	E12	E11	E10	envelope generator 1
1A	X	X	X	X	X	X	X	X	
1B	X	X	X	X	X	X	X	X	
1C	X	X	X	X	X	X	RST	SE	frequency reset (all channels) / sound enable (all channels)
1D	X	X	X	X	X	X	X	X	
1E	X	X	X	X	X	X	X	X	
1F	X	X	X	X	X	X	X	X	

Where:
All don't cares (X) should be written as zero's.
00 to 1F block of registers repeats eight times in the block between addresses 00 to FF (full internal memory map).

APPLICATION INFORMATION (continued)

Table 3 Register description

bit	description
ARn3; ARn2; ARn1; ARn0 (n = 0,5)	4 bits for amplitude control of right channel 0 0 0 0 minimum amplitude (off) 1 1 1 1 maximum amplitude
ALn3; ALn2; ALn1; ALn0 (n = 0,5)	4 bits for amplitude control of left channel 0 0 0 0 minimum amplitude (off) 1 1 1 1 maximum amplitude
Fn7 to Fn0 (n = 0,5)	8 bits for frequency control of the six frequency generators 0 0 0 0 0 0 0 0 lowest frequency 1 1 1 1 1 1 1 1 highest frequency
On2; On1; On0 (n = 0,5)	3 bits for octave control 0 0 0 lowest octave (31 Hz to 61 Hz) 0 0 1 (61 Hz to 122 Hz) 0 1 0 (122 Hz to 244 Hz) 0 1 1 (245 Hz to 488 Hz) 1 0 0 (489 Hz to 977 Hz) 1 0 1 (978 Hz to 1,95 kHz) 1 1 0 (1,96 kHz to 3,91 kHz) 1 1 1 highest octave (3,91 kHz to 7,81 kHz)
FEn (n = 0,5)	frequency enable bit (one tone per generator) FEn = 0 indicates that frequency 'n' is off
NEn (n = 0,5)	noise enable bit (one tone per generator) NEn = 0 indicates that noise 'n' is off
Nn1; Nn0 (n = 0,1)	2 bits for noise generator control. These bits select the noise generator rate (noise 'colour') Nn1 Nn0 clock frequency 0 0 31,3 kHz 0 1 15,6 kHz 1 0 7,6 kHz 1 1 61 Hz to 15,6 kHz (frequency generator 0/3)

bit	description
En7; En5 to En0 (n = 0,1)	7 bits for envelope control En0 0 left and right component have the same envelope 1 right component has inverse of envelope that is applied to left component En3 En2 En1 0 0 0 zero amplitude 0 0 1 maximum amplitude 0 1 0 single decay 0 1 1 repetitive decay 1 0 0 single triangular 1 0 1 repetitive triangular 1 1 0 single attack 1 1 1 repetitive attack En4 0 4 bits for envelope control (maximum frequency = 977 Hz) 1 3 bits for envelope control (maximum frequency = 1,95 kHz) En5 0 internal envelope clock (frequency generator 1 or 4) 1 external envelope clock (address write pulse) En7 0 reset (no envelope control) 1 envelope control enabled
SE	SE sound enable for all channels (reset on power-up to 0) 0 all channels disabled 1 all channels enabled
RST	Reset signal to all frequency generators 0 all generators enabled 1 all generators reset and synchronized

Note

All rates given are based on the input of a 8 MHz clock.

APPLICATION INFORMATION (continued)

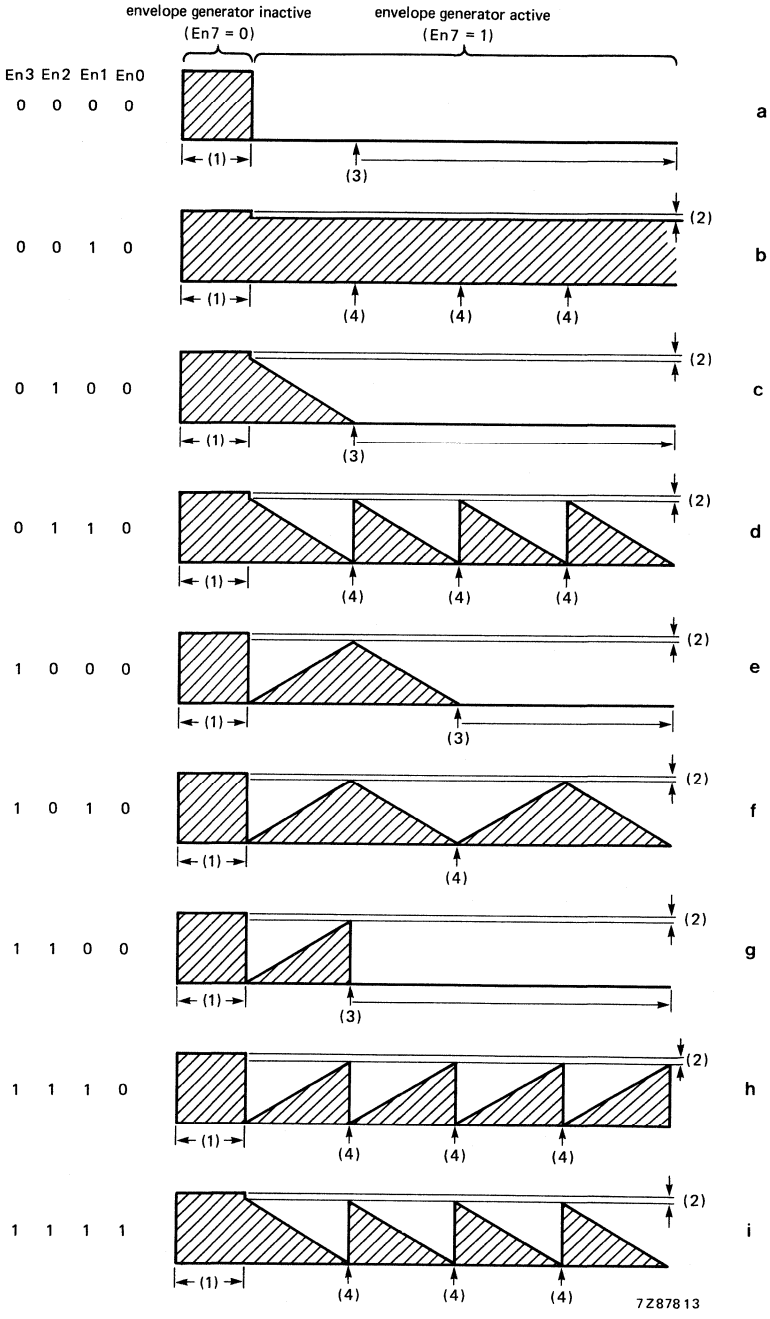


Fig. 5 Envelope waveforms.

Notes to Fig. 5

(1) The level at this time is under amplitude control only (En7 = 0; no envelope).

(2) When the generator is active (En7 = 1) the maximum level possible is 7/8ths of the amplitude level.

(3) After position (3) the buffered controls will be acted upon when loaded.

(4) At positions (4) the buffered controls will be acted upon if already loaded.

(5) Waveforms 'a' to 'h' show the left channel (En0 = 0; left and right components have the same envelope).
Waveform 'i' shows the right channel (En0 = 1; right component inverse of envelope applied to left).

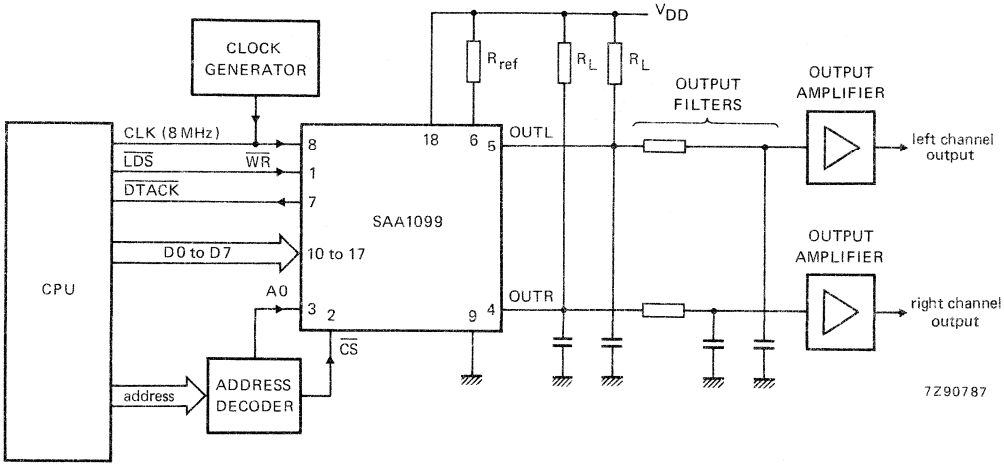


Fig. 6 Typical application circuit diagram.

Philips Semiconductors

Data sheet	
status	Product specification
code	
date of issue	January 1990

SAA1101
Universal sync generator (USG)

FEATURES

- Programmable to seven standards
- Additional outputs to simplify signal processing
- Can be synchronized to an external sync. signal
- Option to select the 524/624 line mode instead of the 525/625 line mode
- Lock from subcarrier to line frequency

GENERAL DESCRIPTION

The SAA1101 is a Universal Sync Generator (USG) and is designed for application in video sources such as cameras, film scanners, video generators and associated apparatus. The circuit can be considered as a successor to the SAA1043 sync generator and the SAA1044 subcarrier coupling IC.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage range (pin 28)	4.5	5.5	V
I_{DD}	quiescent supply current	–	10	µA
f_{OSC}	clock oscillator frequency	–	24	MHz

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA1101P	28	DIL	plastic	SOT117
SAA1101T	28	SO28	plastic	SOT136A

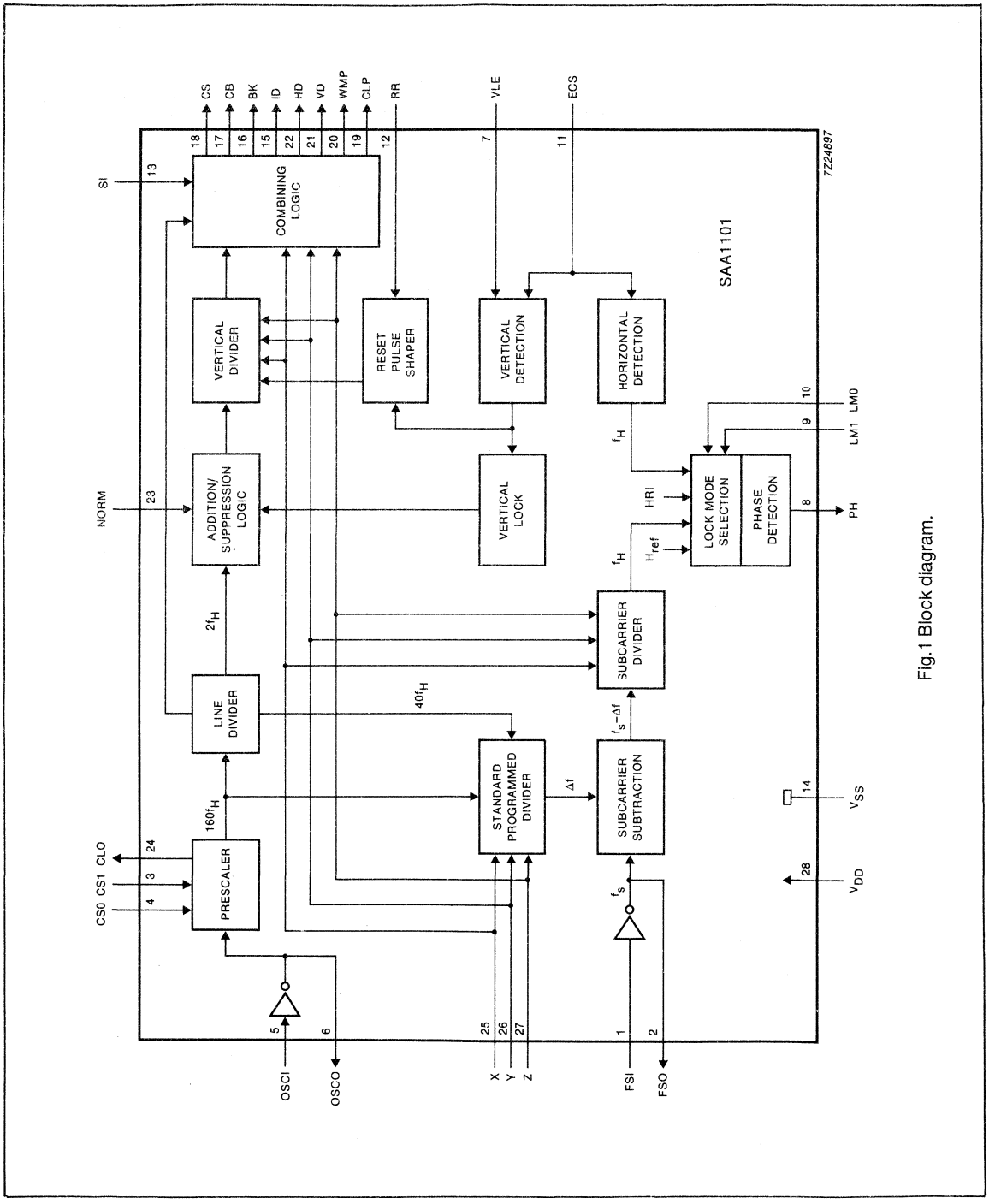


Fig.1 Block diagram.

Universal sync generator (USG) SAA1101

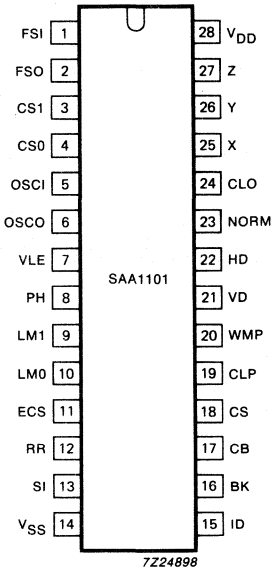


Fig.2 Pinning configuration; SOT117.

PINNING

SYMBOL	PIN	DESCRIPTION
FSI	1	subcarrier oscillator input, where f_{max} = 5 MHz
FSO	2	subcarrier oscillator output
CS1	3	clock frequency selection – CMOS input
CS0	4	clock frequency selection – CMOS input
OSCI	5	clock oscillator input, where f_{max} = 24 MHz
OSCO	6	clock oscillator output
VLE	7	vertical in-lock enable – CMOS input
PH	8	phase detector output – 3-state output
LM1	9	lock mode selection – CMOS input
LM0	10	lock mode selection – CMOS input
ECS	11	external composite sync. signal – CMOS Schmitt-trigger input
RR	12	frame reset – CMOS Schmitt-trigger input
SI	13	set identification, used to set the correct field sequence in PAL-mode. The correction (inversion of fH2) is done at the left-hand slope of the SI-pulse. Minimum pulse width is 800 ns. CMOS Schmitt-trigger input.
V_{SS}	14	ground
ID	15	identification – push-pull output
BK	16	burst key (PAL/NTSC), chroma-blanking (SECAM) – push-pull output
CB	17	composite blanking – push-pull output
CS	18	composite sync. – push-pull output
CLP	19	clamp pulse – push-pull output
WMP	20	white measurement pulse – 3-state output
VD	21	vertical drive pulse – push-pull output
HD	22	horizontal drive pulse – push-pull output
NORM	23	used with X, Y and Z to select TV system; NORM = 0, 625/525 line mode (standard); NORM = 1, 624/524 line mode – CMOS input
CLO	24	clock output – push-pull output
X	25	TV system selection input – CMOS input
Y	26	TV system selection input – CMOS input
Z	27	TV system selection input – CMOS input
V_{DD}	28	voltage supply

FUNCTIONAL DESCRIPTION

Generation of pulses

Generation of standard pulses such as sync, blanking and burst for TV systems: PAL B/G, PALN, PALM, SECAM and NTSC. In addition a number of non-standard pulses have been supplied to simplify signal processing. These signals include – horizontal drive, vertical drive, clamp pulse, identification etc. It is possible to select the 524/624 line mode instead of the 525/625 line mode for all the above TV systems for applications such as robotics, games and computers.

Lock modes

The USG offers four lock modes:

- Lock from the subcarrier
- Slow sync. lock, external H_{ref}
- Slow sync. lock, internal H_{ref}
- Fast sync. lock, internal H_{ref}

LOCK FROM SUBCARRIER

Lock from subcarrier to the line frequency for the above mentioned TV systems is given below; the horizontal frequency (f_H) = 15.625 kHz for 625 line systems and 15.734264 kHz for 525 line systems.

SECAM (1 and 2)	$282f_H$
PALN	$229.2516f_H$
NTSC (1 and 2)	$227.5f_H$
PALM	$227.25f_H$
PAL B/G	$283.7516f_H$

These relationships are obtained by the use of a phase locked loop and the internal programmed divider chain, see Fig. 3(a).

LOCK TO AN EXTERNAL SIGNAL SOURCE

The following methods can be used to lock to an external signal source:

1. Sync. lock slow; the line frequency is locked to an external signal. The line and frame information are extracted from the external sync. signal and used separately in the lock system. The line information is used in a phase-locked loop where external and internal line frequencies are compared by the same phase detector as is used for the subcarrier lock. The external frame information is compared with the internal frame in a slow lock system; mismatch of internal and external frames will result in the addition or suppression of one line depending on the direction of the fault. The maximum lock time for frame lock is 6.25 s, see Fig. 3(b).
2. Sync. lock fast. A fast lock of frames is possible with a frame reset which is extracted out of the incoming external sync. signal, see Fig. 3(c).
3. Sync. lock with external reference. Lock of an external sync. signal to the line frequency with an external line reference to make possible a shifted lock. The subcarrier input is, in this case, used as an external input for the horizontal reference, see Fig. 3(d).

SELECTION OF LOCK MODE

Lock mode is selected using the inputs LM0 and LM1 as illustrated in the Table below.

LM0	LM1	SELECTION
0	0	lock to subcarrier
0	1	slow sync. lock external H_{ref}
1	0	slow sync. lock internal H_{ref}
1	1	fast sync. lock internal H_{ref}

The different lock modes are illustrated by the following figures:

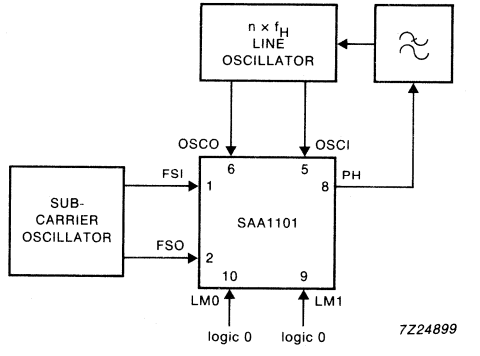


Fig.3(a) Lock to subcarrier.

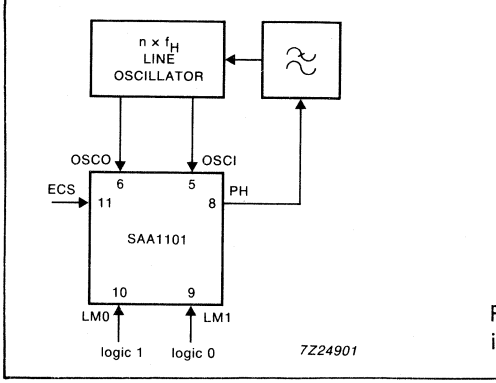


Fig.3(b) Slow sync lock, internal H_{ref}

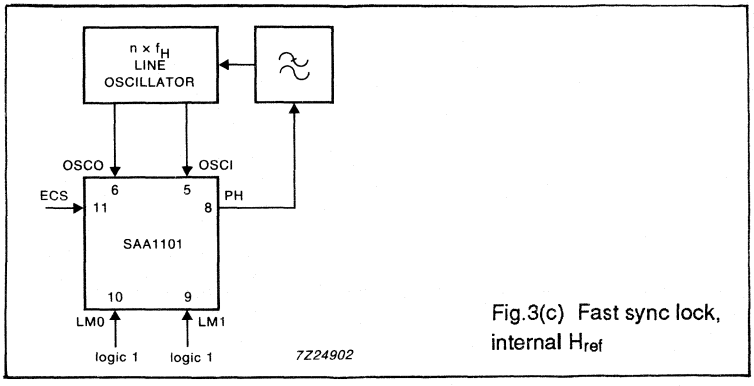


Fig.3(c) Fast sync lock, internal H_{ref}

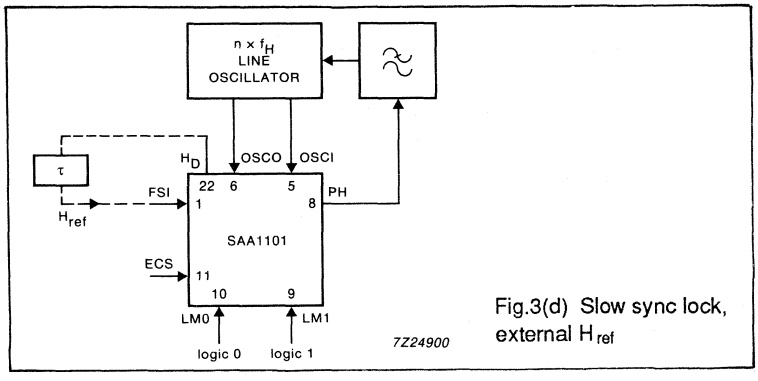


Fig.3(d) Slow sync lock, external H_{ref}

LOCK WITH HORIZONTAL AND VERTICAL SIGNALS

(slow lock modes only)

It is possible to use horizontal and vertical signals instead of composite sync signals. The connections in this situation are: the external horizontal signal is connected to the ECS input (pin 11) and the vertical signal to the RR input (pin 12). The HIGH time of the horizontal pulse must be less than 14.4 μs, otherwise it will be detected as being a vertical pulse and will corrupt the vertical slow lock system.

Selection of Clock Frequency

The clock frequency is selected using the CS0 and CS1 inputs as illustrated below.

CS0	CS1	FREQUENCY	625 LINES	525 LINES	UNITS
0	0	$160f_H$	2.5	2.517482	MHz
0	1	$320f_H$	5	5.034964	MHz
1	0	$960f_H$	15	15.104893	MHz
1	1	$1440f_H$	22.5	22.657340	MHz

Where the horizontal frequency, f_H = 15.625 kHz for 625 lines and 15.734264 kHz for 525 lines.

Oscillators

The subcarrier oscillator has FSI as its input and FSO as its output. It is always used as a crystal oscillator with a series resonance crystal with parallel load capacitor. The maximum frequency, f_{max} = 5 MHz and the load capacitor, $C_L = 10 < C_L < 35$ pF.

The clock oscillator has OSCI as its input and OSCO as its output. It can be used with an LC oscillator or a series resonance crystal with parallel load capacitor (Fig.4). The maximum frequency, f_{max} = 24 MHz and the load capacitor, $C_L = 10 < C_L < 35$ pF.

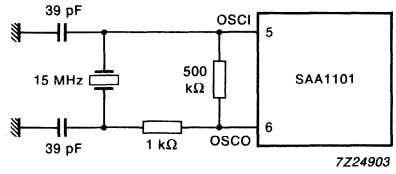


Fig.4 Crystal oscillator circuit.

Selection of TV System

Selection of the required TV system is achieved by the X, Y and Z inputs as illustrated by the following Table.

SYSTEM	X	Y	Z
SECAM1	0	0	0
PALN	0	0	1
NTSC1	0	1	0
PALM	0	1	1
SECAM2	1	0	0 (with identifier)
PAL B/G	1	0	1
NTSC2	1	1	0 (short blanking)

Selection of 625/525 (standard; interlaced mode) or 624/524 lines (non-interlaced mode)

Selection is achieved using the NORM input. When NORM = 0, 625/525 (standard) lines are selected; when NORM = 1, 624/524 line are selected.

Output Dimensions

All push-pull outputs: standard output 2 mA.

White measurement pulse, WMP: 3-state output 2 mA.

Phase detector, PH: 3-state output 2 mA.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+7	V
V_I	input voltage	−0.5	V_{DD} + 0.5 *	V
I_I	maximum input current	–	±10	mA
I_O	maximum output current	–	±10	mA
I_{DD}	maximum supply current in V_{DD}	–	25	mA
P_{tot}	maximum power dissipation	–	400	mW
T_{stg}	storage temperature range	−55	+150	°C

* Input voltage should not exceed 7 V.

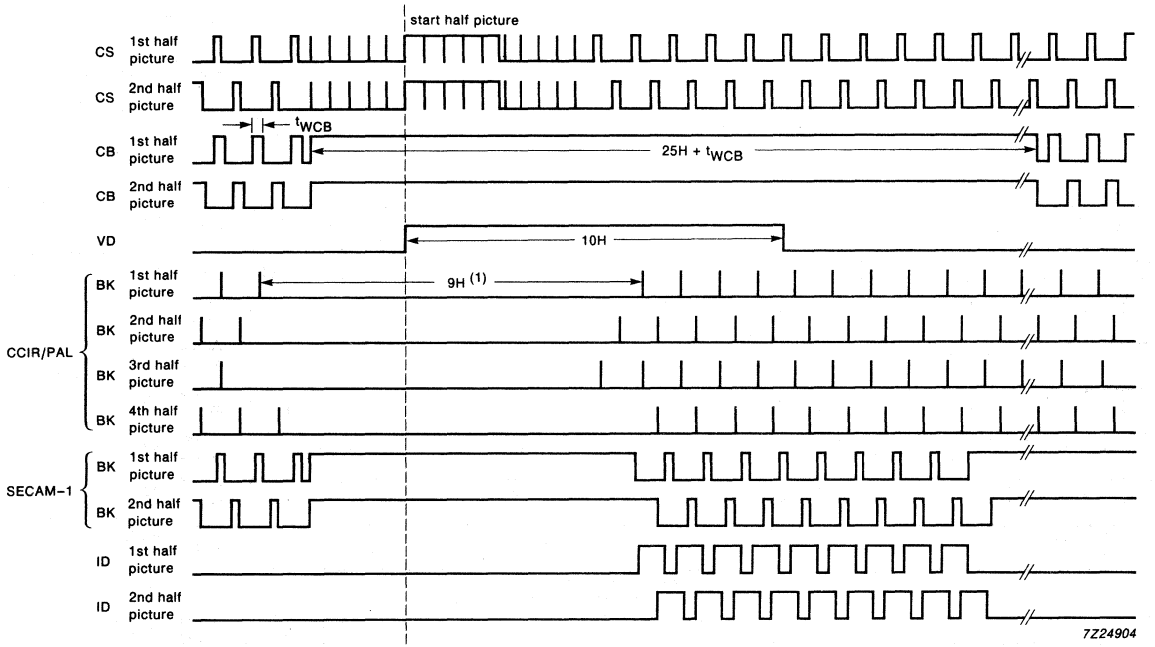
CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = -25 to +70 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		4.5	–	5.5	V
I_{DD}	supply current (quiescent)	T_{amb} = 25 °C	–	–	10	µA
Inputs						
$\pm I_I$	input leakage current	T_{amb} = 25 °C	–	–	100	nA
CMOS COMPATIBLE; X, Y, Z, NORM, CS0, CS1, LM0, LM1 AND VLE						
V_{IH}	input voltage HIGH		$0.7V_{DD}$	–	–	V
V_{IL}	input voltage LOW		–	–	$0.3V_{DD}$	V
SCHMITT TRIGGER INPUTS; ECS, RR AND SI						
V_{T+}	positive-going threshold		–	2.5	4	V
V_{T-}	negative-going threshold		1	1.5	–	V
V_H	hysteresis		0.4	1	–	V
OSCILLATOR INPUTS; OSCI AND FSI						
V_{IH}	input voltage HIGH		$0.7V_{DD}$	-	–	V
V_{IL}	input voltage LOW		–	–	$0.3V_{DD}$	V
Outputs						
PUSH-PULL OUTPUTS; CB, CS, BK, ID, HD, VD, CLP AND CLO						
V_{OH}	output voltage HIGH	$-I_O$ = 2 mA; V_{DD} = 5 V	4.5	–	–	V
V_{OL}	output voltage LOW	I_O = 2 mA; V_{DD} = 5 V	–	–	0.5	V
OSCILLATOR OUTPUTS; OSCO AND FSO						
V_{OH}	output voltage HIGH	$-I_O$ = 0.75 mA; V_{DD} = 5 V	4.5	–	–	V
V_{OL}	output voltage LOW	I_O = 0.75 mA; V_{DD} = 5 V	–	–	0.5	V
3-STATE OUTPUTS; WMP AND PH						
V_{OH}	output voltage HIGH	$-I_O$ = 2 mA; V_{DD} = 5 V	4.5	–	–	V
V_{OL}	output voltage LOW	I_O = 2 mA; V_{DD} = 5 V	–	–	0.5	V
$\pm I_{OZ}$	OFF-state current	T_{amb} = 25 °C	–	–	50	nA

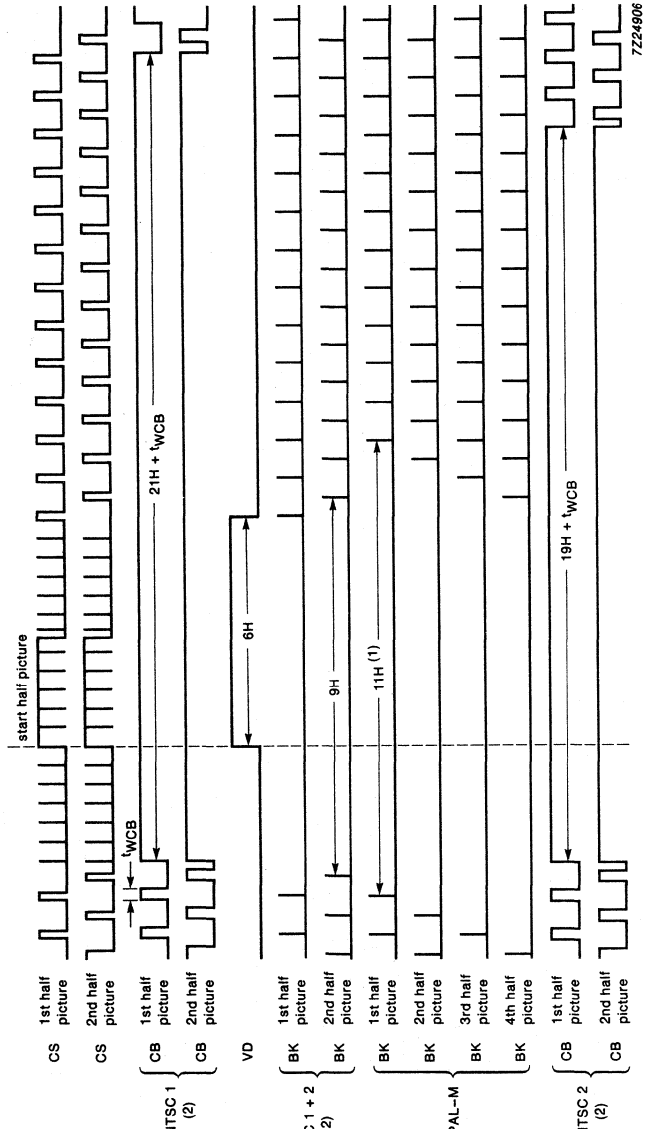
OUTPUT WAVEFORMS

The output waveforms for the different modes of operation are illustrated by Figs 5 and 6.



(1) H = 1 horizontal scan.

Fig.5 Typical output waveforms for PAL/CCIR and SECAM. In the 624-line mode the output waveforms are identical to the first half picture of PAL/CCIR and are not interlaced.



(1) H = 1 horizontal scan.
(2) NTSC mode reset; the fourth half picture is identical to the second half picture for NTSC.

Fig.6 Typical output waveforms for NTSC and PAL-M. In the 524-line mode the output waveforms are identical to the first half picture of NTSC and are not interlaced.

WAVEFORM TIMING

The waveform timing depends on the frequency of the oscillator input (f_{OSCI}). This is illustrated in the table below as the number (N) of oscillations at OSCI. The timings are derived from N x t_{OSCI} ± 100 ns.
One horizontal scan (H) = 320 x t_{OSCI} = $1/f_H$.
Where t_{OSCI} = 200 ns for PAL/SECAM and 198.6 ns for NTSC/PAL-M

SYMBOL	PARAMETER	PAL	NTSC	PAL-M	SECAM	UNIT	N
Composite sync (CS)							
t_{WSC1}	horizontal sync pulse width	4.8	4.77	4.77	4.8	µs	24
t_{WSC2}	equalizing pulse width	2.4	2.38	2.38	2.4	µs	12
t_{WSC3}	serration pulse width	4.8	4.77	4.77	4.8	µs	24
-	duration of pre-equalizing pulses	2.5	3	3	2.5	H	-
-	duration of post-equalizing pulses	2.5	3	3	2.5	H	-
-	duration of serration pulses	2.5	3	3.5	2.5	H	-
Composite blanking (CB) HORIZONTAL BLANKING PULSE WIDTH							
t_{WCB}	PAL/SECAM/PAL-M	12	–	11.12	12	µs	60
t_{WCB}	NTSC1	–	11.12	–	–	µs	56
t_{WCB}	NTSC2	–	10.53 *	–	–	µs	53
FRONT PORCH							
t_{PCBCS}	front porch	1.6	1.59	1.59	1.6	µs	8
DURATION OF VERTICAL BLANKING							
-	PAL/SECAM/PAL-M	25H + t_{WCB}	–	21H + t_{WCB}	25H + t_{WCB}	–	-
-	NTSC1	–	21H + t_{WCB}	–	–	–	-
-	NTSC2	–	19H + t_{WCB}	–	–	–	-
Burst key (BK) (not SECAM)							
t_{WBK}	burst key pulse width	2.4	2.38	2.38	–	µs	12
t_{PCSBK}	CS to burst key delay	5.6	5.56	5.76	–	µs	28
-	burst suppression	9	9	11	–	H	-

* Horizontal blanking pulse width for NTSC2 can be 11.12 µs maximum

SYMBOL	PARAMETER	PAL	NTSC	PAL-M	SECAM	UNIT	N
Burst key (BK) (not SECAM) (continued) POSITION OF BURST SUPPRESSION							
-	first half picture	H623 to H6	H523 to H6	H523 to H8	–	–	-
-	second half picture	H310 to H318	H261 to H269	H260 to H270	–	–	-
-	third half picture	H622 to H5	H523 to H6	H522 to H7	–	–	-
-	fourth half picture	H311 to H319	H261 to H269	H259 to H269	–	–	-
Burst key (BK) (SECAM)							
t_{WBK}	chroma pulse width	–	–	–	7.2	µs	36
t_{PBKCS}	CS to chroma delay	–	–	–	1.6	µs	8
DURATION OF VERTICAL BLANKING							
-	SECAM1	–	–	–	note 1	–	-
-	SECAM2	–	–	–	note 2	–	-
Clamp pulse (CLP)							
t_{WCLP}	clamp pulse width	2.4	2.38	2.38	2.4	µs	12
t_{PCSCLP}	CS to CLP delay	1.6	1.59	1.59	1.6	µs	8
Horizontal drive (HD)							
t_{WHD}	pulse width	7.2	7.15	7.15	7.2	µs	36
t_{PHDCS}	CS to HD delay	0.8	0.79	0.79	0.8	µs	4
-	repetition period	64	63.56	63.56	64	µs	-
Vertical drive (VD)							
-	VD duration	10	6	6	10	H	-
t_{PVDCS}	CS to VD delay	1.6	1.59	1.59	1.6	µs	8
White measurement pulse (WMP)							
-	pulse width	2.4	2.38	2.38	2.4	µs	12
-	CS to WMP delay	34.4	34.16	34.16	34.4	µs	172
-	duration of WMP	10	9	9	10	H	-

WAVEFORM TIMING (CONTINUED)

SYMBOL	PARAMETER	PAL	NTSC	PAL-M	SECAM	UNIT	N
White measurement pulse (WMP) (continued) POSITION OF WMP							
-	first half picture	H163 to H173	H134 to H143	H134 to H143	H163 to H173	–	-
-	second half picture	H475 to H485	H396 to H405	H396 to H405	H475 to H485	–	-
Identification (ID)							
t_{WID}	pulse width	12	11.12	11.12	12	µs	60
t_{PIDCS}	CS to ID delay	1.6	1.59	1.59	1.6	µs	8
POSITION OF ID							
-	first half picture	H7 to H15	H8 to H22	H8 to H22	H7 to H15	–	-
-	second half picture	H320 to H328	H271 to H285	H271 to H285	H320 to H328	–	-

Notes to the characteristics

1. SECAM1, first half picture: 25H + t_{WBK} except H320 to H328. Second half picture: 24.5H + t_{WBK} except H7 to H15.

2. SECAM2, first half picture: 25H + t_{WBK}. Second half picture: 24.5H + t_{WBK}.

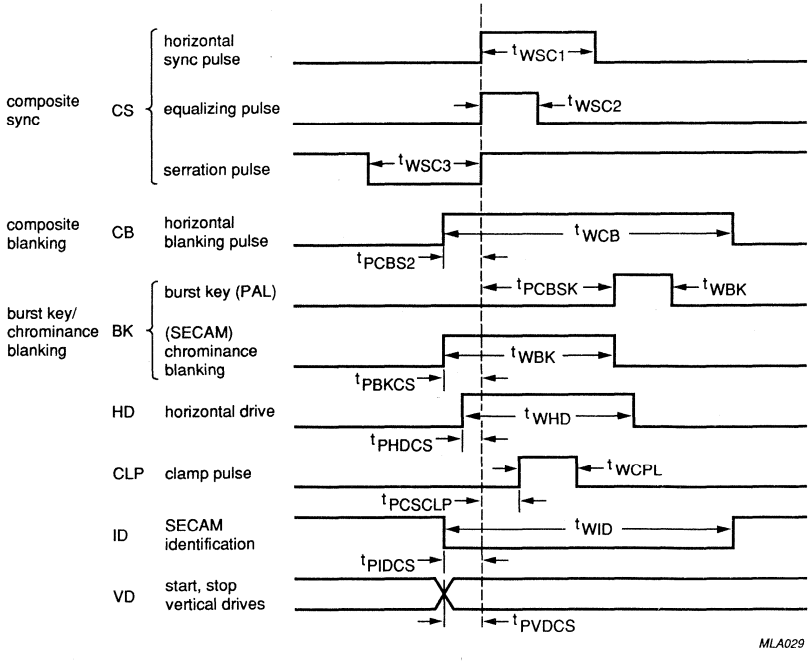


Fig.7 Waveform timing.

TUNER SWITCHING CIRCUIT

The SAA1300 is for switching on and off the supply lines of various circuit parts via an I²C bus signal. Furthermore, it can be used to supply current for switching diodes in radio and television tuners. It contains 5 output stages, which are capable of supplying up to 85 mA in the ON state or sinking up to −100 μA in the OFF state.

Current limiting and short-circuit protection are included. The output stages are driven by a shift register/latch combination which is loaded via data from the I²C bus. A power-on reset of the latches ensures the OFF state of the output stages (OUT 2 to OUT 5) without data reception from the I²C bus. A subaddressing system allows the connection of up to three circuits on the same I²C bus lines; one of the outputs (OUT 1, pin 7) can also be used as an input to select the device via a simple internal A/D converter.

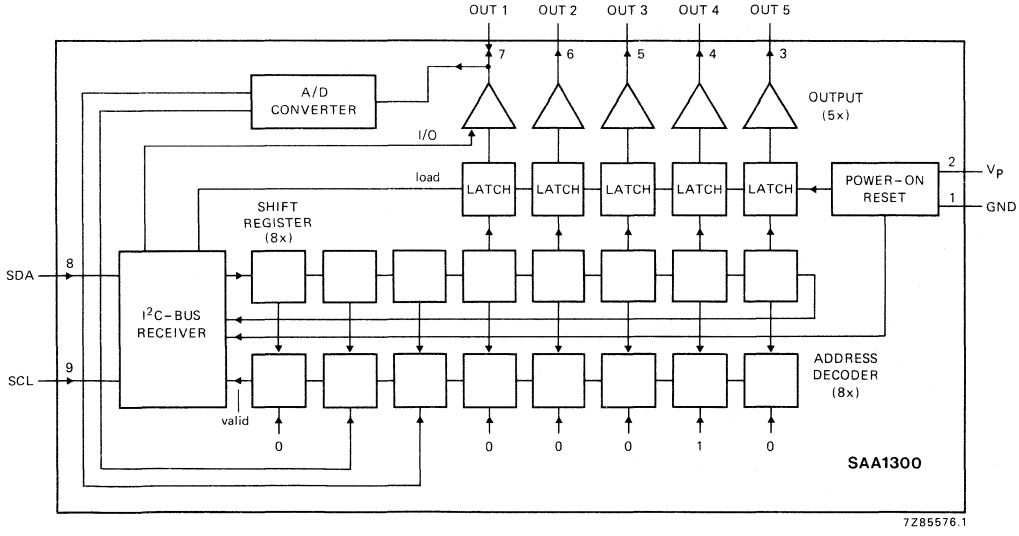


Fig. 1 Block diagram.

PACKAGE OUTLINE

9-lead SIL; plastic (SOT142).

PINNING

pin no.	symbol	function
1	GND	ground
2	V_P	positive supply
3	OUT 5	outputs
4	OUT 4	
5	OUT 3	
6	OUT 2	
7	OUT 1	output and subaddressing input
8	SDA	serial data line (I^2C bus)
9	SCL	serial clock line (I^2C bus)

I^2C BUS INFORMATION

Address, first byte

0 1 0 0 0 A B 0 where,

A	B	function	condition
0	0	general address	OUT 1 = output
0	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,L}$ (LOW)
1	0	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,H}$ (HIGH)
1	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,M}$ (MEDIUM)

Data, second byte

OUT 5, OUT 4, OUT 3, OUT 2, OUT 1, X, X, X

The I/O output stage (OUT 1) is switched as an input stage after a power-on reset. It depends on the contents of the first data transmission whether the output stage is switched as an output or remains as an input.

RATINGS

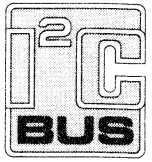
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	13,2	V
Input voltage range at SDA, SCL	V_I		−0,5 to + 6,0	V
Input voltage range at OUT 1	V_I		−0,5 to + 12,5	V
Output voltage range at OUT 1 to OUT 5	V_O		−0,5 to + 12,5	V
Input current at SDA, SCL	I_I	max.	20	mA
Input current at OUT 1	I_I	max.	20	mA
Total power dissipation	P_{tot}	max.	825	mW
Storage temperature range	T_{stg}		−40 to + 125	°C
Operating ambient temperature range	T_{amb}		−20 to + 80	°C

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 2)					
Supply voltage range	V_P	4	8	12	V
Supply current					
5 outputs LOW	I_{PL}	5	10	15	mA
5 outputs HIGH	I_{PH}	30	50	70	mA
Power-on reset level output stage in "OFF' condition	V_{PR}	–	3,5	3,8	V
Maximum power dissipation*	P_{max}	–	650	–	mW
Inputs SDA, SCL (pins 8 and 9)					
Input voltage HIGH	V_{IH}	3,0	–	5,5	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input current HIGH	$-I_{IH}$	–	–	10	μA
Input current LOW	I_{IH}	–	–	0,4	μA
Acknowledge sink current	I_{ACK}	2,5	–	–	mA
Maximum input frequency	$f_{i\,max}$	100	–	–	kHz
Outputs OUT 1 to OUT 5 (pins 3 to 7)					
Maximum output current; source: "ON"	I_{Oso}	+ 85	–	+ 150	mA
Maximum output current; source: "ON" T_{amb} = 80 °C	I_{Oso}	60	–	–	mA
Output voltage HIGH at I_{Oso} = 85 mA	V_{OH}	V_P–2	–	–	V
Output current; sink "OFF"	I_{Osi}	–100	–300	–	μA
Output voltage LOW at I_{Osi} = –100 μA	V_{OL}	–	–	100	mV
Output voltage MEDIUM at I_O = 10 mA	V_{OM}	V_P–0,5	–	–	V
OUT 1 used as subaddressing input					
Input voltage HIGH (code 1 0)	$V_{OUT\,1H}$	0,72 V_P	–	V_P	V
Input voltage MEDIUM (code 1 1)	$V_{OUT\,1M}$	0,39 V_P	–	0,61 V_P	V
Input voltage LOW (code 0 1)	$V_{OUT\,1L}$	0	–	0,28 V_P	V



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

* Outputs must not be driven simultaneously at maximum source current.

Data sheet	
status	Preliminary specification
date of issue	January 1991

SAA1310

Control interface for VHS video recorders

FEATURES

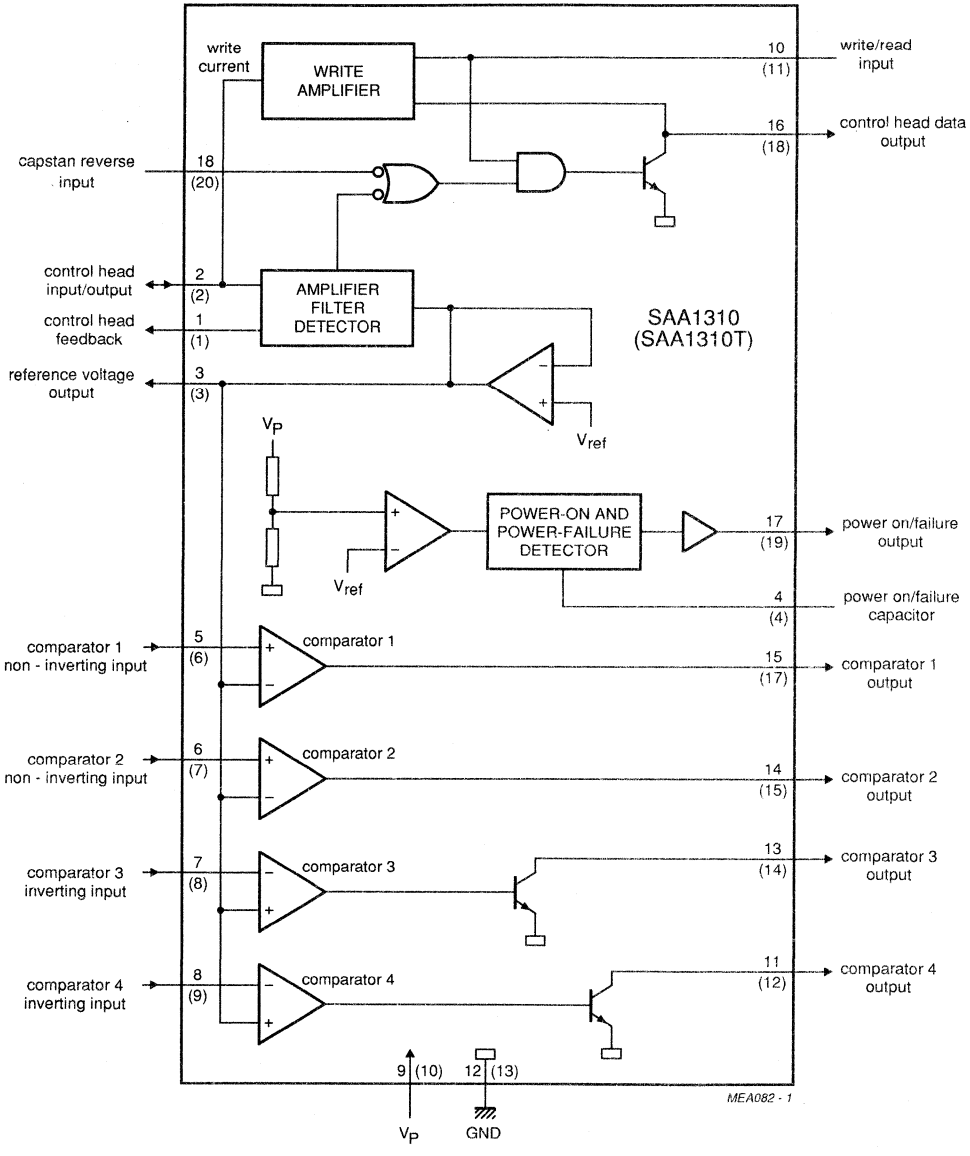
- Full support of VISS and VASS mode (VHS Index/Address Search System
- Read, write and overwrite of Tape Control/head signal (CTL)
- Power-ON and power-failure indicator
- 4 general purpose comparators for interface between sensors and microprocessor
- 2 comparators have a 100 mA output driver
- PAL and NTSC compatible

GENERAL DESCRIPTION

The SAA1310 provides an interface between the tape control head in the VHS deck-electronics.
The circuit also includes an interface between sensors in the deck mechanics and the microprocessor.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA1310	18	DIL	plastic	SOT102
SAA1310T	20	SO	plastic	SOT163A



Pin numbers in parenthesis refer to the SAA1310T.

Fig.1 Block diagram.

PIN CONFIGURATION

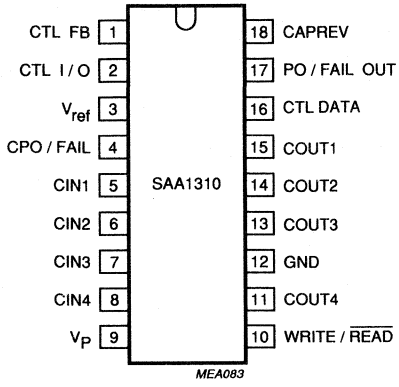


Fig.2 (a) Pin configuration for SAA1310.

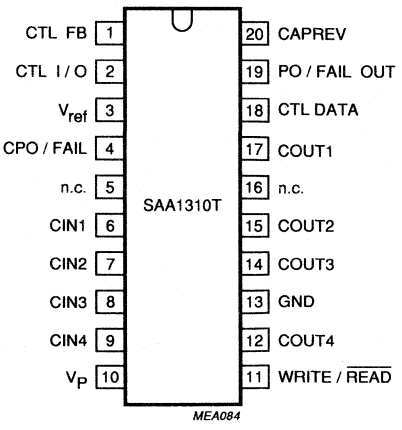


Fig.2 (b) Pin configuration for SAA1310T.

PINNING (pins in parenthesis refer to SAA1310T)

SYMBOL	PIN	DESCRIPTION
CTL FB	1 (1)	control head feedback
CTL I/O	2 (2)	control head input/output
V_{ref}	3 (3)	reference voltage output
CPO/FAIL	4 (4)	power on/failure capacitor
CIN1	5 (6)	comparator 1 input
CIN2	6 (7)	comparator 2 input
CIN3	7 (8)	comparator 3 input
CIN4	8 (9)	comparator 4 input
V_P	9 (10)	supply voltage
WRITE/$\overline{READ}$	10 (11)	write/read input
COUT4	11 (12)	comparator 4 output
GND	12 (13)	ground
COUT3	13 (14)	comparator 3 output
COUT2	14 (15)	comparator 2 output
COUT1	15 (17)	comparator 1 output
CTL DATA	16 (18)	control head data output
PO/FAIL OUT	17 (19)	power on/failure output
CAPREV	18 (20)	capstan reverse input

LIMITING VALUES (pin numbers in parenthesis refer to SAA1310T)

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage range		0	6.0	V
V_I/V_O	voltage on all pins	except pins 11 (12) and 13 (14)	0	V_P	V
V_O	output voltage on pins 11 (12) and 13 (14)		0	18	V
T_{stg}	storage temperature range		−65	+150	°C
T_{amb}	ambient temperature range		0	+70	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
R_{th}	thermal resistance (SAA1310)	75	-	K/W
R_{th}	thermal resistance (SAA1310T)	90	-	K/W

CHARACTERISTICS (pin numbers in parenthesis refer to SAA1310T)

V_P = 5 V; T_{amb} = 25 °C; all voltage referenced to pin 12 (13); according to the test set-up (see Fig.4); unless otherwise specified

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
P_d	power dissipation	note 1	-	85	-	mW
Supply pin 9 (10)						
V_P	supply voltage		4.5	5.0	5.5	V
I_P	supply current	read mode	10	15	20	mA
		write mode; duty factor = 50%	13	18	24	mA
CTL I/O pin 2 (2)						
READ MODE PIN 10 (11) < 0.5 V						
V_I	input voltage (peak-to-peak value)	f = 500 Hz	0.35	-	-	mV
		f = 30 kHz; non-linear operation	-	-	200	mV
B	bandwidth low-pass filter		-	3	-	kHz
I_b	input bias current	read mode	-	0.1	-	µA
WRITE MODE PIN 10 (11) > 3.5 V						
V_O	output voltage LOW	$I_{CTL\ I/O}$ = 3 mA; pin CTL DATA = HIGH	-	-	0.4	V
V_O	output voltage HIGH	$I_{CTL\ I/O}$ = −3 mA; pin CTL DATA = LOW	4.6	-	-	V
WRITE/READ pin 10 (11)						
V_I	input voltage	read mode	-	-	0.5	V
		write mode; analog	1.6	-	3.3	V
I_I	input current	read mode	-	-1.5	-	µA
		write mode	-	0.1	-	µA
V_{ref} pin 3 (3); note 2						
V_O	output voltage		2.4	2.5	2.6	V
I_{tot}	total current	including write current	−4	-	+4	mA
R_O	output resistance		-	0.4	0.6	Ω
CAPREV pin 18 (20)						
V_{IH}	input voltage HIGH		2.0	-	-	V
V_{IL}	input voltage LOW		-	-	0.8	V
I_{IH}	input current HIGH	V_{CAPREV} = 5 V	-	-	10	µA
I_{IH}	input current LOW	V_{CAPREV} = 0 V	−10	-	-	µA
CTL DATA pin 16 (18)						
WRITE MODE						
V_{IH}	input voltage HIGH		2.0	-	-	V
V_{IL}	input voltage LOW		-	-	0.8	V
I_{IH}	input current HIGH	$V_{CTL\ DATA}$ = 5 V	-	-	10	µA
I_{IL}	input current LOW	$V_{CTL\ DATA}$ = 0 V	−10	-	-	µA
READ MODE						
V_{OL}	output voltage LOW	I_{OL} = 0.5 mA	-	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −50 µA	2.4	-	-	V

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
CPO/FAIL and PO/FAIL OUT pin 4 (4) and 17 (19); see Fig.3						
V_O	operating voltage range	at decreasing V_P	1.5	-	5.5	V
V_{OL}	output voltage LOW	I_{OL} = 1 mA	-	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −1 mA	V_P−0.9	-	-	V
t_d	delay time	C_{CAPREV} = 68 nF	-	50	-	ms
V_{TL1}	threshold level 1		4.5	-	4.8	V
V_{TL2}	threshold level 2		-	3.5	-	V
I_O	source current pin 4		-	−3	-	µA
I_O	sink current pin 4		-	300	-	µA
$V_{O(min.)}$	minimum output voltage		-	20	-	mV
$V_{O(max.)}$	maximum output voltage		-	2.1	-	V
High output current type comparators						
CIN3 and CIN4 pins 7 (8) and 8 (9)						
V_{hys}	input hysteresis		-	10	-	mV
V_{IL}	input voltage LOW		-	-	V_{ref} −10 mV	V
V_{IH}	input voltage HIGH		V_{ref} +10 mV	-	-	V
I_{IL}	input current LOW	CIN3 = CIN4 = 0 V	−1	-	-	µA
I_{IH}	input current HIGH	CIN3 = CIN4 = V_P	-	-	+1	µA
COUT3 and COUT4 pins 13 (14) and 11 (12)						
V_{OL}	output voltage LOW	I_{OL} = 100 mA I_{OL} = 2 mA	- -	- -	1.0 0.4	V V
$\pm I_{OL}$	leakage current	output voltage HIGH; COUT3 = COUT4 = 17 V	-	-	1	µA
t_{tr}	transient time	note 3	-	0.5	-	µs
T_j	thermal protection		-	130	-	°C
Low output current type comparators						
CIN1 AND CIN2 pins 5 (6) and 6 (7)						
V_{hys}	input hysteresis		-	10	-	mV
V_{IL}	input voltage LOW		-	-	V_{ref} −10 mV	V
V_{IH}	input voltage HIGH		V_{ref} +10 mV	-	-	V
I_I	input current	CIN1 = CIN2 = 0 V CIN1 = CIN2 = V_P	−1 -	- -	- +1	µA µA
COUT1 AND COUT2 pins 15 (17) and 14 (15)						
V_{OL}	output voltage HIGH	I_{OH} = −100 µA	4.5	-	-	V
V_{OH}	output voltage LOW	I_{OL} = 2 mA	-	-	1	V
t_{tr}	transient time	note 4	-	0.5	-	µs

Notes to the characteristics

1. Without the sink current of the comparators; in write mode.
2. Minimum value of capacitor connected to this pin is 4.7 µF.
3. V_i = 100 mV p-p. Inputs connected to V_{ref} via a 10 kΩ resistor; outputs connected to V_P via a 250 Ω resistor.
4. V_i = 100 mV p-p. Inputs connected to V_{ref} via a 10 kΩ resistor; outputs connected to V_P via a 2.5 kΩ resistor.

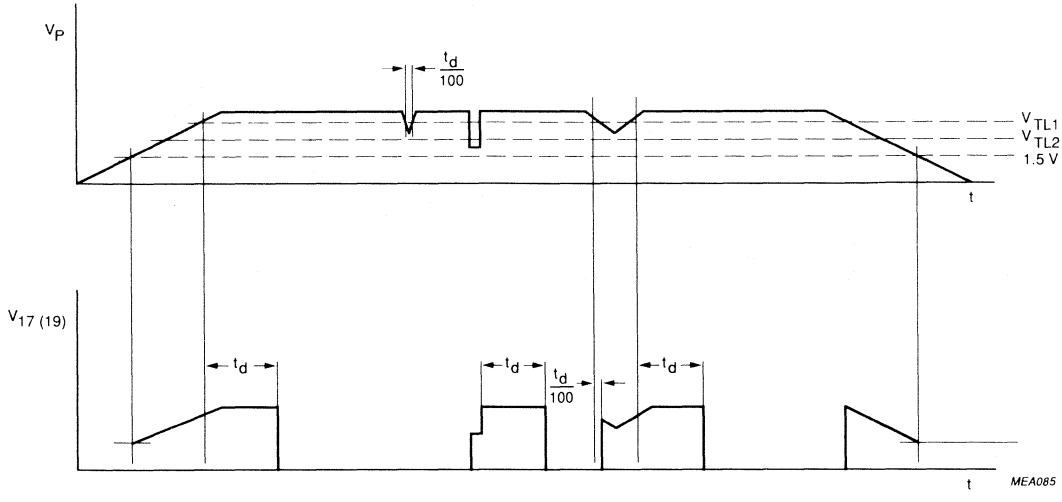


Fig.3 Power-ON and power-failure detector.

APPLICATION INFORMATION

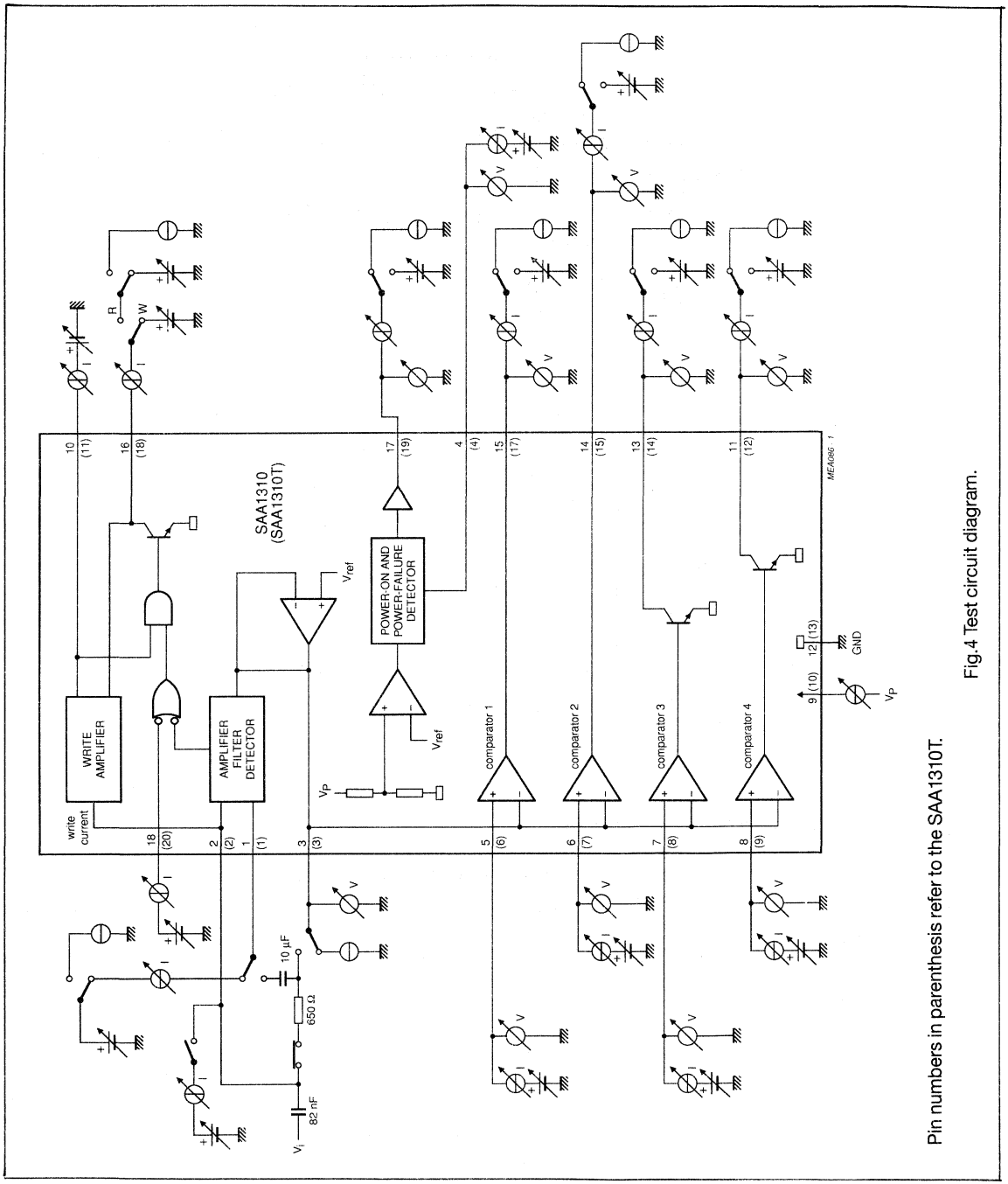
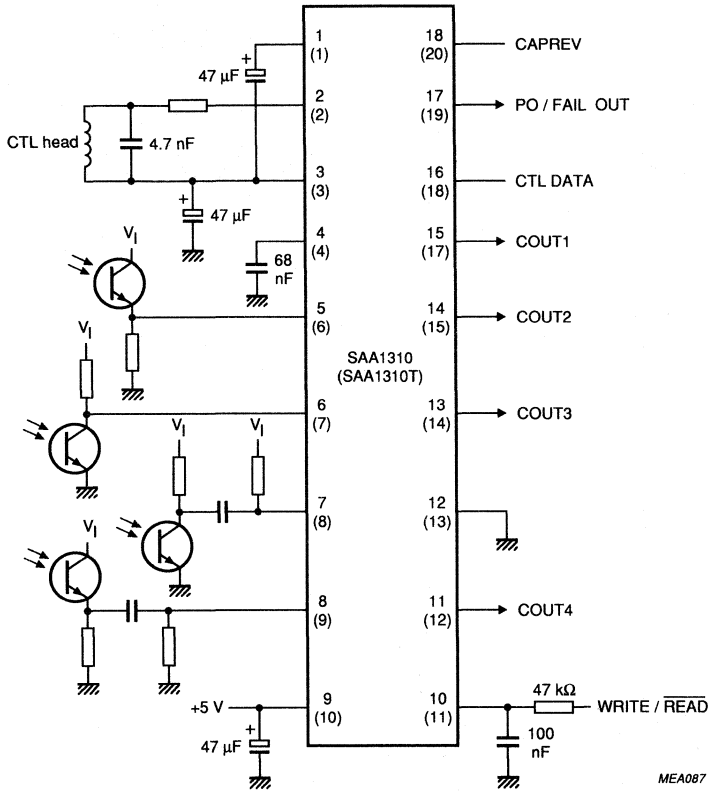


Fig.4 Test circuit diagram.

Pin numbers in parenthesis refer to the SAA1310T.

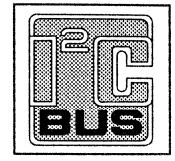


Pin numbers in parenthesis refer to the SAA1310T.

Fig.5 Application diagram.

D2MAC video decompression and descrambling

SAA1760



FEATURES

- Dual energy dispersal cancellation and video clamping for MAC satellite and Cable application
- On-chip video analog-to-digital converter
- 4 : 3 or 16 : 9 aspect ratio modes with panning
- Single or double cut rotation descrambling
- Digital YUV filters and DACs. Filter bandwidths selectable. Compatible with 100% saturated colours
- External YUV input with analog switching for "daisy chaining"
- On-chip MAC clock/data recovery with minimum external components
- Programmable delays for external filter compensation
- Sync outputs for YUV matrix, PAL/SECAM encoders and teletext decoders
- Output port (6-bits) for peripheral chip control
- PLCC68 package

GENERAL DESCRIPTION

The SAA1760 provides video decompression/descrambling and clock/data recovery functions of the Philips 2-chip MAC decoder. It provides two YUV outputs (analog luminance and chrominance) derived by decompressing and, if required, descrambling a baseband D2MAC signal. An analog YUV input is provided for multiplexing MAC and another YUV source on one of the two YUV outputs. These YUV outputs are intended for direct connection to YUV/RGB matrix chips or PAL/SECAM encoders.

The SAA1760 has an on-chip clock and data recovery sub-system implementing all functions of an analog gated phase-locked loop except for (external) loop filter and 20.25 MHz crystal components. D2MAC clock and data pins are provided for connection to the SAA1770 chip which extracts line and field synchronizing data for the chip set.

The SAA1760 is programmed (configured) by CDATA input which is supplied from the SAA1770 chip. This input specifies, for example, the video aspect ratio (4 : 3; 16 : 9), descrambling mode, descrambler control word, filter set-up and programmable delay compensation for external filters. The device also outputs bit error rate data on the CDATA pin.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5	5.5	V
I_{DD}	supply current	–	–	200	mA
f_{xtal}	oscillator frequency	20.248	20.25	20.252	MHz
T_{amb}	operating ambient temperature	0	–	70	°C
Vbw	video bandwidth (±3 dB)	–	5.5	–	MHz

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA1760	68	PLCC	plastic	SOT188CG

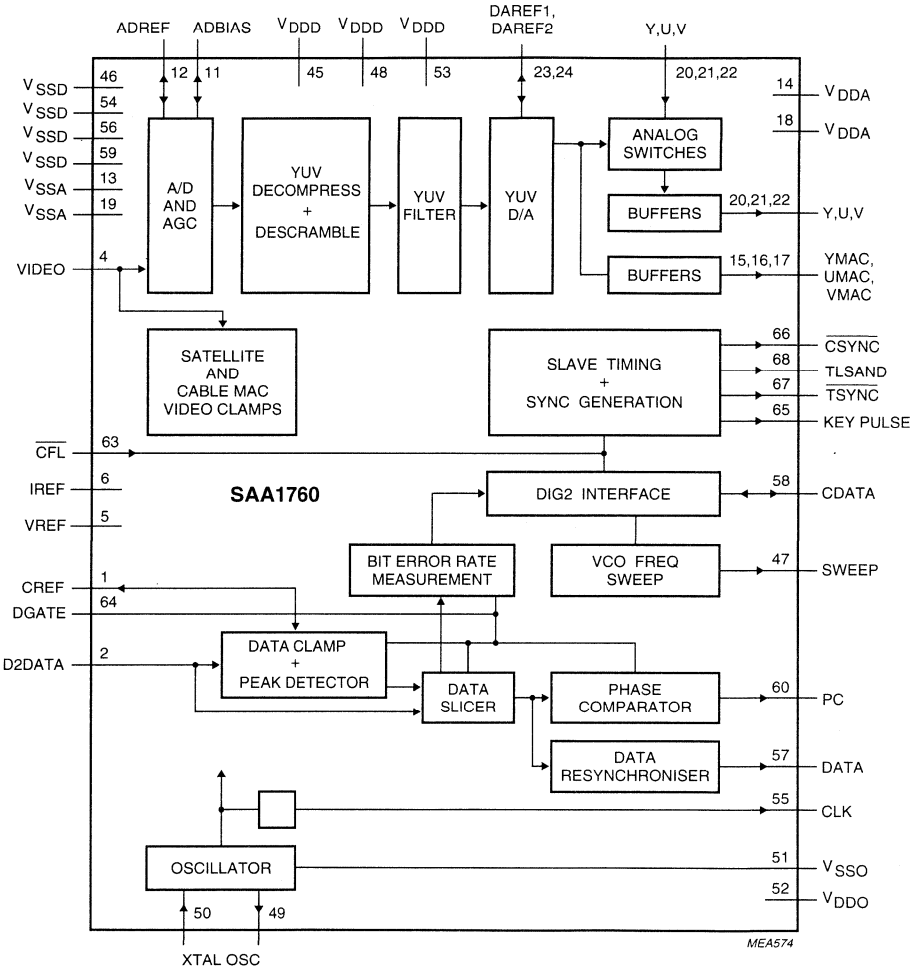


Fig.1 Block diagram.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

PINNING

SYMBOL	PIN	DESCRIPTION
CREF	1	data burst positive peak voltage storage pin. Connected to V_{SSA} via a capacitor
D2DATA	2	analog D2MAC data input. Nominal baseband signal with 800 mV peak-to-peak data burst. Input AC coupled for clamping/energy dispersal cancellation
i.c.	3	internally connected. Connect to ground for normal use
VIDEO	4	analog D2MAC baseband video input. 1 V black-to-white. Input must be AC coupled for clamping and energy dispersal cancellation
VREF	5	connection for external capacitor decoupling internal master reference voltage
IREF	6	connection for resistor defining master reference current
n.c.	7-10	not connected
ADBIAS	11	connection for ADC bias voltage decoupling capacitor
ADREF	12	connection for ADC reference voltage decoupling capacitor
V_{SSA}	13	0 V analog ground
V_{DDA}	14	+5 V supply to analog parts of chip
YMAC	15	analog luminance output. Nominally 1 V black-to-white always derived from MAC video input. Output impedance <300 Ω
VMAC	16	analog chrominance output –(R–Y). Nominally 1.05 V peak-to-peak. Output can be inverted to give (R–Y). Output impedance <300 Ω
UMAC	17	analog chrominance output –(B–Y). Nominally 1.33 V peak-to-peak. Output can be inverted to give (B–Y). Output impedance <300 Ω
V_{DDA}	18	+5 V supply to analog parts of chip
V_{SSA}	19	0 V analog ground
Y	20	analog luminance output. Nominally 1 V or 0.315 V black-to-white when Y output is derived from a MAC video input. Output level is programmable from the SAA1770. Alternatively this output corresponds to the signal on the YIN pin. Output impedance <300 Ω
V	21	analog chrominance output –(R–Y). Nominally 1.05 V peak-to-peak. Output can be inverted to give (R–Y) if derived from the MAC video input of this chip. Alternatively this output corresponds to the signal on the VIN pin. Output impedance <300 Ω
U	22	analog chrominance output –(B–Y). Nominally 1.33 V peak-to-peak. Output can be inverted to give (B–Y) if derived from the MAC video input of this chip. Alternatively this output corresponds to the signal on the UIN pin. Output impedance <300 Ω
DAREF2	23	connection for external capacitor used to store lower reference voltage for the YUV digital-to-analog converters
DAREF1	24	connection for external capacitor used to store upper reference voltage for the YUV digital-to-analog converters
YIN	25	analog luminance input. For (AC coupled) connection of external Y signal to on-chip analog switch
n.c.	26-29	not connected

SYMBOL	PIN	DESCRIPTION
UIN	30	analog chrominance input. For (AC coupled) connection of external U (B–Y) signal to on-chip analog switch. Signals on this pin cannot be inverted before output on pin U
VIN	31	analog chrominance input. For (AC coupled) connection of external V (R–Y) signal to on-chip analog switch. Signals on this pin cannot be inverted before output on pin V
P5, P4	32, 33	digital output port pins. These pins are programmable via the CDATA input
F	34	digital field rate timing signal. HIGH for odd-numbered fields. Changes state near the start of the video input line 1
L	35	digital line rate timing signal. HIGH for odd-numbered lines. Changes state near the start of every video input line
P3, P2, P1, P0	36-39	digital output port pins. These pins are programmable via the CDATA input
i.c.	40	internally connected. Connect to ground for normal operation
i.c.	41	internally connected. Connect to ground for normal operation
n.c.	42-44	not connected
V_{DDD}	45	+5 V supply to the digital parts of the chip
V_{SSD}	46	0 V digital ground
SWEEP	47	3-state digital output. A low frequency square wave can be output on this pin. Intended for assisting the clock/data recovery PLL to lock
V_{DDD}	48	+5 V supply to digital parts of chip
OSC	49	20.25 MHz oscillator output. Connection for external component network
XTAL	50	connection for 20.25 MHz crystal
V_{SSO}	51	0 V oscillator ground
V_{DDO}	52	+5 V supply for oscillator
V_{DDD}	53	+5 V supply to digital parts of chip
V_{SSD}	54	0 V digital ground
CLK	55	20.25 MHz clock. Waveform and amplitude chosen for EMC compatibility
V_{SSD}	56	0 V digital ground
DATA	57	digital binary output recovered from duo-binary D2DATA MAC data input; 10.125 Mbits/s.
CDATA	58	digital configuration data input/output. Open drain in output mode. Used by SAA1770 to control programmable features and provide video descrambler information (control words and frame-count). Also used to transmit bit error rate and AGC information from SAA1760 to SAA1770.
V_{SSD}	59	0 V digital ground
PC	60	3-state digital phase comparator output. When the chip set is locked to a MAC signal this pin is active only during data bursts on each line. Always active if chip set is out of lock.

SYMBOL	PIN	DESCRIPTION
n.c.	61	not connected
i.c.	62	internally connected. Connect to +5 V for normal operation
$\overline{CFL}$	63	digital combined field and line rate synchronizing signal from SAA1770
DGATE	64	digital MAC data burst gating signal from SAA1770. Used for data peak detector gating and phase-locked-loop gating. Active HIGH during data burst or when chip set is out of lock
KEYPULSE	65	active HIGH/LOW programmable line rate pulse output. Can be programmed to start or stop on any sample number. Intended for additional video clamping or as data burst marker for AFC gating
$\overline{CSYNC}$	66	digital negative-going composite sync. The line start time relative to the MAC YUV outputs is programmable for PAL/SECAM encoder/decoder delay compensation
$\overline{TSYNC}$	67	digital composite sync with reduced number of broad pulses and no equalizing pulses. Intended for use with teletext decoders capable of acquiring text on lines 2 to 5 and 315 to 317; i.e. lines normally containing broad or equalizing pulses
TLSAND	68	digital 3-state output. Used with external resistor network to obtain two-level sandcastle pulse for YUV/RGB matrix chips

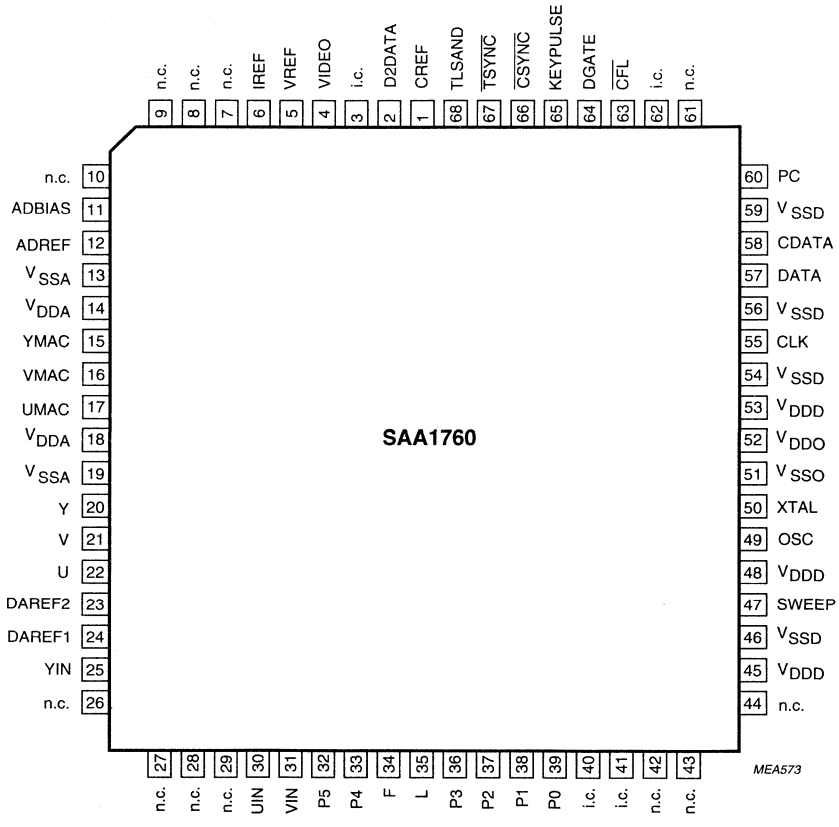


Fig.2 Pin configuration

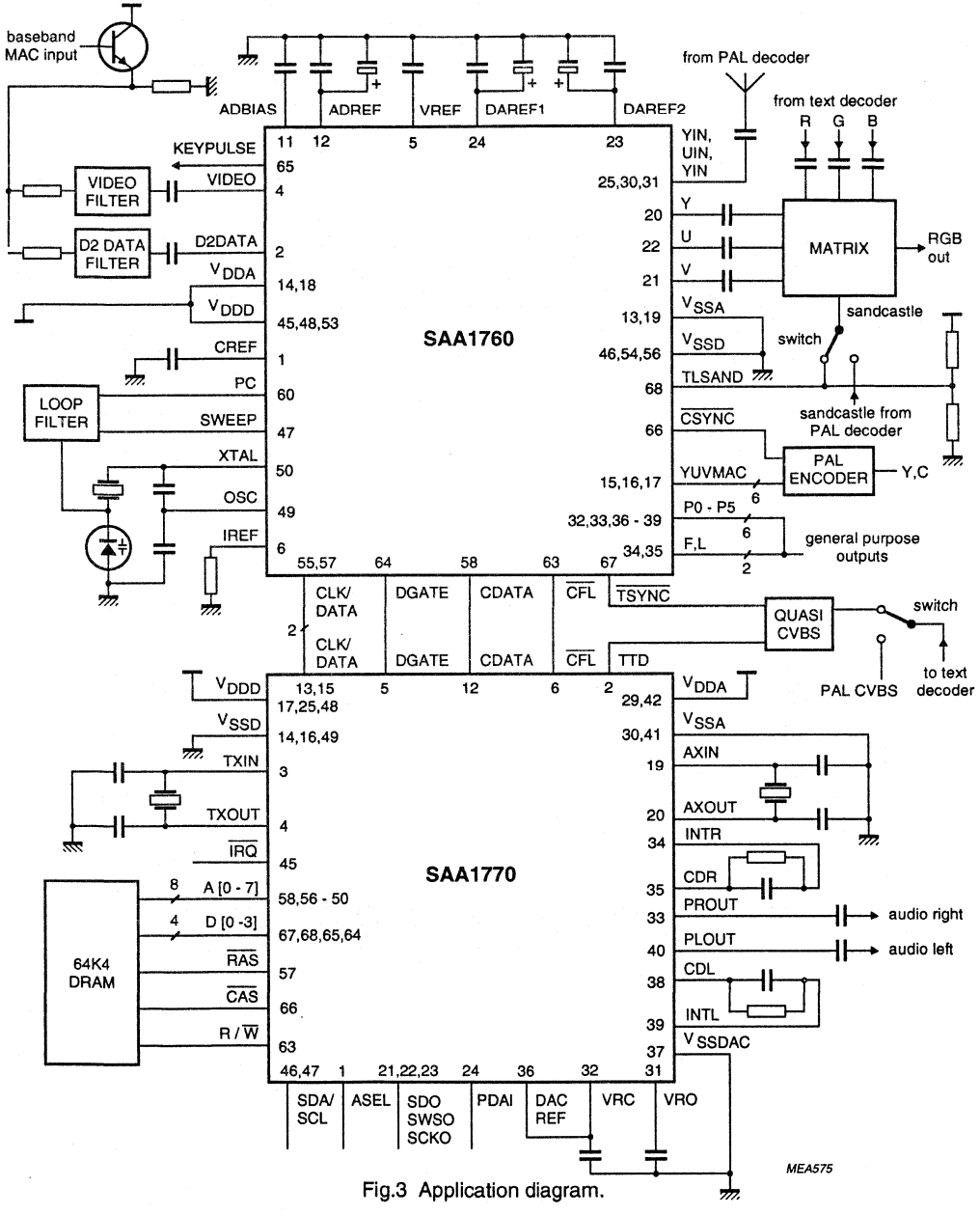


Fig.3 Application diagram.

D2MAC digital MAC packet SAA1770

FEATURES

- Spectrum descrambling and de-interleaving of one 99-bit wide sub-frame
- Full field capability, sub-frame can start anywhere on line 1
- VBI and packet teletext acquisition, frequency converted to output compatible with WST teletext decoders
- Processing of line 625 SDF and RDF with automatic pan vector extraction
- De-scrambling of packets. Four independent packet de-scramblers
- Golay decoding of packet headers and contents where required
- Two independent packet '0' data group acquisition "buffers" with automatic 3-way majority voting
- Four, 8-packet buffers for EMM acquisition
- Four, 16-packet buffers for general purpose (ECM, EMM, data) acquisition
- Three sound acquisition channels decoding any coding schemes in the EBU MAC/packet specification.
- Automatic sound configuration by B1 packets
- Two programmable digital sound mixers
- Primary analog sound output - one bit DACs and J17 de-emphasis on-chip. Also available in DAI format
- Secondary sound output in I²S-format
- Error concealment plus interpolation of sound samples
- Buffering of all received packets using a single external 64K4 DRAM
- I²C-bus control up to 400 kHz
- PLCC68 package

GENERAL DESCRIPTION

The SAA1770 is a D2MAC digital component acquisition and processing device which forms part of the Philips Semiconductors 2nd generation MAC decoder chip set. It accepts clock and data from a D2MAC source and performs all line 625 and sub-frame processing required for normal tv applications.

The SAA1770 synchronizes to the incoming data stream using the line sync words and provides timing for the chip set. It is programmed (configured) by an I²C-bus. The I²C-bus also used to program the SAA1760 via the CDATA output from the SAA1770.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5	5.5	V
I_{DD}	supply current	–	–	200	mA
f_{xtal}	oscillator frequency	20.248	20.25	20.252	MHz
f_{TXT}	teletext crystal frequency	–	6.3975	–	MHz
f_{SND}	sound crystal frequency	–	8.192	–	MHz
T_{amb}	operating ambient temperature	0	–	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA1770	68	PLCC	plastic	SOT188CG

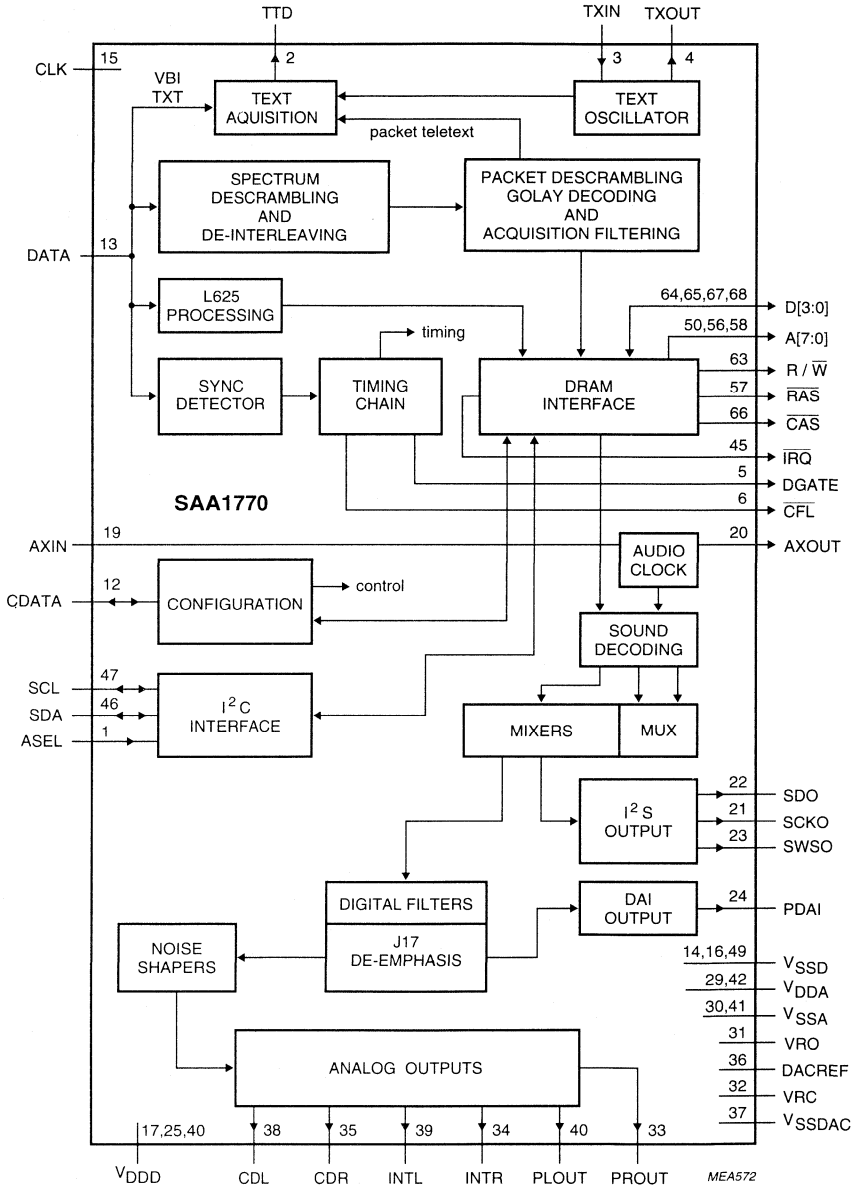


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
ASEL	1	digital input. I²C-bus address select. Selects one of two possible I²C-bus addresses
TTD	2	digital output. Teletext data output at 6.9375 Mb/s rate from VBI or packet teletext with clock run-in and framing code added
TXIN	3	connection for 6.9375 MHz teletext crystal
TXOUT	4	connection for 6.9375 MHz teletext crystal
DGATE	5	digital output. Data gate signal to SAA1760 marks data burst for PLL and data slicer gating etc.
$\overline{CFL}$	6	digital output. Composite field and line timing for synchronizing the SAA1760. Also synchronizes CDATA pin transfers
n.c.	7-11	not connected
CDATA	12	digital input/output. Configuration data to SAA1760 strobed by field timing events on the $\overline{CFL}$ signal. Also used to receive bit error rate information from SAA1760
DATA	13	digital input. Sliced and re-synchronized D2MAC data input from SAA1760 (10.125 Mb/s)
V_{SSD}	14	0 V digital ground
CLK	15	digital input. 20.25 MHz input clock from SAA1760
V_{SSD}	16	0 V digital ground
V_{DDD}	17	+5 V supply to digital parts of chip
i.c.	18	internally connected. Connect to ground for normal operation
AXIN	19	connection for 8.192 MHz sound crystal
AXOUT	20	connection for 8.192 MHz sound crystal
SCKO	21	digital output. Secondary sound output I²S-clock
SDO	22	digital output. Secondary sound output I²S-data
SWSO	23	digital output. Secondary sound output I²S-word select
PDAI	24	DAI output. Primary sound output in DAI format, J17 de-emphasized
V_{DDD}	25	+5 V supply to digital parts of chip
i.c.	26-28	internally connected. Connect to ground for normal operation
V_{DDA}	29	+ 5 V supply to analog parts of chip
V_{SSA}	30	0 V analog ground
VRO	31	voltage reference output for DACs
VRC	32	connection for DAC voltage reference decoupling capacitor
PROUT	33	analog output. Primary sound output right channel, J17 de-emphasized analog bit stream
INTR	34	connection to filter/integrator for right primary sound output
CDR	35	connection to external damping network for right sound output
DACREF	36	voltage reference input for DACs
V_{SSDAC}	37	ground for audio DACs
CDL	38	connection to external damping network for left sound output

SYMBOL	PIN	DESCRIPTION
INTL	39	connection to filter/integrator for left primary sound channel
PLOUT	40	analog output. Primary sound output left channel, J17 de-emphasized analog bit stream
V_{SSA}	41	0 V analogue ground
V_{DDA}	42	+5 V supply to analog parts of chip
n.c.	43	not connected
i.c.	44	internal connection. Connect to ground for normal operation
$\overline{IRQ}$	45	digital output. Open drain interrupt request. Active LOW signal indicating service request. Data available e.g. in packet buffers
SDA	46	digital input/output. I²C-400 kHz serial interface data. Slave receiver for controlling chip set and reading data
SCL	47	digital input/output. I²C-400 kHz serial interface clock. This pin is an output when SAA1760 "stretches" the clock
V_{DDD}	48	+5 V supply to digital parts of chip
V_{SSD}	49	0 V digital ground
A7	50	digital output. Address bus for external 64K4 DRAM
A4	51	digital output. Address bus for external 64K4 DRAM
A3	52	digital output. Address bus for external 64K4 DRAM
A5	53	digital output. Address bus for external 64K4 DRAM
A2	54	digital output. Address bus for external 64K4 DRAM
A6	55	digital output. Address bus for external 64K4 DRAM
A1	56	digital output. Address bus for external 64K4 DRAM
$\overline{RAS}$	57	digital output. Row address strobe for external 64K4 DDRAM
A0	58	digital output. Address bus for external 64K4 DRAM
n.c.	59-62	not connected
R/$\overline{W}$	63	digital output. Read/Write signal for external 64K4 DRAM
D2	64	digital input/output. Data bus for external 64K4 DRAM
D1	65	digital input/output. Data bus for external 64K4 DRAM
$\overline{CAS}$	66	digital output. Column address strobe for external 64K4 DRAM
D0	67	digital input/output. Data bus for external 64K4 DRAM
D3	68	digital input/output. Data bus for external 64K4 DRAM

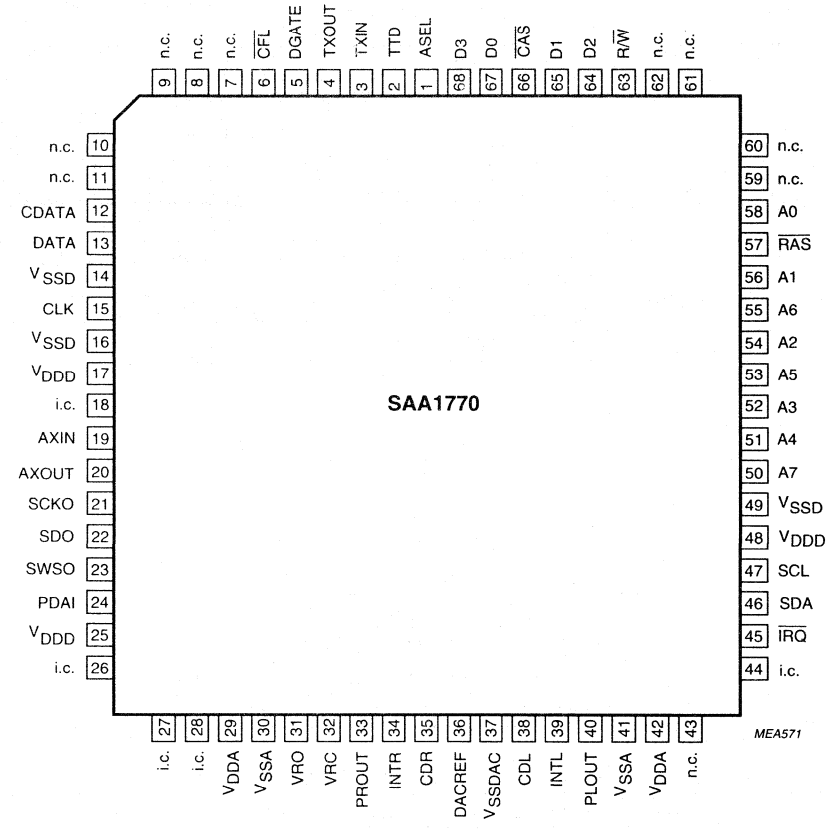


Fig.2 Pin configuration

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

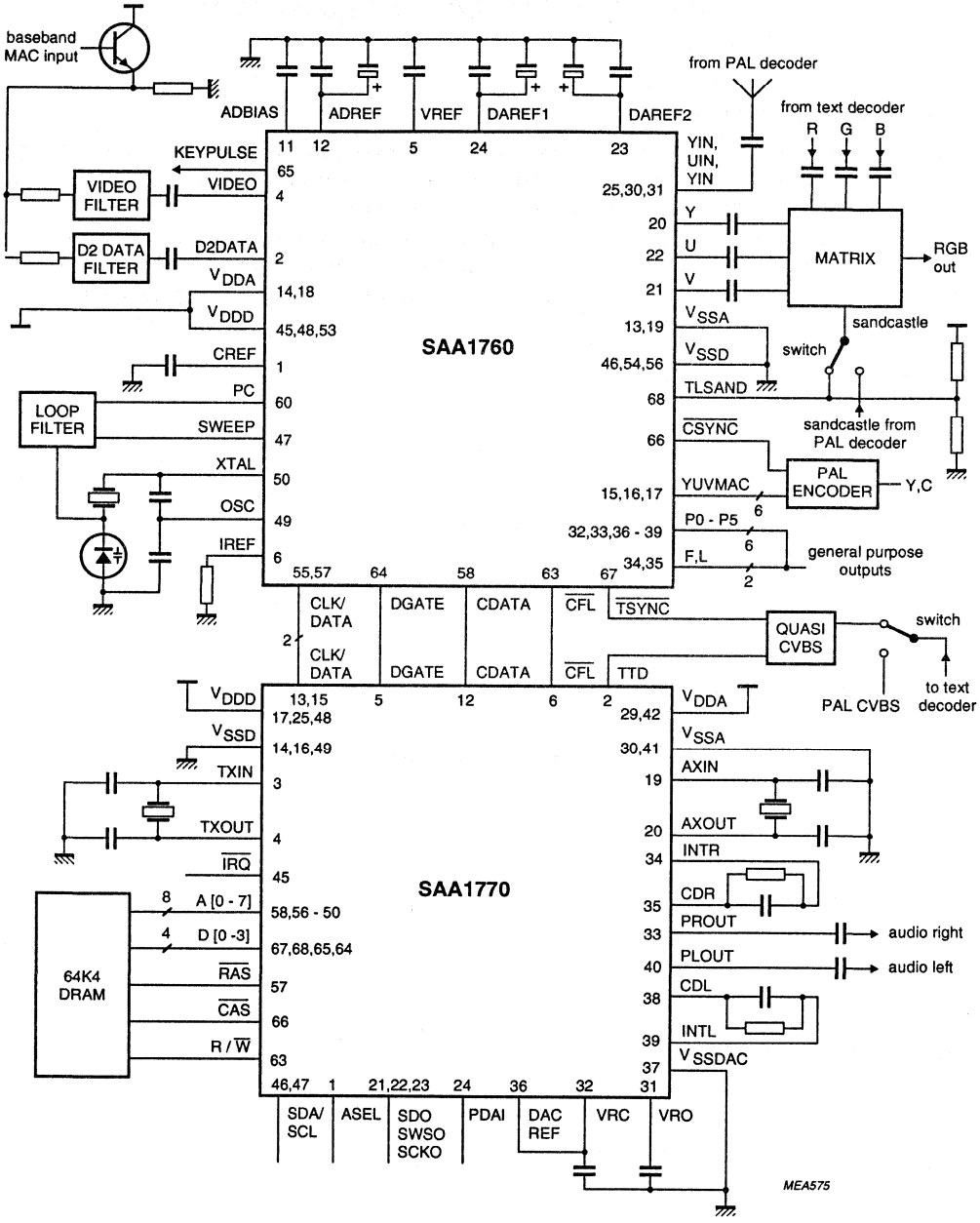


Fig.3 Application diagram.

REMOTE CONTROL TRANSMITTER

GENERAL DESCRIPTION

The SAA3004 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The SAA3004 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

The SAA3004 has the following features:

- Flashed or modulated transmission
- 7 sub-system addresses
- Up to 64 commands per sub-system address
- High-current remote output at V_{DD} = 6 V ($-I_{OH}$ = 40 mA)
- Low number of additional components
- Key release detection by toggle bits
- Very low stand-by current ($< 2\ \mu A$)
- Operational current < 2 mA at 6 V supply
- Wide supply voltage range (4 to 11 V)
- Ceramic resonator controlled frequency (typ. 450 kHz)
- Encapsulation: 20-lead plastic DIL or 20-lead plastic mini-pack (SO-20)

PACKAGE OUTLINES

SAA3004P: 20-lead DIL; plastic (SOT146).
SAA3004T: 20-lead mini-pack; plastic (SO20; SOT163A).

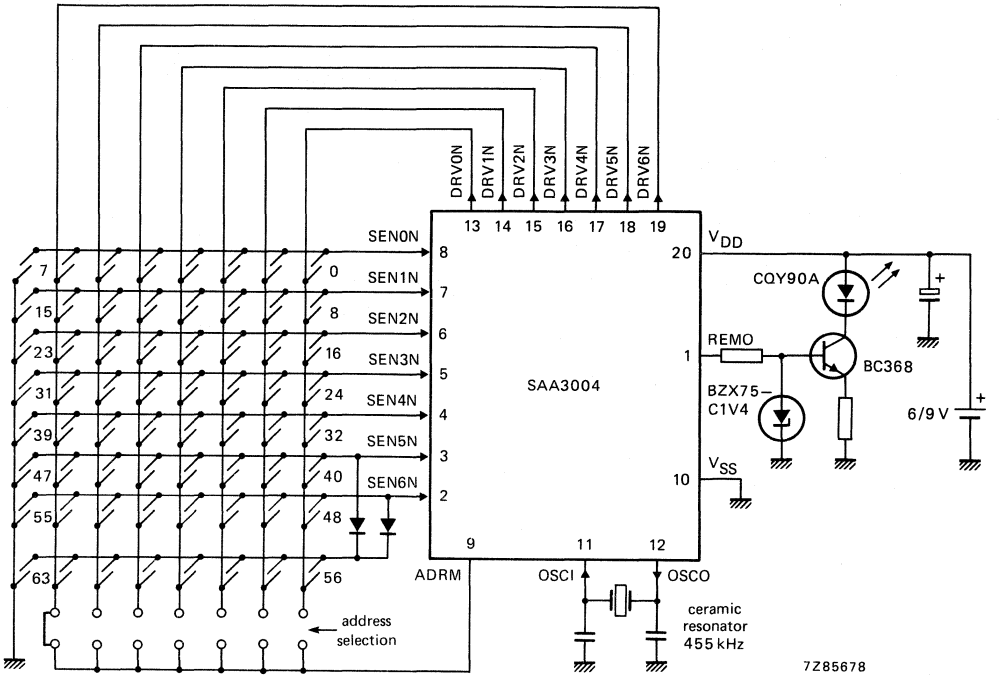


Fig. 1 Transmitter with SAA3004.

INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N)

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in Fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable.The sense inputs have P-channel pull-up transistors, so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

Address mode input (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode. This allows the definition of seven sub-system addresses as shown in Table 3. If driver DRV6N is connected to ADRM the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by presssing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnN with the highest number (n) defines the sub-system address, e.g. if driver DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in transmitters for more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4.

A change of the sub-system address will not start a transmission.

Remote control signal output (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in Tables 1 and 2.

The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see Fig. 3).

The format of the output data is given in Figs 2 and 3. In the flashed transmission mode the data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A, which are defined by the selected key.

In the modulated transmission mode the first toggle bit T1 is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence.

The toggle bits function as an indication for the decoder that the next instruction has to be considered as a new command.

The codes for the sub-system address and the selected key are given in Tables 3 and 4.

Oscillator input/output (OSCI and OSCO)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 400 kHz and 500 kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard operation

In the stand-by mode all drivers (DRV0N to DRV6N) are on. Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see Fig. 4) the output drivers (DRV0N to DRV6N) become active successively.

Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch. In contradiction to the command code the sub-system address is sensed only within the *first* scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.

In a multiple key-stroke sequence (see Fig. 5) the command code is always altered in accordance with the sensed key.

Multiple key-stroke protection

The keyboard is protected against multiple key-strokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see Fig. 5). In case of a multiple key-stroke the scan repetition rate is increased to detect the release of a key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix:

FUNCTIONAL DESCRIPTION (continued)

– The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored.
– SEN5N and SEN6N are not protected against multiple key-stroke on the same driver line, because this condition has been used for the definition of additional codes (code numbers 56 to 63).

Output sequence (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in Figs 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted words will always be completed after the key is released.

The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see Fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

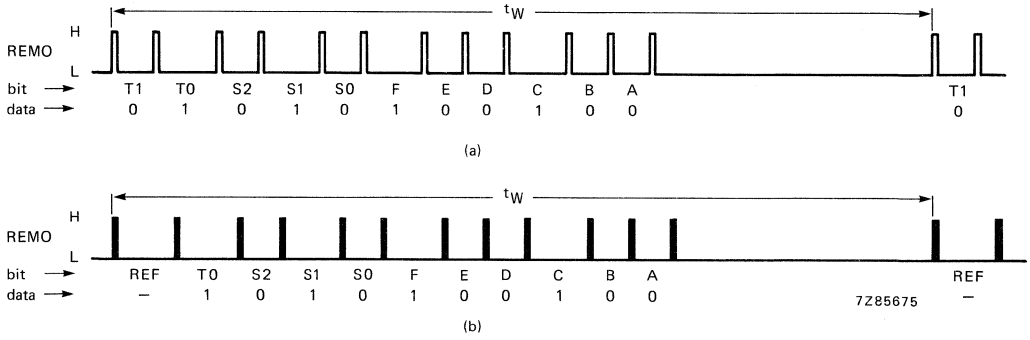
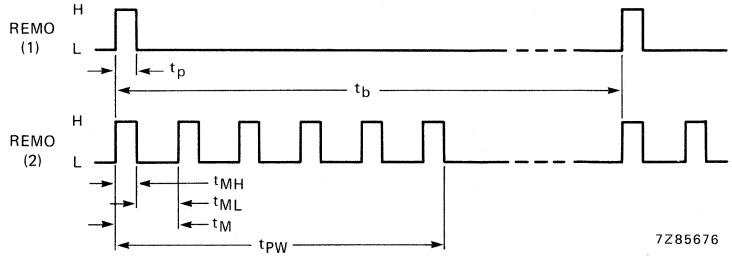


Fig. 2 Data format of REMO output; REF = reference time; T0 and T1 = toggle bits; S0, S1 and S2 = system address; A, B, C, D, E and F = command bits.
(a) flashed mode: transmission with 2 toggle bits and 3 address bits, followed by 6 command bits (pulses are flashed).
(b) modulated mode: transmission with reference time, 1 toggle bit and 3 address bits, followed by 6 command bits (pulses are modulated).



(1) Flashed pulse.
(2) Modulated pulse ($t_{PW} = (5 \times t_M) + t_{MH}$.

Fig. 3 REMO output waveform.

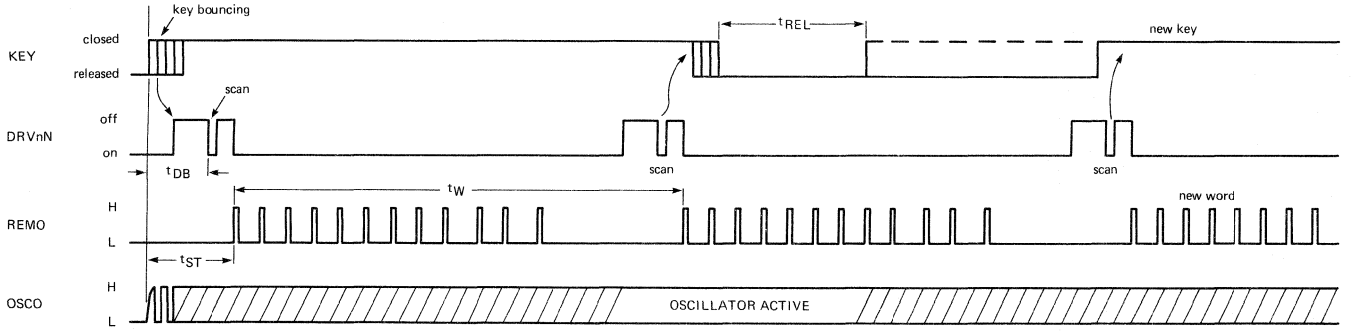


Fig. 4 Single key-stroke sequence.
Debounce time: $t_{DB} = 4$ to $9 \times T_o$.
Start time: $t_{ST} = 5$ to $10 \times T_o$.
Minimum release time: $t_{REL} = T_o$.
Word distance: t_W.

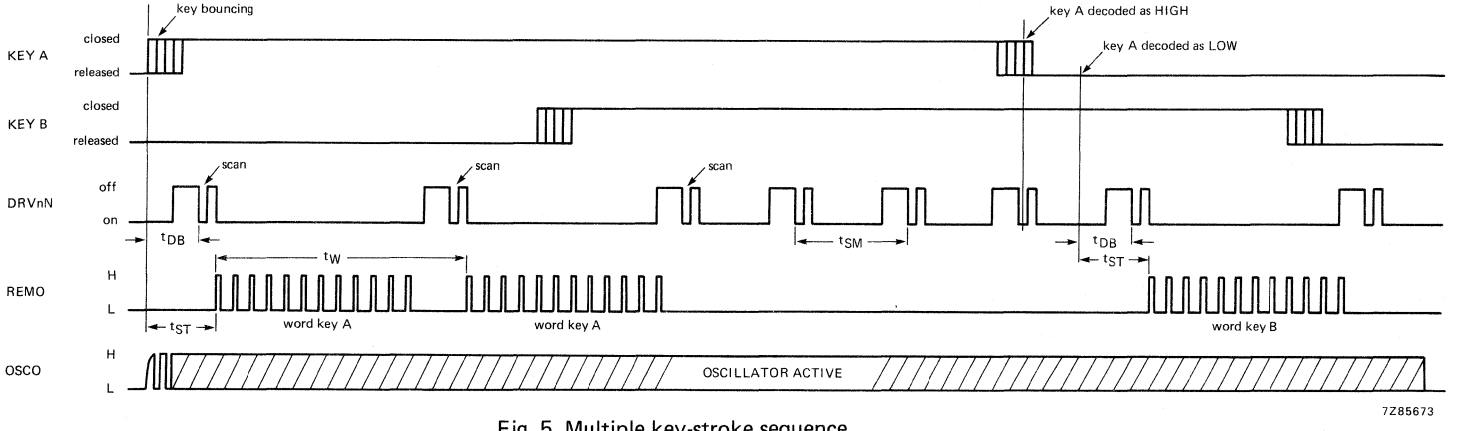


Fig. 5 Multiple key-stroke sequence.
Scan rate multiple key-stroke: $t_{SM} = 6$ to $10 \times T_o$.
For t_{DB}, t_{ST} and t_W see Fig. 4.

Table 1 Pulse train timing

mode	T_o ms	t_p μs	t_M μs	t_{ML} μs	t_{MH} μs	t_W ms
flashed	2,53	8,8	–	–	–	121
modulated	2,53	–	26,4	17,6	8,8	121

f_{osc}	455 kHz	$t_{osc} = 2{,}2\ \mu s$
t_p	$4 \times t_{osc}$	flashed pulse width
t_M	$12 \times t_{osc}$	modulation period
t_{ML}	$8 \times t_{osc}$	modulation period LOW
t_{MH}	$4 \times t_{osc}$	modulation period HIGH
T_o	$1152 \times t_{osc}$	basic unit of pulse distance
t_W	$55\,296 \times t_{osc}$	word distance

Table 2 Pulse train separation (t_b)

code	t_b
logic "0"	$2 \times T_o$
logic "1"	$3 \times T_o$
reference time	$3 \times T_o$
toggle bit time	$2 \times T_o$ or $3 \times T_o$

Table 3 Transmission mode and sub-system address selection

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode.

mode	sub-system address				driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
F	0	1	1	1							
L	1	0	0	0	o						
A	2	0	0	1	X	o					
S	3	0	1	0	X	X	o				
H	4	0	1	1	X	X	X	o			
E	5	1	0	0	X	X	X	X	o		
D	6	1	0	1	X	X	X	X	X	o	
M											
O	0	1	1	1							o
D	1	0	0	0	o						o
U	2	0	0	1	X	o					o
L	3	0	1	0	X	X	o				o
A	4	0	1	1	X	X	X	o			o
T	5	1	0	0	X	X	X	X	o		o
E	6	1	0	1	X	X	X	X	X	o	o
D											

o = connected to ADRM
blank = not connected to ADRM
X = don't care

Table 4 Key codes

matrix drive	matrix sense	code F	E	D	C	B	A	matrix position
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V_{SS}	SEN0N	0	0	0	1	1	1	7
*	SEN1N	0	0	1		**		8 to 15
*	SEN2N	0	1	0		**		16 to 23
*	SEN3N	0	1	1		**		24 to 31
*	SEN4N	1	0	0		**		32 to 39
*	SEN5N	1	0	1		**		40 to 47
*	SEN6N	1	1	0		**		48 to 55
*	SEN5N and SEN6N	1	1	1		**		56 to 63

* The complete matrix drive as shown above for SEN0N is also applicable for the matrix sense inputs SEN1N to SEN6N and the combined SEN5N/SEN6N.

** The C, B and A codes are identical to SEN0N as given above.

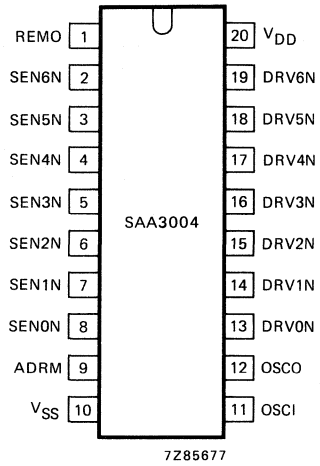


Fig. 6 Pinning diagram.

PINNING

1	REMO	remote data output
2	SEN6N	key matrix sense inputs
3	SEN5N	
4	SEN4N	
5	SEN3N	
6	SEN2N	
7	SEN1N	
8	SEN0N	
9	ADRM	address mode control input
10	V_{SS}	ground
11	OSCI	oscillator input
12	OSCO	oscillator output
13	DRV0N	key matrix drive outputs
14	DRV1N	
15	DRV2N	
16	DRV3N	
17	DRV4N	
18	DRV5N	
19	DRV6N	
20	V_{DD}	positive supply

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to +15		V
Input voltage range	V_I	−0,5 to V_{DD} +0,5		V
Output voltage range	V_O	−0,5 to V_{DD} +0,5		V
D.C. current into any input or output	±I	max.	10	mA
Peak REMO output current during 10 μs; duty factor = 1%	$-I_{(REMO)M}$	max.	300	mA
Power dissipation per package for T_{amb} = −20 to +70 °C	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}	−55 to +150		°C
Operating ambient temperature range	T_{amb}	−20 to +70		°C

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage T_{amb} = 0 to +70 °C	–	V_{DD}	4	–	11	V
Supply current; active f_{osc} = 455 kHz; REMO output unloaded	6 9	I_{DD} I_{DD}	– –	1 3	– –	mA mA
Supply current; inactive (stand-by mode) T_{amb} = 25 °C	6 9	I_{DD} I_{DD}	– –	– –	2 2	μA μA
Oscillator frequency (ceramic resonator)	4 to 11	f_{osc}	400	–	500	kHz
Keyboard matrix						
Inputs SEN0N to SEN6N						
Input voltage LOW	4 to 11	V_{IL}	–	–	0,2 x V_{DD}	V
Input voltage HIGH	4 to 11	V_{IH}	0,8 x V_{DD}	–	–	V
Input current V_I = 0 V	4 11	$-I_I$ $-I_I$	10 30	– –	100 300	μA μA
Input leakage current V_I = V_{DD}	11	I_I	–	–	1	μA
Outputs DRV0N to DRV6N						
Output voltage "ON" I_O = 0,1 mA I_O = 1,0 mA	4 11	V_{OL} V_{OL}	– –	– –	0,3 0,5	V V
Output current "OFF" V_O = 11 V	11	I_O	–	–	10	μA
Control input ADRM						
Input voltage LOW	–	V_{IL}	–	–	0,8 x V_{DD}	V
Input voltage HIGH	–	V_{IH}	0,2 x V_{DD}	–	–	V
Input current (switched P- and N-channel pull-up/ pull-down)						
Pull-up active stand-by voltage: 0 V	4 11	I_{IL} I_{IL}	10 30	– –	100 300	μA μA
Pull-down active stand-by voltage: V_{DD}	4 11	I_{IH} I_{IH}	10 30	– –	100 300	μA μA

CHARACTERISTICS (continued)

V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Data output REMO						
Output voltage HIGH	6	V_{OH}	3	–	–	V
$-I_{OH}$ = 40 mA	9	V_{OH}	6	–	–	V
Output voltage LOW	6	V_{OL}	–	–	0,2	V
I_{OL} = 0,3 mA	9	V_{OL}	–	–	0,1	V
Oscillator						
Input current OSCI at V_{DD}	6	I_I	0,8	–	2,7	μA
Output voltage HIGH $-I_{OL}$ = 0,1 mA	6	V_{OH}	–	–	V_{DD}–0,6	V
Output voltage LOW I_{OH} = 0,1 mA	6	V_{OL}	–	–	0,6	V

INFRARED REMOTE CONTROL TRANSMITTER (RECS 80 LOW VOLTAGE)

GENERAL DESCRIPTION

The SAA3008 transmitter IC is designed for infrared remote control systems. It has a capacity for 1280 commands arranged in 20 sub-system address groups of 64 commands each. The subsystem address may be selected by press-button, slider switches or be hard-wired.

Commands are transmitted in patterns which are pulse distance coded. Modulated pulse transmissions allow a narrow-band receiver to be used for improved noise rejection. The modulation frequency of the SAA3008 is 38 kHz which is 1/12 of the oscillator frequency of 455 kHz (typical).

Features

- Modulated transmission
- Ceramic resonator controlled frequency
- Data-word-start with reference time of unique start pattern
- Supply voltage range 2 V to 6.5 V
- 40 mA output current capability
- Very low standby current ($< 4\ \mu A$ at $V_{DD} = 6$ V)
- Up to 20 subsystem address groups
- Up to 64 commands per subsystem address

  } up to 1280 commands
- Requires few additional components

PACKAGE OUTLINES

SAA3008P: 20-lead DIL; plastic (SOT146).
SAA3008T: 20-lead mini-pack; plastic (SO20; SOT163A).

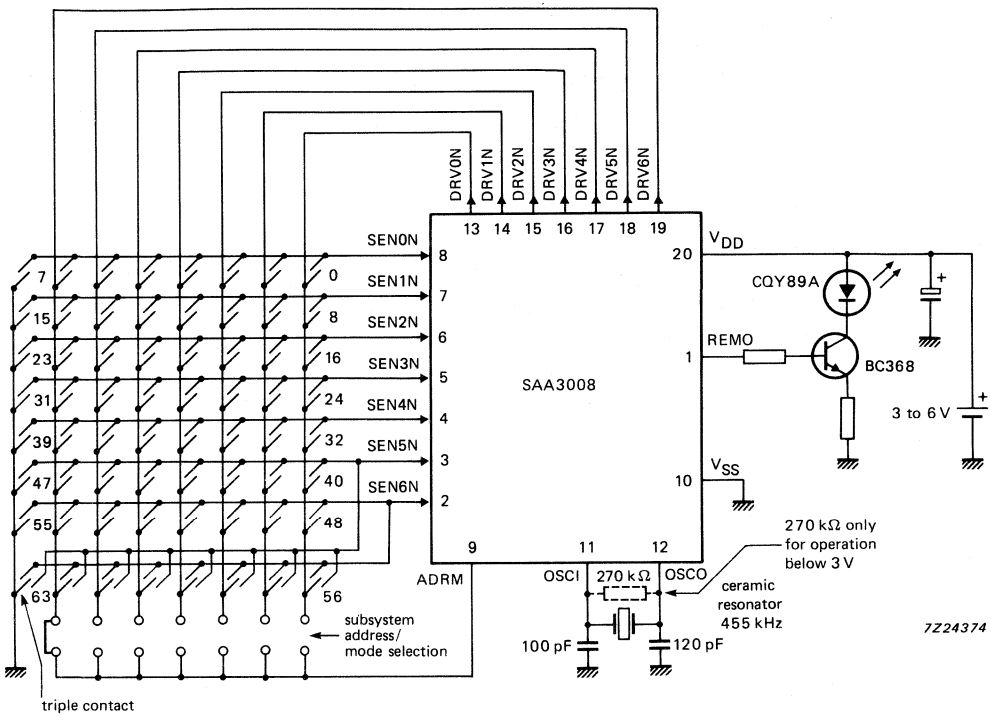


Fig.1 SAA3008 application example.

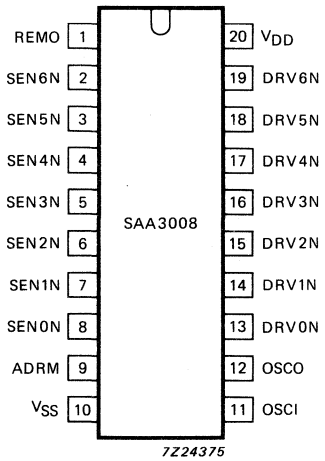


Fig.2 Pinning diagram.

PINNING

1	REMO	remote data output
2	SEN6N	sense inputs from key matrix
3	SEN5N	
4	SEN4N	
5	SEN3N	
6	SEN2N	
7	SEN1N	
8	SEN0N	
9	ADRM	address/mode control input
10	V_{SS}	ground (0 V)
11	OSCI	oscillator input
12	OSCO	oscillator output
13	DRV0N	drive outputs to key matrix
14	DRV1N	
15	DRV2N	
16	DRV3N	
17	DRV4N	
18	DRV5N	
19	DRV6N	
20	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Key matrix (DRV0N - DRV6N and SEN0N - SEN6N)

The transmitter keyboard is arranged as a scanned matrix with seven driver outputs (DRV0N to DRV6N) and seven sensing inputs (SEN0N to SEN6N) as shown in Fig.1. The driver outputs are open-drain n-channel transistors which are conductive in the stand-by mode. The sensing inputs enable the generation of 56 command codes. With two external diodes connected (or triple contact), as in Fig.1, all 64 commands are addressable. The sense lines have p-channel pull-up transistors, so that they are HIGH until pulled LOW by connecting them to an output via a key depression to initiate a code transmission.
The maximum allowable value of contact series resistance for keyboard switches in the ON-state is 7 kΩ.

Address/mode input (ADRM)

Subsystem addresses are defined by connecting one or two of the key matrix driver lines (DRV0N to DRV6N) to the ADRM input. This allows up to 20 subsystem addresses to be generated for the REMO output (bits S3, S2, S1 and S0) as shown in Table 1 and Fig.3.

The transmission mode is defined by the DRV6N to ADRM connection as follows:

- Mode 1 DRV6N not connected to ADRM
- Mode 2 DRV6N connected to ADRM

In Mode 1 the reference time REF equals 3To, this may be used as a reference time for the decoding sequence. In Mode 2 an additional modulated pulse has been inserted into the middle of the reference time, therefore, these pulses are now separated by 1.5To. This unique start pattern START uses the detection of a beginning word (see Fig.3).
When more than one connection is made to ADRM then all connections should be decoupled using diodes.

The ADRM input has switched pull-up and pull-down loads. In the standby mode only pull-down load is active and ADRM input is held LOW (this condition is independent of the ADRM circuit configuration and minimizes power loss in the standby mode). When a key is pressed the transmitter becomes active (pull-down is switched OFF, pull-up is switched ON) and the driver line signals are sensed for the subsystem address coding.

The subsystem address is sensed only within the first scan cycle, whereas the command code is sensed in every scan. The transmitted subsystem address remains unchanged if the subsystem address selection is changed while the command key is pressed. A change of the subsystem address does not start a transmission.

In a multiple keystroke sequence (Fig.6) the second word B might be transmitted with subsystem address 18 or 19 instead of the preselected subsystem address (Table 1). This is only relevant for systems decoding subsystem address 18 or 19.

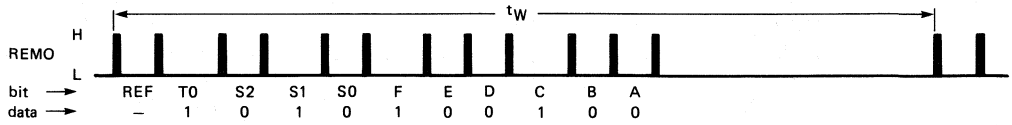
Remote control signal output (REMO)

The REMO output driver stage incorporates a bipolar emitter-follower which allows a high output current in the output active (HIGH) state (Fig.7).
The information is defined by the distance 't_b' between the leading edges of the modulated pulses (Fig.4). The distance t_b is a multiple of the basic unit T_o (Table 3) which equals 1152 periods of the oscillator frequency f_{osc} (Table 3). The pulses are modulated with 6 periods of 1/12 of the oscillator frequency (38 kHz).
The format of the output data is illustrated in Figs 3 and 4.
A data word starts with the reference time and toggle bit T0 and is followed by the definition bits for the subsystem address S3, S2, S1 and S0 (bit S3 is transmitted only for subsystem addresses 8 to 20).
The selected command key is defined by bits F, E, D, C, B and A as shown in Table 2.

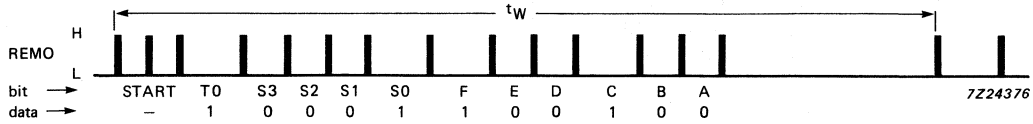
DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

The toggle bit T0 acts as an indication for the decoder whether the next instruction should be considered as a new command or not. The codes for the subsystem address and the selected key are given in Table 3.



(a) Transmission with reference time and subsystem addresses 1 to 7.



(b) Transmission with start-pattern and subsystem addresses 8 to 20.

Where:

Reference time	
start pattern	T0 toggle bit
S3, S2, S1, S0	subsystem address
A to F	command bits
t_W	word length
binary values	determined by pulse spacing

Fig.3 Data format of remote control signal (REMO).

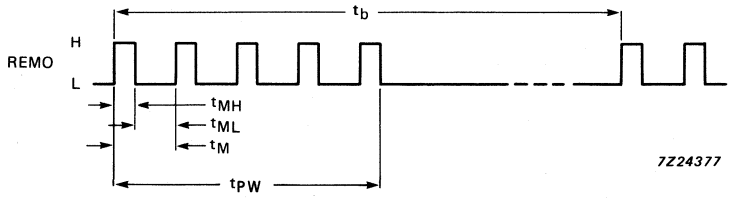


Fig.4 Waveform for one pulse period at REMO output; for timing values see Table 3.

Oscillator (OSCI, OSCO)

The external components for the oscillator circuit are connected to OSCI and OSCO. The oscillator operates with a ceramic resonator in the frequency range 350 kHz to 500 kHz, as defined by the resonator. When operating at a supply voltage of below 3 V a 270 kHz resistor should be connected in parallel with the resonator.

DEVELOPMENT DATA

Table 1 Definition of subsystem addresses

address number	driver line(s) connected to ADRM	subsystem address S3	S2	S1	S0
1	no connection	–	1	1	1
2	DRV0N	–	0	0	0
3	DRV1N	–	0	0	1
4	DRV2N	–	0	1	0
5	DRV3N	–	0	1	1
6	DRV4N	–	1	0	0
7	DRV5N	–	1	0	1
8	DRV0N and DRV2N	0	0	0	0
9	DRV0N and DRV3N	1	0	0	0
10	DRV0N and DRV4N	0	1	0	0
11	DRV0N and DRV5N	1	1	0	0
12	DRV1N and DRV2N	0	0	0	1
13	DRV1N and DRV3N	1	0	0	1
14	DRV1N and DRV4N	0	1	0	1
15	DRV1N and DRV5N	1	1	0	1
16	DRV2N and DRV3N	1	0	1	0
17	DRV2N and DRV4N	0	1	1	0
18	DRV2N and DRV5N	1	1	1	0
19	DRV3N and DRV4N	0	1	1	1
20	DRV3N and DRV5N	1	1	1	1

Table 2 Definition of command codes

key pressed	drive-to-sense connection made	command code generated F	EE	D	C	B	A
0	DRV0N to SEN0N	0	0	0	0	0	0
1	DRV1N to SEN0N	0	0	0	0	0	1
2	DRV2N to SEN0N	0	0	0	0	1	0
3	DRV3N to SEN0N	0	0	0	0	1	1
4	DRV4N to SEN0N	0	0	0	1	0	0
5	DRV5N to SEN0N	0	0	0	1	0	1
6	DRV6N to SEN0N	0	0	0	1	1	0
7	DRV7N to SEN0N	0	0	0	1	1	1
8	DRV0N to SEN1N	0	0	1	0	0	0
9	DRV1N to SEN1N	0	0	1	0	0	1
10	DRV2N to SEN1N	0	0	1	0	1	0
11	DRV3N to SEN1N	0	0	1	0	1	1
12	DRV4N to SEN1N	0	0	1	1	0	0
13	DRV5N to SEN1N	0	0	1	1	0	1
14	DRV6N to SEN1N	0	0	1	1	1	0
15	DRV7N to SEN1N	0	0	1	1	1	1
16	DRV0N to SEN2N	0	1	0	0	0	0
17	DRV1N to SEN2N	0	1	0	0	0	1
18	DRV2N to SEN2N	0	1	0	0	1	0
19	DRV3N to SEN2N	0	1	0	0	1	1
20	DRV4N to SEN2N	0	1	0	1	0	0

Table 2 Definition of command codes (continued)

key pressed	drive-to-sense connection made	command code generated F	E	D	C	B	A
21	DRV5N to SEN2N	0	1	0	1	0	1
22	DRV6N to SEN2N	0	1	0	1	1	0
23	DRV7N to SEN2N	0	1	0	1	1	1
24	DRV0N to SEN3N	0	1	1	0	0	0
25	DRV1N to SEN3N	0	1	1	0	0	1
26	DRV2N to SEN3N	0	1	1	0	1	0
27	DRV3N to SEN3N	0	1	1	0	1	1
28	DRV4N to SEN3N	0	1	1	1	0	0
29	DRV5N to SEN3N	0	1	1	1	0	1
30	DRV6N to SEN3N	0	1	1	1	1	0
31	DRV7N to SEN3N	0	1	1	1	1	1
32	DRV0N to SEN4N	1	0	0	0	0	0
33	DRV1N to SEN4N	1	0	0	0	0	1
34	DRV2N to SEN4N	1	0	0	0	1	0
35	DRV3N to SEN4N	1	0	0	0	1	1
36	DRV4N to SEN4N	1	0	0	1	0	0
37	DRV5N to SEN4N	1	0	0	1	0	1
38	DRV6N to SEN4N	1	0	0	1	1	0
39	DRV7N to SEN4N	1	0	0	1	1	1
40	DRV0N to SEN5N	1	0	1	0	0	0
41	DRV1N to SEN5N	1	0	1	0	0	1
42	DRV2N to SEN5N	1	0	1	0	1	0
43	DRV3N to SEN5N	1	0	1	0	1	1
44	DRV4N to SEN5N	1	0	1	1	0	0
45	DRV5N to SEN5N	1	0	1	1	0	1
46	DRV6N to SEN5N	1	0	1	1	1	0
47	DRV7N to SEN5N	1	0	1	1	1	1
48	DRV0N to SEN6N	1	1	0	0	0	0
49	DRV1N to SEN6N	1	1	0	0	0	1
50	DRV2N to SEN6N	1	1	0	0	1	0
51	DRV3N to SEN6N	1	1	0	0	1	1
52	DRV4N to SEN6N	1	1	0	1	0	0
53	DRV5N to SEN6N	1	1	0	1	0	1
54	DRV6N to SEN6N	1	1	0	1	1	0
55	DRV7N to SEN6N	1	1	0	1	1	1
56	DRV0N to SEN5N and SEN6N	1	1	1	0	0	0
57	DRV1N to SEN5N and SEN6N	1	1	1	0	0	1
58	DRV2N to SEN5N and SEN6N	1	1	1	0	1	0
59	DRV3N to SEN5N and SEN6N	1	1	1	0	1	1
60	DRV4N to SEN5N and SEN6N	1	1	1	1	0	0
61	DRV5N to SEN5N and SEN6N	1	1	1	1	0	1
62	DRV6N to SEN5N and SEN6N	1	1	1	1	1	0
63	DRV7N to SEN5N and SEN6N	1	1	1	1	1	1

Table 3 Pulse timing

parameter	symbol	duration	duration at f_{osc} = 455 kHz; t_{osc} = 2.2 μs
Modulation period	t_M	$12t_{osc}$	26.4 μs
Modulation LOW time	t_{ML}	$8t_{osc}$	17.6 μs
Modulation HIGH time	t_{MH}	$4t_{osc}$	8.8 μs
Modulation pulse width	t_{PW}	$5t_M + t_{MH}$	140.8 μs
Basic unit of pulse spacing	t_o	$1152t_{osc}$	2.53 ms
Word length for subsystem addresses			
0 to 7	t_W	$55296t_{osc}$	121.44 ms
8 to 20	t_W	$59904t_{osc}$	132.56 ms
Pulse separation for			
logic 0	t_b	$2t_o$	5.06 ms
logic 1	t_b	$3t_o$	7.59 ms
reference time	t_b	$3t_o$	7.59 ms
toggle bit	t_b	$2t_o$	5.06 ms
		$3t_o$	7.59 ms
Start pattern	t_b	$2 \times 1.5t_o$	2 x 3.79 ms

DEVELOPMENT DATA

OPERATION

Keyboard

In the standby mode all drivers DRV0N-DRV6N are ON but are non-conducting due to their open drain configuration. When a key is pressed, a completed drain connection pulls down one or more of the sense lines to ground. Referring to Fig.5, the power-up sequence for the IC commences as a key is pressed. The oscillator becomes active and then, following the debounce time (t_{DB}), the output drivers become active successively.

Within the first scan cycle the transmission mode, subsystem address and the selected command code are sensed and loaded into an internal data latch. In a multiple keystroke sequence (Fig.6) the command code is always altered according to the sensed key.

Multiple keystroke protection

The keyborad is protected against multiple keystrokes. If more than one key is pressed the circuit will not generate a new REMO sequence (Fig.6).
In a multiple keystroke sequence the scan repetition rate is increased to detect the release of the key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix:

- The keys switching directly to ground (codes 7, 15, 23, 31, 39, 47, 55, 63) are not completely covered by multiple keystroke protection. If one sense input is switched to ground, other keys on that sense line are ignored.
- The sense lines SEN5N and SEN6N are not protected against multiple keystrokes on the same driver line because this has been used to define codes 56 to 63.

OPERATION (continued)

Output sequence

The output operation starts when the code of the selected key has been loaded into the internal command register. A burst of pulses, including the latched address and command codes, is generated at the output REMO for as long as the key is pressed. The format of the output pulse train is as shown in Figs 3 and 4. The operation is terminated by releasing the key, or by pressing more than one key at the same time. Once a sequence has been started, the transmitted words will always be completed after the key has been released.

The toggle bit T0 is incremented if the key is released for a minimum time t_{REL} (Fig.5). In a multiple keystroke sequence the toggle bit remains unchanged.

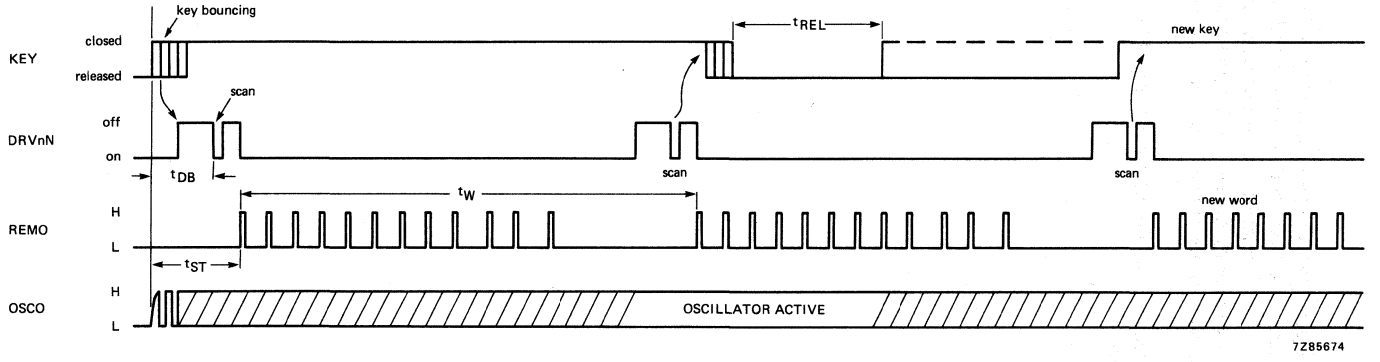


Fig.5 Single keystroke sequence; t_{DB} = debounce time = $4T_O$ to $9T_O$; t_{ST} = start time = $5T_O$ to $10T_O$; t_{REL} = minimum release time = T_O; t_W = word length.

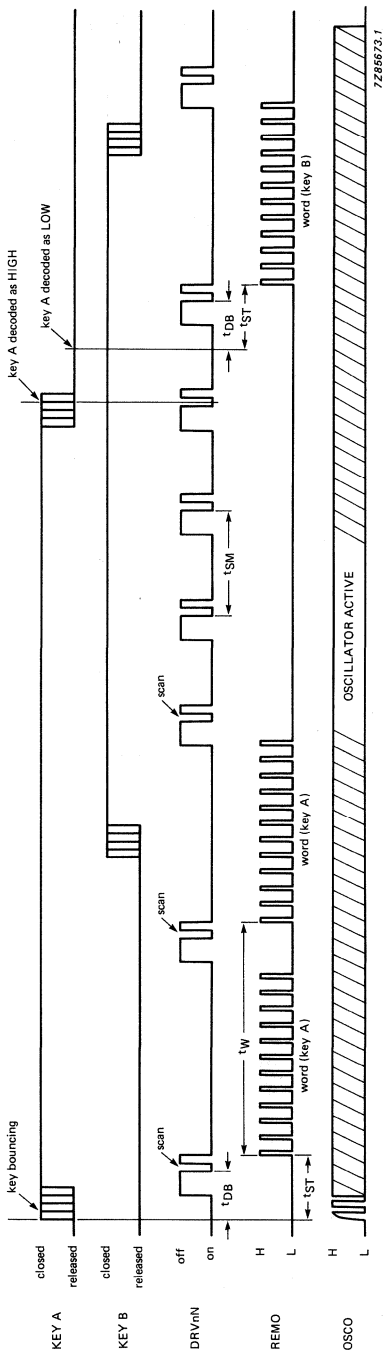


Fig.6 Scan rate multiple keystroke sequence: t_{SM} = scan rate (multiple keystroke) = $6T_O$ to $10T_O$; t_{DB}, t_{ST}, and t_W are as per Fig.5.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0.3	+7	V
Input voltage range		V_I	−0.3	V_{DD} + 0.3	V
Output voltage range		V_O	−0.3	V_{DD} + 0.3	V
Total power dissipation					
DIL package (SOT146)		P_{tot}	–	300	mW
mini-pack (SO20; SOT163A)		P_{tot}	–	200	mW
Power dissipation					
matrix outputs DRV0N to DRV6N		P_O	–	50	mW
remote data output REMO		P_O	–	200	mW
Operating ambient temperature range		T_{amb}	−20	+70	°C
Storage temperature range		T_{stg}	−20	+125	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 0 to +70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	2.0	–	6.5	V
Supply current active	f_{osc} = 455 kHz;					
	V_{DD} = 3 V	I_{DD}	–	0.25	–	mA
	V_{DD} = 4.5 V	I_{DD}	–	0.5	–	mA
	V_{DD} = 6 V	I_{DD}	–	1	–	mA
Standby mode	T_{amb} = 25 °C;					
	V_{DD} = 6 V	I_{DD}	–	–	4	μA
Oscillator frequency (ceramic resonator)	V_{DD} = 2 to 6.5 V	f_{osc}	350	–	500	kHz
Inputs SEN0N to SEN6N						
Input voltage LOW	V_{DD} = 2 to 6.5 V	V_{IL}	–	–	0.3 V_{DD}	V
Input voltage HIGH	V_{DD} = 2 to 6.5 V	V_{IH}	0.7 V_{DD}	–	–	V
Input current (p-channel pull-up)	V_{IL} = 0 V					
	V_{DD} = 2 V	I_I	−10	–	−100	μA
	V_{DD} = 6.5 V	I_I	−100	–	−600	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Outputs DRV0N to DRV6N (open drain 1)						
Output voltage ON	I_O = 0.25 mA; V_{DD} = 2 V	V_{OL}	–	–	0.3	V
	I_O = 2.5 mA; V_{DD} = 6.5 V	V_{OL}	–	–	0.6	V
Output current OFF	V_{DD} = 6.5 V	I_O	–	–	10	μA
Input ADRM						
Input voltage LOW		V_{IL}	–	–	0.4 V_{DD}	V
Input voltage HIGH		V_{IH}	0.85 V_{DD}	–	–	V
Input current (switched p and n channel pull-up and pull-down)						
pull-up active	V_I = 0 V					
	V_{DD} = 2 V	I_{IL}	−10	–	−100	μA
	V_{DD} = 6.5 V	I_{IL}	−100	–	−600	μA
pull-down active	V_I = V_{DD}					
	V_{DD} = 2 V	I_{IH}	10	–	100	μA
	V_{DD} = 6.5 V	I_{IH}	100	–	600	μA
Output REMO						
Output voltage HIGH	I_{OH} = −40 mA; T_{amb} = 25 °C					
	V_{DD} = 2 V	V_{OH}	0.8	–	–	V
	V_{DD} = 6.5 V	V_{OH}	5.0	–	–	V
	I_{OH} = 0.5 mA; V_{DD} = 2 V	V_{OH}	0.8 V_{DD}	–	–	V
Output voltage LOW	I_{OL} = 0.5 mA; V_{DD} = 2 V	V_{OL}	–	–	0.4	V
	I_{OL} = 2.0 mA; V_{DD} = 6.5 V	V_{OL}	–	–	0.4	V
Input OSCI						
Input current HIGH	V_{DD} = 6.5 V	I_{IH}	3.0	–	7.0	μA
Output OSCO						
Output voltage HIGH	I_{OH} = 100 μA; V_{DD} = 6.5 V	V_{OH}	V_{DD}−0.8	–	–	V
Output voltage LOW	I_{OL} = 100 μA; V_{DD} = 6.5 V	V_{OL}	–	–	0.7	V

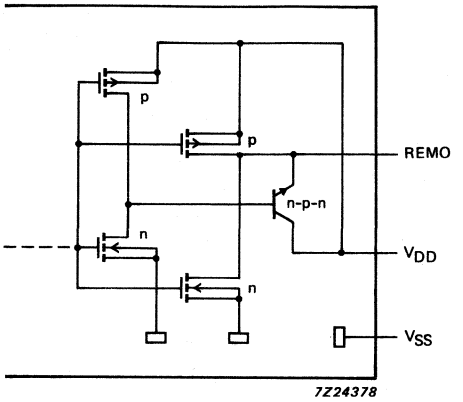


Fig.7 REMO output stage.

DEVELOPMENT DATA

INFRARED REMOTE CONTROL DECODERS

GENERAL DESCRIPTION

The main function of the SAA3009 and SAA3049 ICs is to check and convert the received coded data (RECS80/RC5) into latched binary outputs. The device address can be hard-wired for a particular address allowing several devices in one location. Alternatively, received data with any address can be accepted, the received data and address are then outputs.

Features

- Decodes 64 remote control commands with a maximum of 32 subaddresses
- Accepts RECS80 codes with pulse position modulation (SAA3004, SAA3007, SAA3008) or RC5 codes with biphase transmission (SAA3006, SAA3010)
- Available at SAA3009 with 8 high current (10 mA) open-drain outputs and internal pull-ups for direct LED drive via resistors or as SAA3049 for low supply current applications
- Adding circuitry for binary decoding allows a maximum of 2048 commands to be used, for example 1-of-16 decoder (HEF4515)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
SAA3009	note 1	V_{CC}	4.5	5.0	5.5	V
SAA3049	note 2	V_{CC}	2.5	–	5.5	V
Supply current						
SAA3009	note 1	I_{CC}	–	–	70	mA
SAA3049	note 2	I_{CC}	–	1.0	2.0	mA
Oscillator frequency		f_{osc}	–	4	–	MHz
Output sink current LOW (pins 1 to 8)						
SAA3009	note 3	I_{OL}	–	–	10	mA
SAA3049	note 4	I_{OL}	1.6	3.0	–	mA

Notes to the QUICK REFERENCE DATA

1. T_{amb} = 0 to + 70 °C.
2. T_{amb} = −40 to + 85 °C.
3. Open-drain with 20 to 50 kΩ internal pull-up resistor.
4. Open-drain without internal pull-up resistor at V_{CC} = 5 V ± 10%; V_O = 0.4 V.

PACKAGE OUTLINES

SAA3009P; SAA3049P: 20 lead DIL; plastic (SOT146).
SAA3049T: 20 lead mini-pack; plastic (SO20; SOT163A).

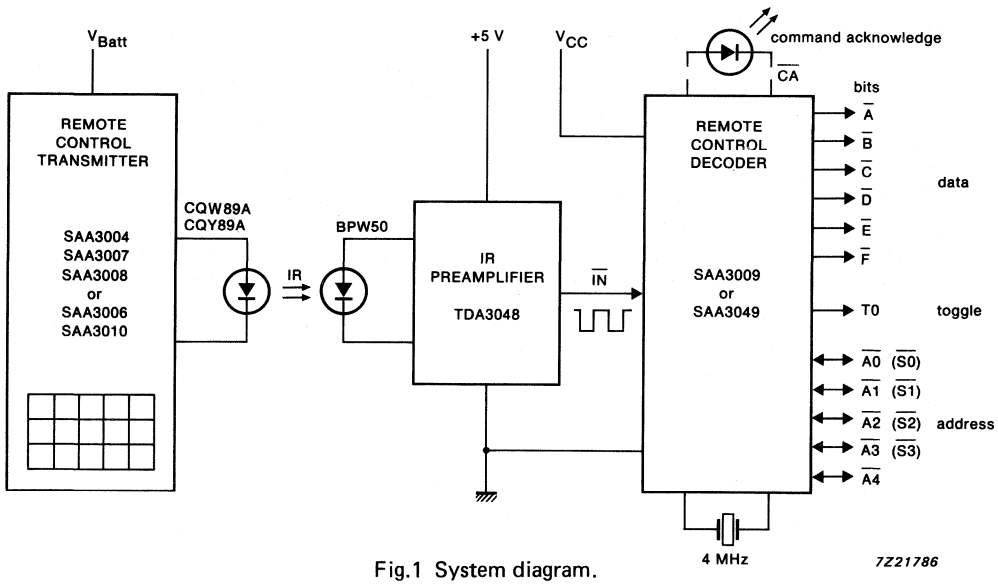


Fig.1 System diagram.

TRANSMITTERS (see individual data sheets for full specifications)

SAA3004 V_{Batt} = 4 to 11 V (max.); 7 x 64 = 448 commands (RECS80 code)

SAA3007 V_{Batt} = 2 to 6.5 V (max.); 20 x 64 = 1280 commands (RECS80 code)

SAA3008 V_{Batt} = 2 to 6.5 V (max.); 20 x 64 = 1280 commands (RECS80 code)

SAA3006 V_{Batt} = 2 to 7.0 V (max.); 32 x 64 = 2048 commands (RC5 code)

SAA3010 V_{Batt} = 2 to 7.0 V (max.); 32 x 64 = 2048 commands (RC5 code)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage				
SAA3009	V_{CC}	−0.5	7.0	V
SAA3049	V_{CC}	−0.8	8.0	V
Input voltage (any pin)				
SAA3009	V_I	−0.5	7.0	V
SAA3049	V_I	−0.8	$V_{CC}+0.8$	V
DC input/output current				
SAA3009 (pins 1 to 8)	$\pm I_I, \pm I_O$	–	20	mA
SAA3009 (all other pins)	$\pm I_I, \pm I_O$	–	10	mA
SAA3049 (any pin)	$\pm I_I, \pm I_O$	–	10	mA
Total power dissipation				
SAA3009	P_{tot}	–	1	W
SAA3049	P_{tot}	–	0.5	W
Operating ambient temperature range				
SAA3009	T_{amb}	0	+70	°C
SAA3049	T_{amb}	−40	+85	°C
Storage temperature range				
SAA3009	T_{stg}	−65	+150	°C
SAA3049	T_{stg}	−65	+150	°C

DEVELOPMENT DATA

CHARACTERISTICS

All voltages measured with respect to ground (V_{EE} = 0 V).

SAA3009: V_{CC} = 4.5 to 5.5 V; T_{amb} = 0 to + 70 °C unless otherwise specified
SAA3049: V_{CC} = 2.5 to 5.5 V; T_{amb} = –40 to + 85 unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
SAA3009		V_{CC}	4.5	5.0	5.5	V
SAA3049		V_{CC}	2.5	–	5.5	V
Supply current						
SAA3009		I_{CC}	–	–	70	mA
SAA3049		I_{CC}	–	0.8	2.0	mA
Input signals (pin 9)						
Input voltage HIGH						
SAA3009		V_{IH}	2.0	–	V_{CC} + 0.5	V
SAA3049		V_{IH}	0.7 V_{CC}	–	V_{CC}	V
Input voltage LOW	active					
SAA3009		V_{IL}	0.5	–	0.8	V
SAA3049		V_{IL}	0	–	0.3 V_{CC}	V
Mode selection (pin 11)						
Input voltage HIGH	note 1					
SAA3009		V_{IH}	2.0	–	V_{CC} + 0.5	V
SAA3049		V_{IH}	0.7 V_{CC}	–	V_{CC}	V
Input voltage LOW	note 2					
SAA3009		V_{IL}	–0.5	–	0.8	V
SAA3049		V_{IL}	0	–	0.3 V_{CC}	V
Command received indicator and mode control (pin 19)	note 3					
Input voltage HIGH						
SAA3009		V_{IH}	3.0	–	V_{CC} + 0.5	V
SAA3049		V_{IH}	0.7 V_{CC}	–	V_{CC}	V
Input voltage LOW						
SAA3009		V_{IL}	–0.5	–	1.5	V
SAA3049		V_{IL}	0	–	0.3 V_{CC}	V
Crystal oscillator						
Oscillator frequency	note 4	f_{osc}	–	4	–	MHz

parameter	conditions	symbol	min.	typ.	max.	unit
SAA3009 OUTPUTS						
10 mA open-drain with internal pull-up resistor						
(pins 1 to 8)						
Output voltage HIGH	$I_{OH} = -50\ \mu A$	V_{OH}	2.4	–	V_{CC}	V
Output voltage LOW	$I_{OL} = 10$ mA	V_{OL}	–	–	1.0	V
Output sink current LOW		I_{OL}	–	–	10	mA
5 mA open-drain without internal pull-up resistor						
(pins 18 and 19)						
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW	$I_{OL} = 5$ mA	V_{OL}	–	–	0.45	V
Output sink current LOW		I_{OL}	–	–	5	mA
1.6 mA open-drain with internal pull-up resistor						
(pins 15, 16 and 17)						
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW	$I_{OL} = 1.6$ mA	V_{OL}	–	–	0.45	V
Output sink current LOW		I_{OL}	–	–	1.6	mA
SAA3049 OUTPUTS						
Open-drain without internal pull-up resistor	note 5					
Output sink current LOW	$V_{CC} = 5\ V \pm 10\%$; $V_{OL} = 0.4$ V	I_{OL}	1.6	3.0	–	mA

DEVELOPMENT DATA

Notes to the characteristics

1. RECS80 decoder for transmitters SAA3004, SAA3007 or SAA3008; SAA3009 has an internal pull-up resistor.
2. RC5 decoder for transmitters SAA3006 or SAA3010.
3. With pin 19 = HIGH, then pins 7, 8, 15, 16 and 17 are address inputs.
   With pin 19 = LOW, then pins 7, 8, 15, 16 and 17 are 4 or 5 address received outputs.

   In Figs 4, 5 and 6 this HIGH/LOW switching is dependent on whether the transistor on pin 19 is fed via a series resistor or not. In both applications pin 19, which toggles several times (see Fig.3) while a valid command is acknowledged, can be used to activate (flash) an LED indicator.
4. A quartz crystal with a frequency of 4 MHz is recommended for the standard transmitter application.
4. Application as output requires connection of an external pull-up resistor.

CHARACTERISTICS (continued)

Reset (pin 14)

The simple circuit is shown in Figs 4, 5 and 6. The alternative reset circuit shown in Fig.2 protects against short term power supply transients by generating a reset.

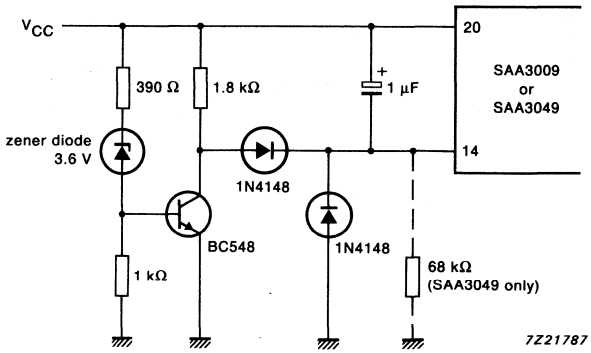


Fig.2 Proposed improved reset circuit.

Infrared signal input (pin 9)

This pin is sensitive to a negative-going edge.

Command received indicator (pin 19)

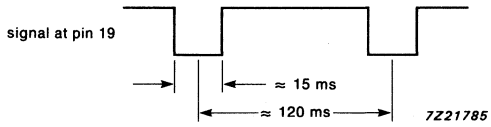
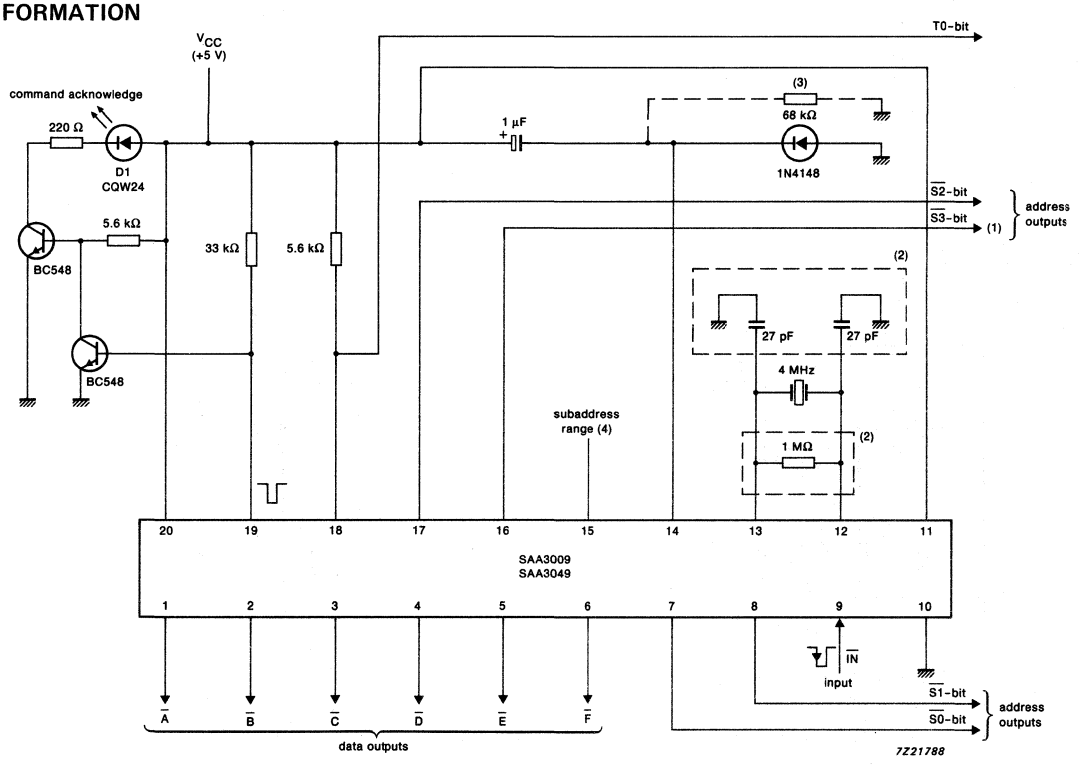


Fig.3 Output diagram of command acknowledge.

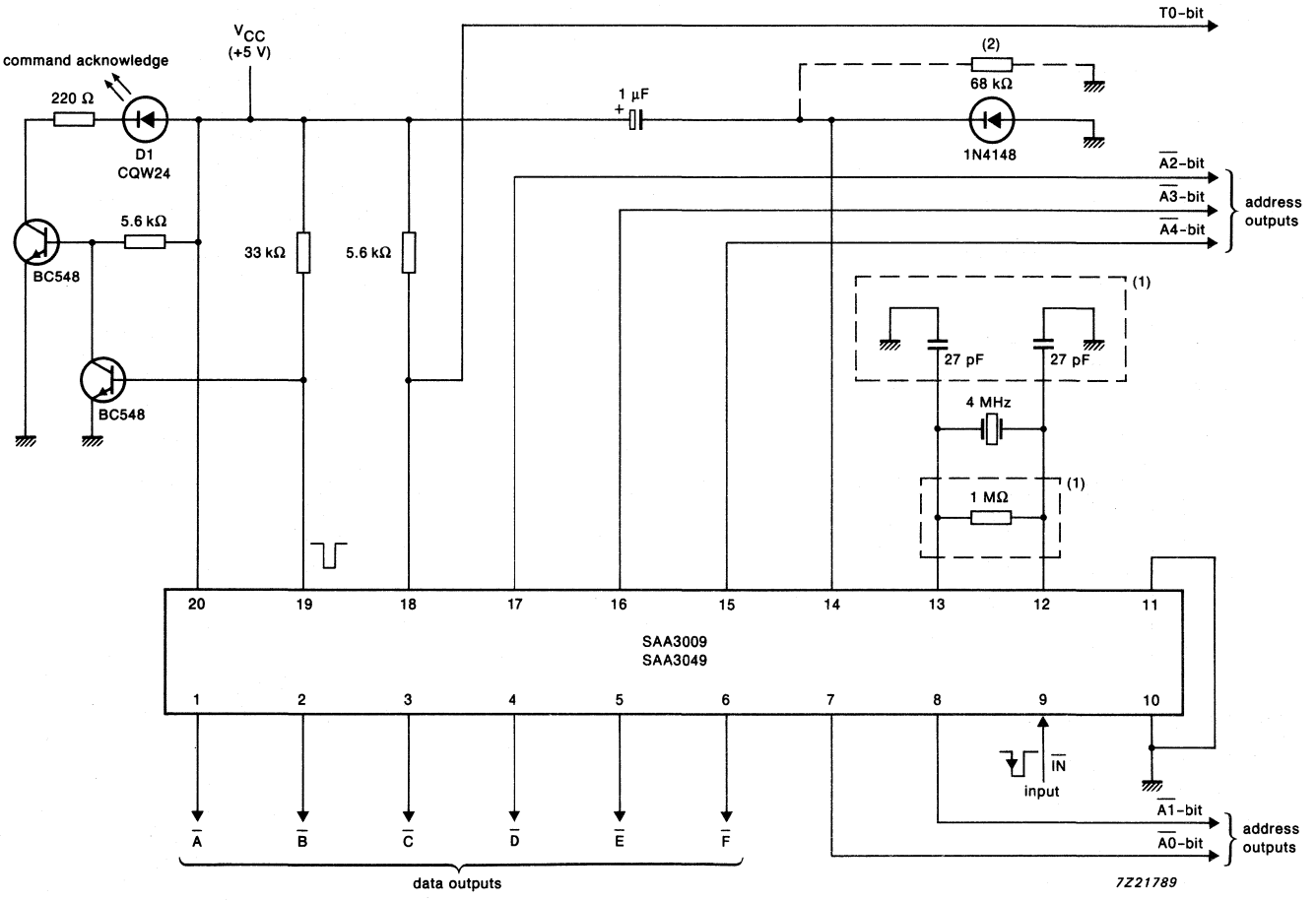
APPLICATION INFORMATION



(1) only for subaddress 8 to 20.
(2) only for SAA3009.
(3) only for SAA3049.
(4) subaddress range:
when LOW (subaddress 8 to 20) pin 15 is connected to ground
when HIGH (subaddress 1 to 7) pin 15 is open (SAA3009)
when HIGH (subaddress 1 to 7) pin 15 is connected via pull-up resistor to V_{CC} (SAA3049)

Fig.4 Remote control decoder with latched 11 (10) -bit parallel outputs (10 (9) -bits inverted) for use with transmitter types SAA3004, SAA3007 or SAA3008; pin 11 is HIGH for RECS80 code.

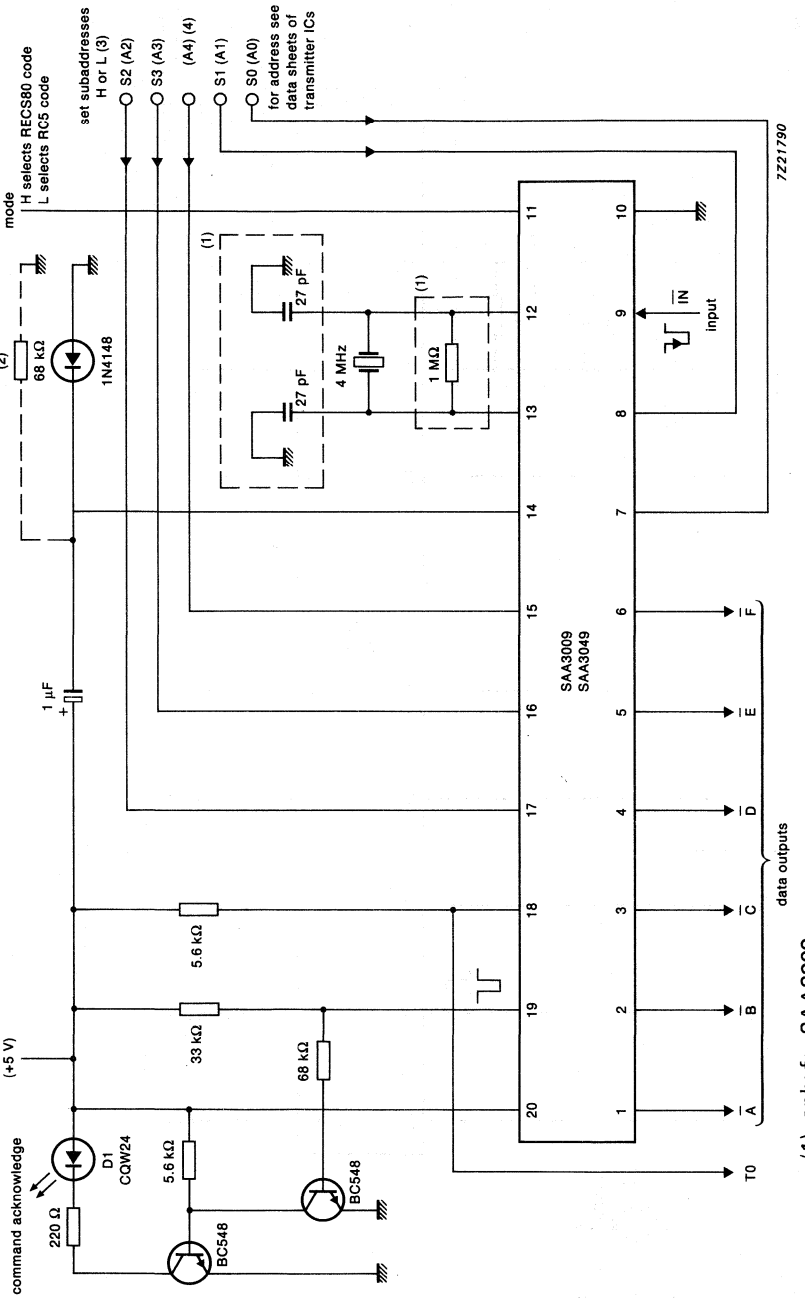
APPLICATION INFORMATION (continued)



(1) only for SAA3009.
(2) only for SAA3049.

Fig.5 Remote control decoder with latched 12-bit parallel outputs (11 bits inverted) for use with transmitter types SAA3006 or SAA3010; pin 11 is LOW for RC5 code.

DEVEL MENT DATA



(1) only for SAA3009.
(2) only for SAA3049.
(3) address inputs:
when LOW address input pin is connected to ground
when HIGH address input pin is open (SAA3009)
when HIGH address input pin is connected via pull-up resistor to V_{CC} (SAA3049)
(4) subaddress range RECS80 code:
when LOW (subaddress 8 to 20) pin 15 is connected to ground
when HIGH (subaddress 1 to 7) pin 15 is open (SAA3009)
when HIGH (subaddress 1 to 7) pin 15 is connected via pull-up resistor to V_{CC} (SAA3049)

Fig.6 Remote control decoder for up to 20 subaddresses with 6 + 1-bit parallel outputs (RECS80 code). Decoder is set for required subaddress by holding address pins HIGH or LOW. Pin 11 is HIGH for use with transmitter types SAA3004, SAA3007 or SAA3008 (RECS80 code). Pin 11 is LOW for use with transmitter types SAA3006 or SAA3010 (RC5 code). Remote control decoder for up to 32 subaddresses with 6 + 1-bit parallel outputs (RC5 code).

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATASHEET

INFRARED REMOTE CONTROL TRANSMITTER RC-5

GENERAL DESCRIPTION

The SAA3010 is intended as a general purpose (RC-5) infrared remote control system for use where a low voltage supply and a large debounce time are expected. The device can generate 2048 different commands and utilizes a keyboard with a single pole switch for each key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands. The keyboard interconnection is illustrated by Fig.3.

The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified in the section **"KEYBOARD OPERATION"**.

Features

- Low voltage requirement
- Biphase transmission technique
- Single pin oscillator
- Test mode facility

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_{DD}	2	–	7	V
Input voltage range*	V_I	−0.5	–	V_{DD}+0.5	V
Input current	I_I	–	–	±10	mA
Output voltage range*	V_O	−0.5	–	V_{DD}+0.5	V
Output current	I_O	–	–	±10	mA
Operating ambient temperature range	T_{amb}	−25	–	85	°C

* V_{DD}+0.5 V must not exceed 9 V.

The use of this device must conform with the Philips Standard number URT-0421.

PACKAGE OUTLINES

28-lead DIL plastic; (SOT117).
28-lead mini-pack; plastic (SO28; SOT136A).

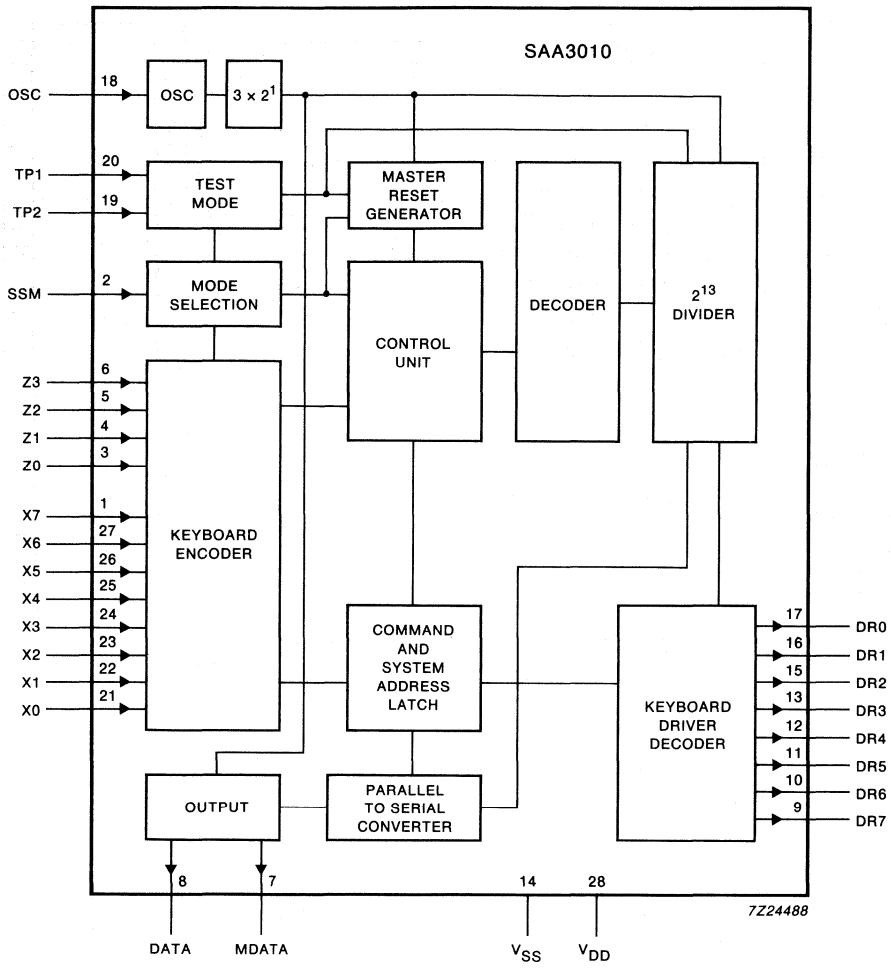


Fig.1 Block diagram.

PINNING

pin	mnemonic	function
1	X7 (IPU)	sense input from key matrix
2	SSM (I)	system mode selection input
3-6	Z0-Z3 (IPU)	sense inputs from key matrix
7	MDATA (OP3)	generated output data modulated with 1/12 the oscillator frequency at a 25% duty factor
8	DATA (OP3)	generated output information
9-13	DR7-DR3 (ODN)	scan drivers
14	V_{SS}	ground (0 V)
15-17	DR2-DR0 (ODN)	scan drivers
18	OSC (I)	oscillator input
19	TP2 (I)	test point 2
20	TP1 (I)	test point 1
21-27	X0-X6 (IPU)	sense inputs from key matrix
28	V_{DD} (I)	voltage supply

(I) = input
(IPU) = input with p-channel pull-up transistor
(ODN) = output with open drain n-channel transistor
(OP3) = output 3-state

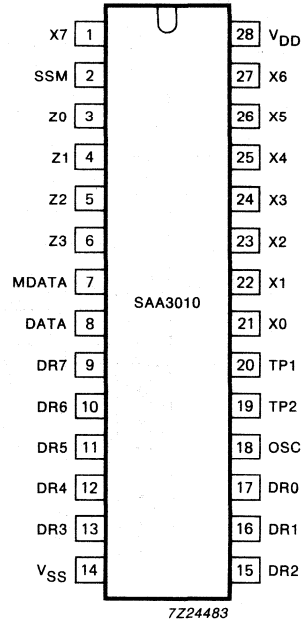


Fig.2 Pinning diagram.

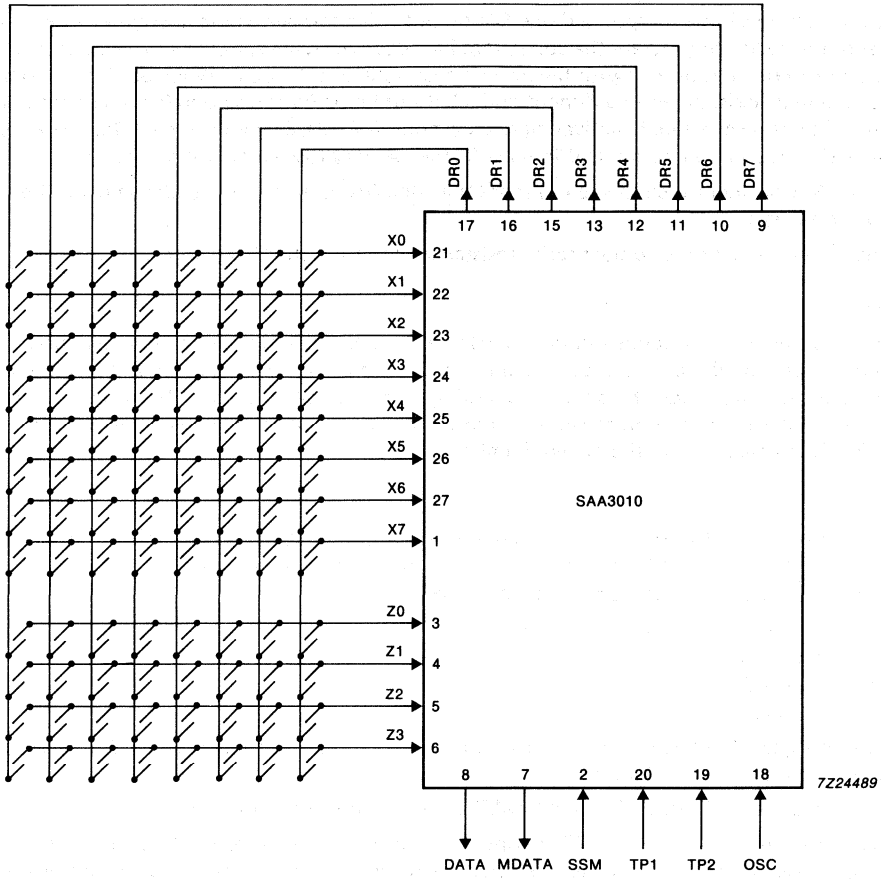


Fig.3 Keyboard interconnection.

FUNCTIONAL DESCRIPTION

Keyboard operation

Every connection of one X-input and one DR-output will be recognized as a legal key operation and will cause the device to generate the corresponding code. The same applies to every connection of one Z-input to one DR-output with the proviso that SSM must be LOW. When SSM is HIGH a wired connection must exist between a Z-input and a DR-output. If no connection is present the system number will not be generated. Activating two or more X-inputs, Z-inputs or Z-inputs and X-inputs at the same time is an illegal action and inhibits further activity (oscillator will not start).

When one X- or Z-input is connected to more than one DR-output, the last scan signal will be considered as legal.

The maximum value of the contact series resistance of the switched keyboard is 7 kΩ.

Inputs

In the quiescent state the command inputs X0 to X7 are held HIGH by an internal pull-up transistor. When the system mode selection (SSM) input is LOW and the system is quiescent, the system inputs Z0 to Z3 are also held HIGH by an internal pull-up transistor. When SSM is HIGH the pull-up transistor for the Z-inputs is switched off, in order to prevent current flow, and a wired connection in the Z-DR matrix provides the system number.

Outputs

The output signal DATA transmits the generated information in accordance with the format illustrated by Fig.4 and Tables 1 and 2. The code is transmitted using a biphase technique as illustrated by Fig.5. The code consists of four parts:

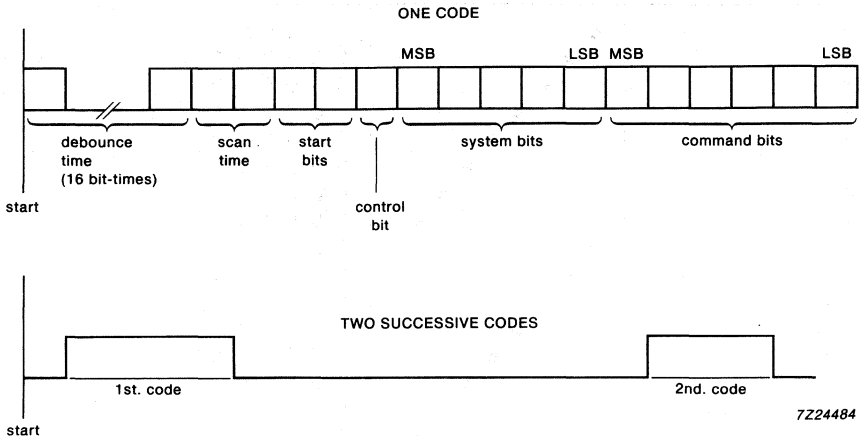
- Start part – 1.5 bits (2 x logic 1)
- Control part – 1 bit
- System part – 5 bits
- Command part – 6 bits

The output signal MDATA transmits the generated information modulated by 1/12 of the oscillator frequency with a 50% duty factor.

In the quiescent state both DATA and MDATA are non-conducting (3-state outputs).

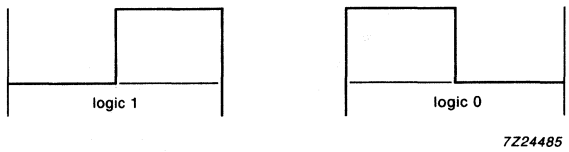
The scan driver outputs DR0 to DR7 are open drain n-channel transistors and conduct when the circuit is quiescent. After a legal key operation the scanning cycle is started and the outputs switched to the conductive state one by one. The DR-outputs were switched off at the end of the preceding debounce cycle.

FUNCTIONAL DESCRIPTION (continued)



Where: debounce time + scan time = 18 bit-times
repetition time = 4 x 16 bit-times

Fig.4 Data output format.



Where: 1 bit-time = 3.2^8 x T_{OSC} = 1.778 ms (typ.)

Fig.5 Biphase transmission technique.

Table 1 Command matrix (X-DR)

code no.	X-lines 0 1 2 3 4 5 6 7	DR-lines 0 1 2 3 4 5 6 7	command bits 5 4 3 2 1 0
0	●	●	0 0 0 0 0 0
1	●	●	0 0 0 0 0 1
2	●	●	0 0 0 0 1 0
3	●	●	0 0 0 0 1 1
4	●	●	0 0 0 1 0 0
5	●	●	0 0 0 1 0 1
6	●	●	0 0 0 1 1 0
7	●	●	0 0 0 1 1 1
8	●	●	0 0 1 0 0 0
9	●	●	0 0 1 0 0 1
10	●	●	0 0 1 0 1 0
11	●	●	0 0 1 0 1 1
12	●	●	0 0 1 1 0 0
13	●	●	0 0 1 1 0 1
14	●	●	0 0 1 1 1 0
15	●	●	0 0 1 1 1 1
16	●	●	0 1 0 0 0 0
17	●	●	0 1 0 0 0 1
18	●	●	0 1 0 0 1 0
19	●	●	0 1 0 0 1 1
20	●	●	0 1 0 1 0 0
21	●	●	0 1 0 1 0 1
22	●	●	0 1 0 1 1 0
23	●	●	0 1 0 1 1 1
24	●	●	0 1 1 0 0 0
25	●	●	0 1 1 0 0 1
26	●	●	0 1 1 0 1 0
27	●	●	0 1 1 0 1 1
28	●	●	0 1 1 1 0 0
29	●	●	0 1 1 1 0 1
30	●	●	0 1 1 1 1 0
31	●	●	0 1 1 1 1 1

FUNCTIONAL DESCRIPTION (continued)

Table 1 Command matrix (X-DR) (continued)

code no.	X-lines 0 1 2 3 4 5 6 7	DR-lines 0 1 2 3 4 5 6 7	command bits 5 4 3 2 1 0
32	●	●	1 0 0 0 0 0
33	●	●	1 0 0 0 0 1
34	●	●	1 0 0 0 1 0
35	●	●	1 0 0 0 1 1
36	●	●	1 0 0 1 0 0
37	●	●	1 0 0 1 0 1
38	●	●	1 0 0 1 1 0
39	●	●	1 0 0 1 1 1
40	●	●	1 0 1 0 0 0
41	●	●	1 0 1 0 0 1
42	●	●	1 0 1 0 1 0
43	●	●	1 0 1 0 1 1
44	●	●	1 0 1 1 0 0
45	●	●	1 0 1 1 0 1
46	●	●	1 0 1 1 1 0
47	●	●	1 0 1 1 1 1
48	●	●	1 1 0 0 0 0
49	●	●	1 1 0 0 0 1
50	●	●	1 1 0 0 1 0
51	●	●	1 1 0 0 1 1
52	●	●	1 1 0 1 0 0
53	●	●	1 1 0 1 0 1
54	●	●	1 1 0 1 1 0
55	●	●	1 1 0 1 1 1
56	●	●	1 1 1 0 0 0
57	●	●	1 1 1 0 0 1
58	●	●	1 1 1 0 1 0
59	●	●	1 1 1 0 1 1
60	●	●	1 1 1 1 0 0
61	●	●	1 1 1 1 0 1
62	●	●	1 1 1 1 1 0
63	●	●	1 1 1 1 1 1

Table 2 System matrix (Z-DR)

syst. no.	Z-lines 0 1 2 3 4 5 6 7	DR-lines 0 1 2 3 4 5 6 7	system bits 4 3 2 1 0
0	●	●	0 0 0 0 0
1	●	●	0 0 0 0 1
2	●	●	0 0 0 1 0
3	●	●	0 0 0 1 1
4	●	●	0 0 1 0 0
5	●	●	0 0 1 0 1
6	●	●	0 0 1 1 0
7	●	●	0 0 1 1 1
8	●	●	0 1 0 0 0
9	●	●	0 1 0 0 1
10	●	●	0 1 0 1 0
11	●	●	0 1 0 1 1
12	●	●	0 1 1 0 0
13	●	●	0 1 1 0 1
14	●	●	0 1 1 1 0
15	●	●	0 1 1 1 1
16	●	●	1 0 0 0 0
17	●	●	1 0 0 0 1
18	●	●	1 0 0 1 0
19	●	●	1 0 0 1 1
20	●	●	1 0 1 0 0
21	●	●	1 0 1 0 1
22	●	●	1 0 1 1 0
23	●	●	1 0 1 1 1
24	●	●	1 1 0 0 0
25	●	●	1 1 0 0 1
26	●	●	1 1 0 1 0
27	●	●	1 1 0 1 1
28	●	●	1 1 1 0 0
29	●	●	1 1 1 0 1
30	●	●	1 1 1 1 0
31	●	●	1 1 1 1 1

FUNCTIONAL DESCRIPTION (continued)

Combined system mode (SSM is LOW)

The X and Z sense inputs have p-channel pull-up transistors, so that they are HIGH, until pulled LOW by connecting them to an output as the result of a key operation. Legal operation of a key in the X-DR or Z-DR matrix will start the debounce cycle, once key contact has been established for 18 bit-times without interruption, the oscillator enable signal is latched and the key may be released. An interruption within the 18 bit-time period resets the device.

At the end of the debounce cycle the DR-outputs are switched off and two scan cycles are started, that switch on the DR-lines one by one. When a Z- or X-input senses a low level, a latch enable signal is fed to the system (Z-input) or command (X-input) latches.

After latching a system number the device will generate the last command (i.e. all command bits logic 1) in the chosen system for as long as the key is operated. Latching of a command number causes the chip to generate this command together with the system number memorized in the system latch. Releasing the key will reset the device if no data is to be transmitted at the time. Once transmission has started the code will complete to the end.

Single system mode (SSM is HIGH)

In the single system mode, the X-inputs will be HIGH as in the combined system mode. The Z-inputs will be disabled by having their pull-up transistors switched off; a wired connection in the Z-DR matrix provides the system code. Only legal key operation in the X-DR matrix will start the debounce cycle, once key contact has been established for 18 bit-times without interruption the oscillator enable signal is latched and the key may be released. An interruption within the 18 bit-time period resets the internal action.

At the end of the debounce cycle the pull-up transistors in the X-lines are switched off and those in the Z-lines are switched on for the first scan cycle. The wired connection in the Z-matrix is then translated into a system number and memorized in the system latch. At the end of the first scan cycle the pull-up transistors in the Z-lines are switched off and the inputs are disabled again; the pull-up transistors in the X-lines are switched on. The second scan cycle produces the command number which, after being latched, is transmitted together with the system number.

Key release detection

An extra control bit is added which will be complemented after key release; this indicates to the decoder that the next code is a new command. This is important in the case where more digits need to be entered (channel numbers of Teletext or Viewdata pages). The control bit will only be complemented after the completion of at least one code transmission. The scan cycles are repeated before every code transmission, so that even with "take over" of key operation during code transmission the right system and command numbers are generated.

Reset action

The device will be reset immediately a key is released during:

- debounce time
- between two codes.

When a key is released during matrix scanning, a reset will occur if:

- a key is released while one of the driver outputs is in the low ohmic state (logic 0)
- a key is released before that key has been detected
- there is no wired connection in the Z-DR matrix when SSM is HIGH.

Oscillator

The OSC is the input/output for a 1-pin oscillator. The oscillator is formed by a ceramic resonator, TOKO CRK429, order code, 2422 540 98069 or equivalent. A resistor of 6.8 kΩ must be placed in series with the resonator. The resistor and resonator are grounded at one side.

Test

Initialization of the circuit is performed when TP1, TP2 and OSC are HIGH. All internal nodes are defined except for the LATCH. The latch is defined when a scan cycle is started by pulling down an X- or Z-input while the oscillator is running.

If the debounce cycle has been completed, the scan cycle can be completed 3×2^3 faster, by setting TP1 HIGH.

If the scan cycle has been completed, the contents of the latch can be read 3×2^7 faster by setting TP2 HIGH.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	8.5	V
Input voltage range *	V_I	−0.5	V_{DD}+0.5	V
Output voltage range *	V_O	−0.5	V_{DD}+0.5	V
Input current	I_I	−	±10	mA
Output current	I_O	−	±10	mA
Maximum power dissipation				
OSC output	P_O	−	50	mW
other outputs	P_O	−	100	mW
Total power dissipation	P_{tot}	−	200	mW
Operating ambient temperature range	T_{amb}	−25	+ 85	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

* V_{DD}+0.5 V must not exceed 9.0 V.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling, however, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

DC CHARACTERISTICS

T_{amb} = −25 °C to + 70 °C; V_{DD} = 2.0 to 7.0 V unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	2.0	–	7.0	V
Quiescent supply current	note 1 T_{amb} = 25 °C; I_O = 0 mA at all outputs. X0 to X7 and Z0 to Z3 at V_{DD} TP1, TP2, OSC at V_{SS} SSM at V_{SS} or V_{DD}	I_{DD}	–	–	10	μA
INPUTS						
Keyboard inputs X and Z with p-channel pull-up transistor						
Input current at each input	V_I = 0 V; TP1 = TP2 = SSM = LOW	$-I_I$	10	–	600	μA
Input voltage HIGH	note 2	V_{IH}	$0.7V_{DD}$	–	V_{DD}	V
Input voltage LOW	note 2	V_{IL}	0	–	$0.3V_{DD}$	V
Input leakage current	T_{amb} = 25 °C; V_I = 7 V; TP1 = TP2 = HIGH	I_{LI}	–	–	1	μA
Input leakage current	T_{amb} = 25 °C; V_I = 0 V; TP1 = TP2 = HIGH	$-I_{LI}$	–	–	1	μA
OSC						
Input leakage current	T_{amb} = 25 °C; V_I = 0 V; TP1 = TP2 = HIGH	$-I_{LI}$	–	–	2	μA
Input current	T_{amb} = 25 °C; V_I = V_{DD}	I_{OSC}	4.5	–	30	μA
SSM, TP1, TP2						
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD}	V
Input voltage LOW		V_{IL}	0	–	$0.3V_{DD}$	V
Input leakage current	T_{amb} = 25 °C; V_I = 7.0 V	I_{LI}	–	–	1	μA
Input leakage current	T_{amb} = 25 °C; V_I = 0 V	$-I_{LI}$	–	–	1	μA

DC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
OUTPUTS						
DATA, MDATA						
Output voltage HIGH	$I_{OH} = -0.4$ mA	V_{OH}	$V_{DD}-0.3$	–	–	V
Output voltage LOW	$I_{OL} = 0.6$ mA	V_{OL}	–	–	0.3	V
Output leakage current	$V_O = 7.0$ V	$+I_{LO}$	–	–	10	μA
	$V_O = 7.0$ V; $T_{amb} = 25\ ^oC$	$+I_{LO}$	–	–	1	μA
	$V_O = 0$ V	$-I_{LO}$	–	–	20	μA
	$V_O = 0$ V; $T_{amb} = 25\ ^oC$	$-I_{LO}$	–	–	2	μA
DR0 to DR7						
Output voltage LOW	$I_{OL} = 0.3$ mA	V_{OL}	–	–	0.3	V
Output leakage current	$V_O = 7.0$ V	$+I_{LO}$	–	–	10	μA
	$V_O = 7.0$ V; $T_{amb} = 25\ ^oC$	$+I_{LO}$	–	–	1	μA

Notes to the DC characteristics

1. Quiescent supply current measurement must be preceded by the initialization procedure described in the **TEST** section.
2. This DC test condition protects the AC performance of the output. The DC current requirements in the actual application are lower.

AC CHARACTERISTICS

T_{amb} = −25 to + 85 °C; V_{DD} = 2.0 to 7.0 V unless otherwise stated

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator frequency	C_L = 160 pF; Figs 6 and 7					
operational		f_{OSC}	−	−	450	kHz
free-running		f_{OSC}	10	−	120	kHz

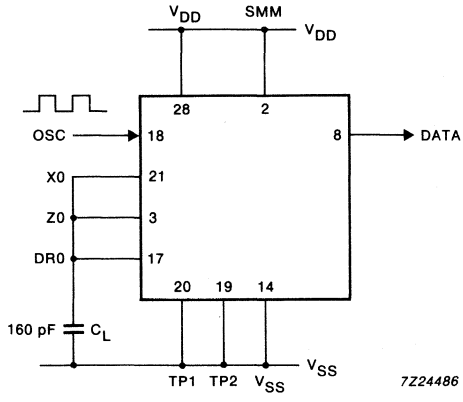


Fig.6 Test set-up for maximum f_{OSC} measurement.

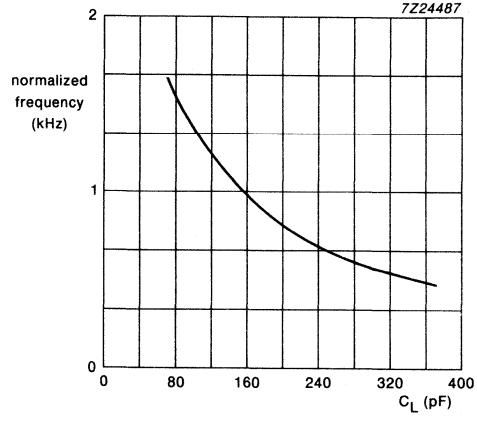


Fig.7 Typical normalized frequency as a function of keyboard load capacitance.

INFRARED REMOTE CONTROL TRANSMITTER (RC-5)

GENERAL DESCRIPTION

The SAA3027 is intended for a general purpose (RC-5) infrared remote control system. The device can generate 2048 different commands and utilizes a keyboard with a single-pole switch per key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands.

The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified later in this publication (see KEY ACTIVITIES).

Features

- Transmitter for 32 x 64 commands
- One transmitter controls 32 systems
- Very low current consumption
- For infrared transmission link
- Transmission by biphase technique
- Short transmission times; speed-up of system reaction time
- LC oscillator; no crystal required
- Input protection
- Test mode facility

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	4,75 to 12,6	V
Input voltage range	V_I	$-0,5$ to $(V_{DD}+0,5)$	V*
Input current	$\pm I_I$	max. 10	mA
Output voltage range	V_O	$-0,5$ to $(V_{DD}+0,5)$	V*
Output current	$\pm I_O$	max. 10	mA
Operating ambient temperature range	T_{amb}	-25 to $+85$	°C

* V_{DD} + 0,5 V not to exceed 15 V.

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

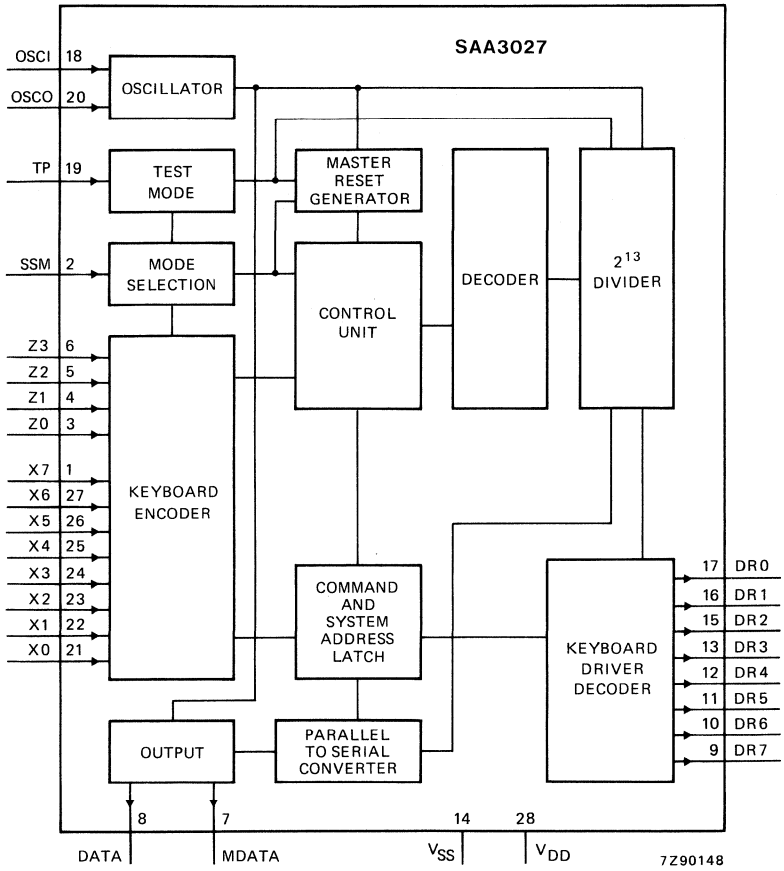


Fig. 1 Block diagram.

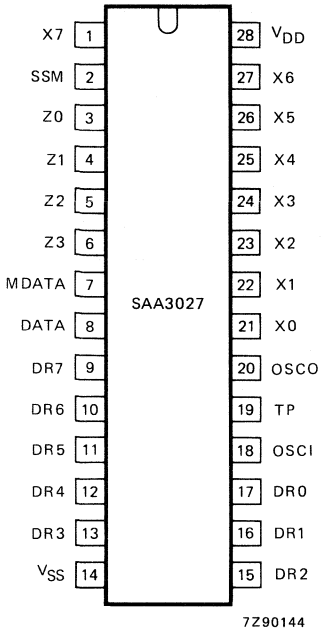
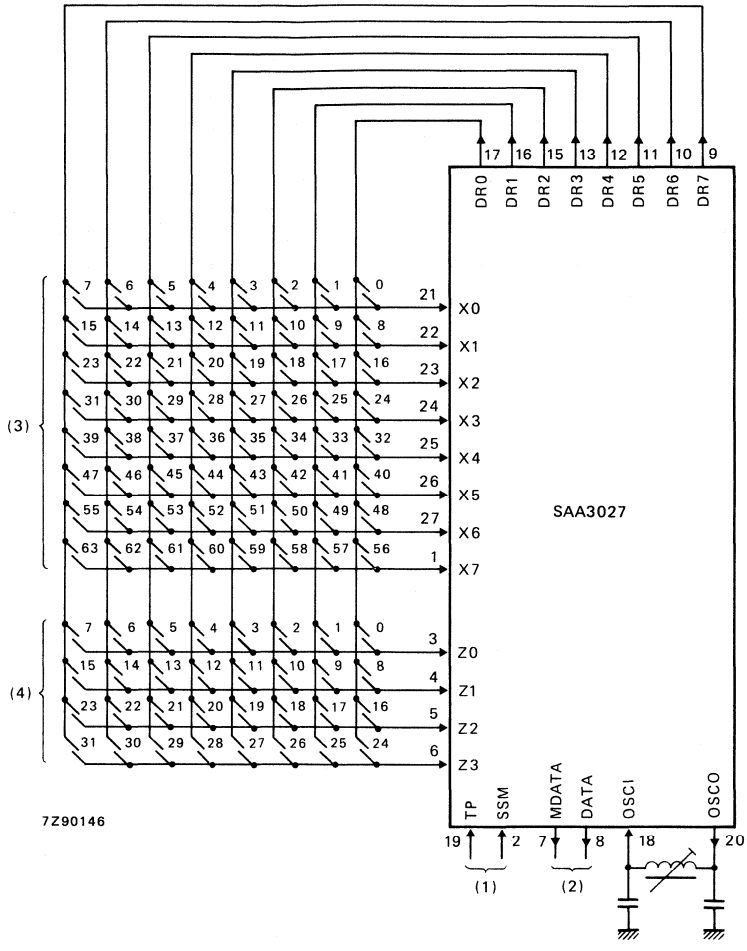


Fig. 2 Pinning diagram.

PINNING

14	V_{SS}	negative supply (ground)
28	V_{DD}	positive supply
21	X0	keyboard command inputs with P-channel pull-up transistors
22	X1	
23	X2	
24	X3	
25	X4	
26	X5	
27	X6	
1	X7	
3	Z0	keyboard system inputs with P-channel pull-up transistors
4	Z1	
5	Z2	
6	Z3	
2	SSM	system mode selection input
19	TP	test pin
18	OSC1	oscillator input
20	OSC0	oscillator output
17	DR0	scan driver outputs with open drain N-channel transistors
16	DR1	
15	DR2	
13	DR3	
12	DR4	
11	DR5	
10	DR6	
9	DR7	
7	MDATA	remote signal outputs (3-state outputs)
8	DATA	



(1) Programming inputs for operating modes, test mode and reset.
(2) Remote signal outputs.
(3) Keyboard command code matrix 8 x 8.
(4) Keyboard system code matrix 4 x 8.

Fig. 3 Keyboard interconnection.

FUNCTIONAL DECRIPTION

Combined system mode (SSM = LOW)

The X and Z-lines are active HIGH in the quiescent state. Legal key operation either in the X-DR or Z-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator-enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the DR-outputs are switched off and two scan cycles are started, switching on the DR-outputs one by one. When a Z or X-input senses a LOW level, a latch-enable signal is fed to the system address or command latches, depending on whether sensing was found in the Z or X-input matrix. After latching a system address number, the device will generate the last command (i.e. all command bits '1') in the chosen system as long as the key is pressed. Latching of a command number causes the device to generate this command together with the system address number stored in the system address latch. Releasing the key will reset the internal action if no data is transmitted at that time. Once the transmission is started, the signal will be finished completely.

Single system mode (SSM = HIGH)

The X-lines are active HIGH in the quiescent state; the pull-up transistors of the Z-lines are switched off and the inputs are disabled. Only legal key operation in the X-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator-enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the pull-up transistors in the X-lines are switched off, those in the Z-lines are switched on during the first scan cycle. The wired connection in the Z-matrix is then translated into a system address number and stored in the system address latch. At the end of the first scan cycle the pull-up transistors in the Z-lines are switched off and the inputs are disabled again, while the transistors in the X-lines are switched on. The second scan cycle produces the command number which, after latching, is transmitted together with the system address number.

Inputs

The command inputs X0 to X7 carry a logical '1' in the quiescent state by means of an internal pull-up transistor. When SSM is LOW, the system inputs Z0 to Z3 also carry a logical '1' in the quiescent state by means of an internal pull-up transistor.

When SSM is HIGH, the transistors are switched off and no current flows via the wired connection in the Z-DR matrix.

Oscillator

OSCI and OSCO are the input/output respectively of a two-pin oscillator. The oscillator is formed externally by one inductor and two capacitors and operates at 72 kHz (typical).

Key-release detection

An extra control bit is added which will be complemented after key-release. In this way the decoder gets an indication that shows if the next code is to be considered as a new command. This is very important for multi-digit entry (e.g. by channel numbers or Teletext/Viewdata pages). The control bit will only be complemented after finishing at least one code transmission. The scan cycles are repeated before every code transmission, so that, even by 'take-over' of key operation during code transmission, the correct system and command numbers are generated.

FUNCTIONAL DESCRIPTION (continued)

Outputs

The output DATA carries the generated information according to the format given in Fig. 4 and Tables 1 and 2. The code is transmitted in biphase; definitions of logical '1' and '0' are given in Fig. 5.

The code consists of four parts:

- Start part formed by 2 bits (two times a logical '1');
- Control part formed by 1 bit;
- System part formed by 5 bits;
- Command part formed by 6 bits.

The output MDATA carries the same information as output DATA but is modulated on a carrier frequency of half the oscillator frequency, so that each bit is presented as a burst of 32 oscillator periods. To reduce power consumption, the carrier frequency has a 25% duty cycle.

In the quiescent state, both outputs are non-conducting (3-state outputs). The scan drivers DR0 to DR7 are of the open drain N-channel type and are conducting in the quiescent state of the circuit. After a legal key operation, a scanning procedure is started so that they are switched into the conducting state one after the other.

Reset action

The circuit will be reset immediately when a key release occurs during:

- debounce time;
- between two codes.

When a key release occurs during scanning of the matrix, a reset action will be accomplished if:

- the key is released while one of the driver outputs is in the low-ohmic '0' state;
- the key is released before detection of that key;
- there is no wired connection in the Z-DR matrix while SSM is HIGH.

Test pin

The test pin TP is an input which can be used for testing purposes.

When LOW, the circuit operates normally.

When HIGH, all pull-up transistors are switched off, the control bit is set to zero and the output data is 2^6 times faster than normal.

When Z2 = Z3 = LOW, the counter will be reset to zero.

KEY ACTIVITIES

Every connection of one X-input and one DR-output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating more than one X-input at a time is an illegal keyboard operation and no circuit action is taken (oscillator does not start).

When SSM is LOW, every connection of one Z-input and one DR-output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating two or more Z-inputs, or Z-inputs and X-inputs, at one time is an illegal keyboard operation and no circuit action is taken.

When SSM is HIGH, a wired connection must be made between a Z-input and a DR-output. If no connection is made, the code is not generated.

When one X or Z-input is connected to more than one DR-output, the last scan signal is considered legal.

The maximum allowable value of the contact series resistance of the keyboard switches is 10 kΩ.

Z2 or Z3 must be connected to V_{DD} to avoid unwanted supply current.

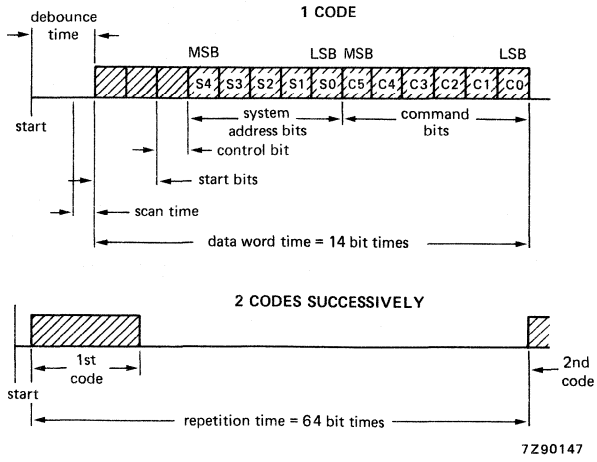


Fig. 4 DATA output format (RC-5).

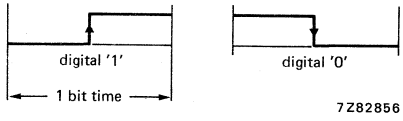


Fig. 5 Biphase transmission code; 1 bit time = $2^7 \times T_{OSC}$ = 1,778 ms (typical), where T_{OSC} is the oscillator period time.

Table 1 Command matrix X-DR

code no.	X-lines X.. 0	1	2	3	4	5	6	7	DR-lines DR.. 0	1	2	3	4	5	6	7	command bits C.. 5	4	3	2	1	0
0	●								●								0	0	0	0	0	0
1	●									●							0	0	0	0	0	1
2	●										●						0	0	0	0	1	0
3	●											●					0	0	0	0	1	1
4	●												●				0	0	0	1	0	0
5	●													●			0	0	0	1	0	1
6	●														●		0	0	0	1	1	0
7	●															●	0	0	0	1	1	1
8		●							●								0	0	1	0	0	0
9		●								●							0	0	1	0	0	1
10		●									●						0	0	1	0	1	0
11		●										●					0	0	1	0	1	1
12		●											●				0	0	1	1	0	0
13		●												●			0	0	1	1	0	1
14		●													●		0	0	1	1	1	0
15		●														●	0	0	1	1	1	1
16			●						●								0	1	0	0	0	0
17			●							●							0	1	0	0	0	1
18			●								●						0	1	0	0	1	0
19			●									●					0	1	0	0	1	1
20			●										●				0	1	0	1	0	0
21			●											●			0	1	0	1	0	1
22			●												●		0	1	0	1	1	0
23			●													●	0	1	0	1	1	1
24				●					●								0	1	1	0	0	0
25				●						●							0	1	1	0	0	1
26				●							●						0	1	1	0	1	0
27				●								●					0	1	1	0	1	1
28				●									●				0	1	1	1	0	0
29				●										●			0	1	1	1	0	1
30				●											●		0	1	1	1	1	0
31				●												●	0	1	1	1	1	1

code no.	X-lines X..								DR-lines DR..								command bits C..					
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	5	4	3	2	1	0
32					●				●								1	0	0	0	0	0
33					●					●							1	0	0	0	0	1
34					●						●						1	0	0	0	1	0
35					●							●					1	0	0	0	1	1
36					●								●				1	0	0	1	0	0
37					●									●			1	0	0	1	0	1
38					●										●		1	0	0	1	1	0
39					●											●	1	0	0	1	1	1
40						●			●								1	0	1	0	0	0
41						●				●							1	0	1	0	0	1
42						●					●						1	0	1	0	1	0
43						●						●					1	0	1	0	1	1
44						●							●				1	0	1	1	0	0
45						●								●			1	0	1	1	0	1
46						●									●		1	0	1	1	1	0
47						●										●	1	0	1	1	1	1
48							●		●								1	1	0	0	0	0
49							●			●							1	1	0	0	0	1
50							●				●						1	1	0	0	1	0
51							●					●					1	1	0	0	1	1
52							●						●				1	1	0	1	0	0
53							●							●			1	1	0	1	0	1
54							●								●		1	1	0	1	1	0
55							●									●	1	1	0	1	1	1
56								●	●								1	1	1	0	0	0
57								●		●							1	1	1	0	0	1
58								●			●						1	1	1	0	1	0
59								●				●					1	1	1	0	1	1
60								●					●				1	1	1	1	0	0
61								●						●			1	1	1	1	0	1
62								●							●		1	1	1	1	1	0
63								●								●	1	1	1	1	1	1

Table 2 System matrix Z-DR

system no.	Z-lines Z..				DR-lines DR..								system bits S..				
	0	1	2	3	0	1	2	3	4	5	6	7	4	3	2	1	0
0	●				●								0	0	0	0	0
1	●					●							0	0	0	0	1
2	●						●						0	0	0	1	0
3	●							●					0	0	0	1	1
4	●								●				0	0	1	0	0
5	●									●			0	0	1	0	1
6	●										●		0	0	1	1	0
7	●											●	0	0	1	1	1
8		●			●								0	1	0	0	0
9		●				●							0	1	0	0	1
10		●					●						0	1	0	1	0
11		●						●					0	1	0	1	1
12		●							●				0	1	1	0	0
13		●								●			0	1	1	0	1
14		●									●		0	1	1	1	0
15		●										●	0	1	1	1	1
16			●		●								1	0	0	0	0
17			●			●							1	0	0	0	1
18			●				●						1	0	0	1	0
19			●					●					1	0	0	1	1
20			●						●				1	0	1	0	0
21			●							●			1	0	1	0	1
22			●								●		1	0	1	1	0
23			●									●	1	0	1	1	1
24				●	●								1	1	0	0	0
25				●		●							1	1	0	0	1
26				●			●						1	1	0	1	0
27				●				●					1	1	0	1	1
28				●					●				1	1	1	0	0
29				●						●			1	1	1	0	1
30				●							●		1	1	1	1	0
31				●								●	1	1	1	1	1

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}	−0,5 to +15	V
Input voltage range	V_I	−0,5 to (V_{DD} + 0,5)	V*
Input current	$\pm I_I$	max. 10	mA
Output voltage range	V_O	−0,5 to (V_{DD} + 0,5)	V*
Output current	$\pm I_O$	max. 10	mA
Power dissipation output OSCO	P_O	max. 50	mW
Power dissipation per output (all other outputs)	P_O	max. 100	mW
Total power dissipation per package	P_{tot}	max. 200	mW
Operating ambient temperature range	T_{amb}	−25 to +85	°C
Storage temperature range	T_{stg}	−55 to +150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

* V_{DD} + 0,5 V not to exceed 15 V.

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −25 to 85 °C unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage	–	V_{DD}	4,75	–	12,6	V
Supply current at I_O = 0 mA for all outputs; X0 to X7 and Z3 at V_{DD}; all other inputs at V_{DD} or V_{SS}; excluding leakage current from open drain N-channel outputs; T_{amb} = 25 °C	12,6	I_{DD}	–	–	10	μA
Inputs						
Keyboard inputs X and Z with P-channel pull-up transistors						
Input current (each input) at V_I = 0 V; TP = SSM = LOW	4,75 to 12,6	$-I_I$	10	–	300	μA
Input voltage HIGH	4,75 to 12,6	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	4,75 to 12,6	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at T_{amb} = 25 °C; TP = HIGH;						
V_I = 12,6 V	12,6	I_{IR}	–	–	1	μA
V_I = 0 V	12,6	$-I_{IR}$	–	–	1	μA
SSM, TP and OSCI inputs						
Input voltage HIGH	4,75 to 12,6	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	4,75 to 12,6	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at T_{amb} = 25 °C;						
V_I = 12,6 V	12,6	I_{IR}	–	–	1	μA
V_I = 0 V	12,6	$-I_{IR}$	–	–	1	μA
Outputs						
DATA, MDATA outputs						
Output voltage HIGH at $-I_{OH}$ = 0,8 mA	4,75 to 12,6	V_{OH}	V_{DD} − 0,6	–	–	V
Output voltage LOW at I_{OL} = 0,8 mA	4,75 to 12,6	V_{OL}	–	–	0,4	V
Output leakage current at:						
V_O = 12,6 V	12,6	I_{OR}	–	–	10	μA
V_O = 0 V	12,6	$-I_{OR}$	–	–	20	μA
T_{amb} = 25 °C;						
V_O = 12,6 V	12,6	I_{OR}	–	–	1	μA
V_O = 0 V	12,6	$-I_{OR}$	–	–	2	μA

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
DR0 to DR7 outputs						
Output voltage LOW; at I_{OL} = 0,35 mA	4,75 to 12,6	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 12,6 V	12,6	I_{OR}	–	–	10	μA
at V_O = 12,6 V; T_{amb} = 25 °C	12,6	I_{OR}	–	–	1	μA
OSCO output						
Output voltage HIGH at $-I_{OH}$ = 0,2 mA; OSCI = V_{SS}	4,75 to 12,6	V_{OH}	$V_{DD}-0,6$	–	–	V
Output voltage LOW at $-I_{OL}$ = 0,45 mA; OSCI = V_{DD}	4,75 to 12,6	V_{OL}	–	–	0,5	V
Oscillator						
Maximum oscillator frequency at C_L = 40 pF (Figs 6 and 7)	4,75	f_{OSCI}	75	72	–	kHz
	6	f_{OSCI}	120	72	–	kHz
	12,6	f_{OSCI}	300	72	–	kHz

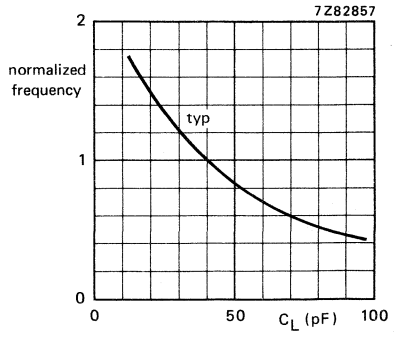


Fig. 6 Typical normalized input frequency as a function of the load (keyboard) capacitance.

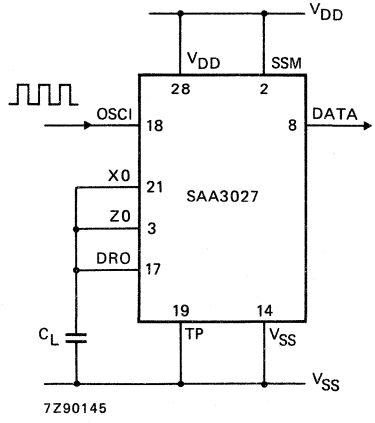


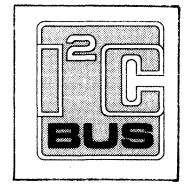
Fig. 7 Test circuit for measurement of maximum oscillator frequency.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	September 1990

SAA3028

Infrared remote control transcoder (RC-5)



FEATURES

- Converts RC-5 biphase coded signals into binary equivalents
- Two data inputs
- Rejects all codes not in RC-5 format
- I²C output interface capability
- Power-off facility
- Power-on-reset for defined start-up

GENERAL DESCRIPTION

The SAA3028 is intended for use in general purpose (RC-5) remote control systems. The main function of this integrated circuit is to convert RC-5 biphase coded signals into equivalent binary values. Two input circuits are available for RC-5 coded signals. The input used is that at which an active code is first detected. Coded signals not in RC-5 format are rejected. Data input and output is by serial transfer, the output interface being compatible for I²C-bus operation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage range		4.5	5.5	V
I_{DD}	supply current (quiescent)	V_{DD} = 5.5 V; T_{amb} = 25 °C	-	200	µA
T_{amb}	operating temperature range		−25	+85	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA3028P	16	16	plastic	SOT38D
SAA3028T	16	16	mini-pack	SO16L; SOT162A

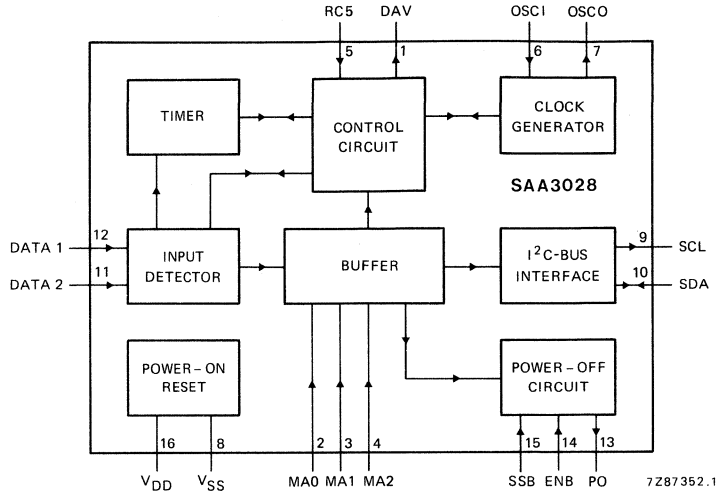


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DAV	1	data valid output with open drain n-channel transistor
MA0	2	master address input 0
MA1	3	master address input 1
MA2	4	master address input 2
RC5	5	data 2 input select
OSCI	6	oscillator input
OSCO	7	oscillator output
V_{SS}	8	negative supply (ground)
SCL	9	I^2C bus serial clock line
SDA	10	I^2C bus serial data line
DATA 2	11	data 2 input
DATA 1	12	data 1 input
PO	13	power-off signal output with open drain n-channel transistor
ENB	14	enable input
SSB	15	set standby input
V_{DD}	16	positive supply (+5 V)

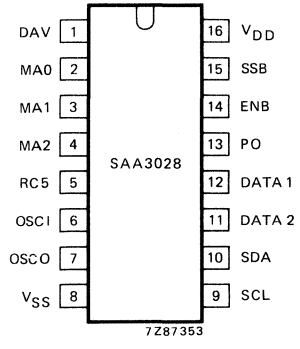


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Input function

The two data inputs are accepted into the buffer as follows:

- DATA 1 Only biphase coded signals which conform to the RC-5 format are accepted at this input.
- DATA 2 This input performs according to the logic state of the select input RC-5. Only when RC-5 = HIGH, DATA 2 input will accept the RC-5 coded signals.

The input detector selects the input, DATA 1 or DATA 2, in which a HIGH to LOW transition is first detected. The selected input is then accepted by the buffer for code conversion. All signals received that are not in the RC-5 or RC-5(ext) format are rejected. Note that in a steady state DATA 1 and DATA 2 are LOW.

Formats of RC-5 biphase coded signals are shown in Fig.3; the codes commence from the left of the formats shown. The bit-times of the biphase codes are defined in Fig.4.

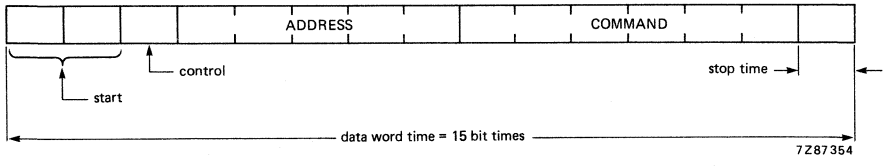


Fig.3 RC-5 code format: the first start bit is used only for detection and input gain-setting; stop time = 1.5 bit-times (nominal).

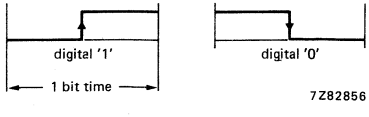


Fig.4 Biphase code definition: RC-5 bit-time = 2^7 x T_{OSC} = 1.778 ms (typical).

More information is added to the input data held in the buffer in order to make it suitable for transmission via the I²C interface. The information now held in the buffer is shown in Table 1

Table 1 RC-5 buffer contents

CONTENTS	NUMBER OF BITS
data valid indicator	1
format indicator	1
input indicator	1
control	1
address data	5
command data	6

The information assembled in the buffer is subjected to the following controls before being made available at the I²C interface:

ENB = HIGH Enables the set standby input SSB.

SSB = LOW Causes power-off output PO to go HIGH.

PO = HIGH This occurs when the set standby input SSB = LOW and allows the existing values in the buffer to be overwritten by the new binary equivalent values. After ENB = LOW, SSB is don't care.

PO = LOW This occurs according to the type of code being processed, as follows:
RC-5. When the binary equivalent value is transferred to the buffer.
At power-on, PO is reset to LOW.

DAV = LOW This occurs when the buffer contents are valid. If the buffer is not empty, or an output transfer is taking place, the new binary values are discarded.

Output function

The data assembled in the buffer in the format shown in Fig.5 for RC-5 binary equivalent values. The data is output serially, starting from the left of the formats.

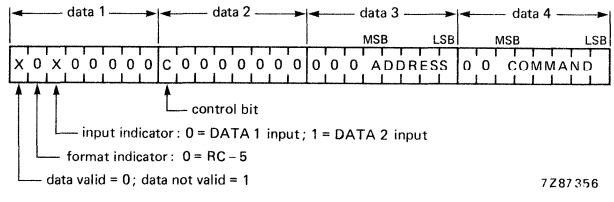


Fig.5 RC-5 binary equivalent value format.

The output signal DAV, derived in the buffer from the data valid bit, is provided to facilitate use of the transcoder on an interrupt basis. This output is reset to LOW during power-on.

The I²C interface allows transmission on a bidirectional, two-wire I²C-bus. The interface is a slave transmitter with a built-in slave address, having a fixed 7-bit binary value of 0100110.

Serial output of the slave address to the I²C bus starts from the left-hand bit.

Oscillator

The oscillator can comprise a ceramic resonator circuit as shown in Fig.6. The typical frequency of oscillation is 455 kHz.

(1) Catalogue number of ceramic resonator: 2422 540 98008.

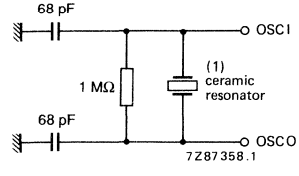


Fig.6 Oscillator circuit.

I²C-bus transmission

Formats for I²C transmission in low- and high-speed modes shown respectively in Figs.7 and 8.

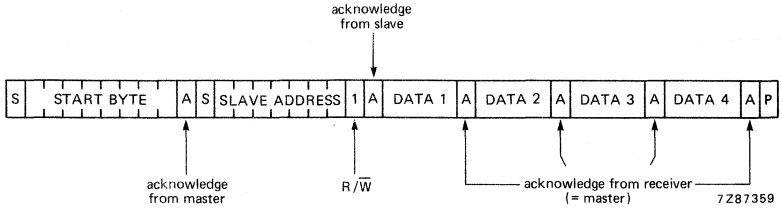


Fig.7 Format for transmission in I²C low-speed mode.

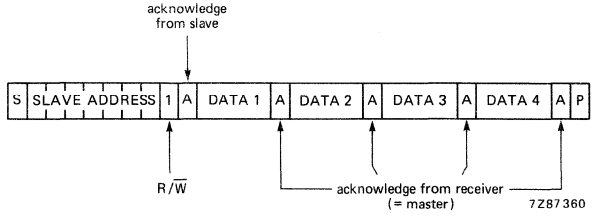


Fig.8 Format for transmission in I²C high-speed mode.

Note to figures 7 and 8

When R/$\overline{W}$ bit = 0; the slave generates an $\overline{ACK}$ (negative acknowledge), leaves the data line HIGH and waits for a stop (P) condition.
When the receiver generates an $\overline{ACK}$; the slave leaves the data line HIGH and waits for P (the slave acting as if all data has been transmitted).
When all data has been transmitted, the data line remains HIGH and the slave waits for P.

LIMITING VALUES

Limiting values in accordance with the absolute maximum system (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply range with respect to V_{SS}	−0.5	+15	V
V_I	input voltage range	−0.5	V_{DD}+0.5*	V
$\pm I_I$	input current	-	10	mA
V_O	output voltage range	−0.5	V_{DD}+0.5*	V
$\pm I_O$	output current	-	10	mA
P_O	power dissipation output OSCO	-	50	mW
P_O	power dissipation per output (all other outputs)	-	100	mW
P_{tot}	total power dissipation per package	-	200	mW
T_{amb}	operating ambient temperature range	−25	+85	°C
T_{stg}	storage temperature range	−55	+150	°C

HANDLING

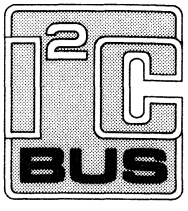
Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

* V_{DD} + 0.5 V not to exceed 15 V.

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −25 to 85 °C; at V_{DD} = 4.5 to 5.5 V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.5	-	5.5	V
I_{DD}	supply current; quiescent	T_{amb} = 25 °C; V_{DD} = 5.5 V	-	-	200	µA
Inputs						
MA0,MA1,MA2, DATA 1,DATA 2, RC5,SCL,ENB,SSB,OSCI						
V_{IH}	input voltage HIGH		0.7V_{DD}	-	V_{DD}	V
V_{IL}	input voltage LOW		0	-	0.3V_{DD}	V
I_{LI}	input leakage current	V_I = 5.5 V; T_{amb} = 25 °C; V_{DD} = 5.5 V	-	-	1	µA
I_{LI}	input leakage current	V_I = 0 V; T_{amb} = 25 °C; V_{DD} = 5.5 V	-	-	−1	µA
Outputs						
DAV,PO						
V_{OL}	output voltage LOW	I_{OL} = 1.6 mA	-	-	0.4	V
I_{LO}	output leakage current	V_O = 5.5 V; T_{amb} = 25 °C; V_{DD} = 5.5 V	-	-	1	µA
OSCO						
V_{OH}	output voltage HIGH	I_{OH} = −0.2 mA	V_{DD}−0.5	-	-	V
V_{OL}	output voltage LOW	I_{OL} = 0.3 mA	-	-	0.4	V
	output leakage current	T_{amb} = 25 °C		-		-
I_{LO}		V_O = 5.5 V; V_{DD} = 5.5 V		-		-
I_{LO}		V_O = 0 V; V_{DD} = 5.5 V				
SDO						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	-	-	0.4	V
I_{LO}	output leakage current	V_O = 5.5 V; T_{amb} = 25 °C; V_{DD} = 25 °C	-	-	1	µA
Oscillator						
f_{OSCI}	maximum oscillator frequency	V_{DD} = 4.75 V; see Fig.6	500	-	-	kHz

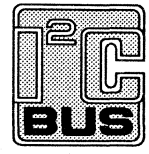


Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	March 1991

SAA4700
VPS dataline processor



FEATURES

- Adaptive sync slicer with buffered composite sync output VCS
- Adaptive data slicer
- Data rate clock regenerator
- Field selection and line 16 decoding
- Startcode and biphase check
- Data valid output
- Storage of data line information in a 40 bit register bank
- I²C-bus transmission

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pins 15 and 16)	4.5	5	5.5	V
I_P	total supply current	-	18	23	mA
$V_{i\ CVBS}$	CVBS input signal sync-to-white (peak-to-peak value)	0.5	1	1.4	V
T_{amb}	operating ambient temperature	0	-	+70	°C

GENERAL DESCRIPTION

The SAA4700 is a bipolar integrated circuit designed for use in dataline receivers and incorporates a dataline slicer and decoder. The slicer extracts the dataline signal from the video signal and regenerates the data clock. It also provides signals for the decoder in order to decode the binary data that is transmitted in line 16 of every first field of the composite video signal (video programming signal and video recording programming by Teletext, VPS and VPT systems). The decoded information out of words 5 and 11 to 14 is accessed via the built-in I²C-bus interface. This information then can be used for programming a video cassette recorder in order to start and stop a recording of a television program at the correct aligned time, regardless of a delay or extension in the transmission time of the required program.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA4700	18	DIL	plastic	SOT102

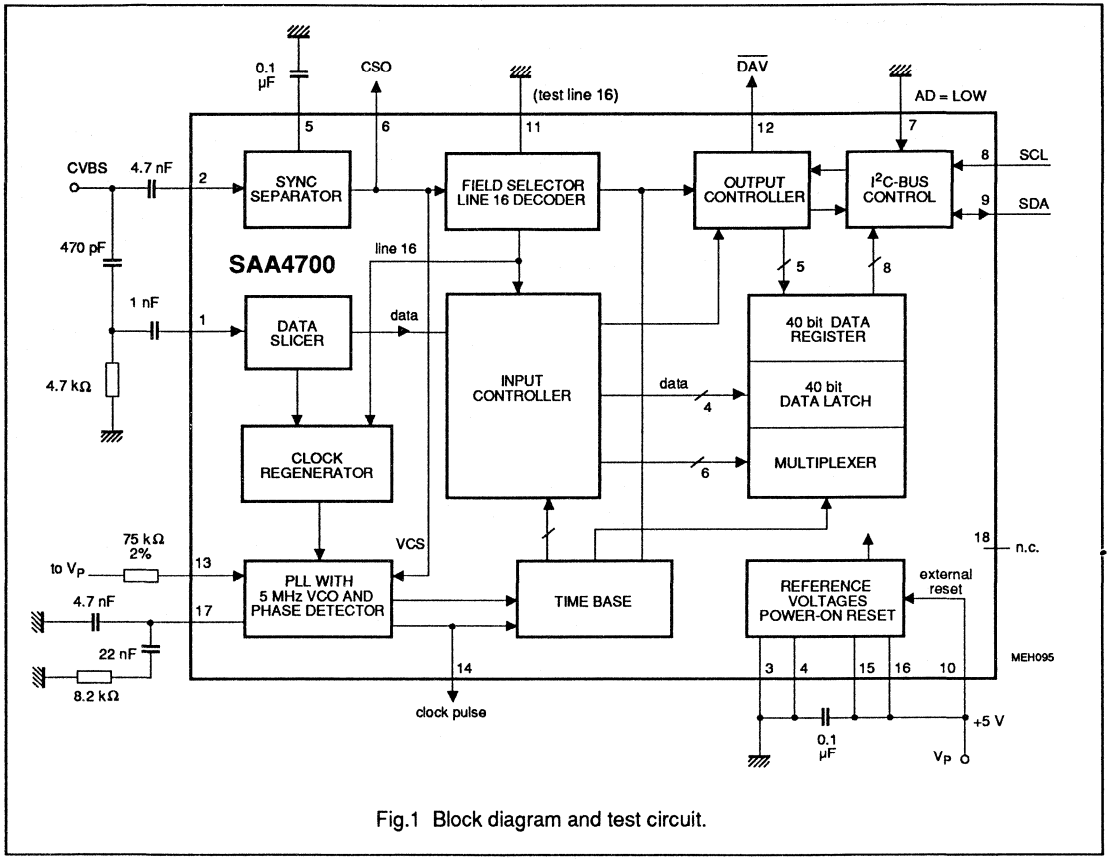


Fig.1 Block diagram and test circuit.

FUNCTIONAL DESCRIPTION

Dataline 16

The information in dataline 16 consists of fifteen 8-bit words; the total information content is shown in Table 1; and the organization of transmitted bytes is shown in Table 2.

Out of the fifteen possible 8-bit words the SAA4700 extracts words 5 and 11 to 14. The contents of these words can be read via the built-in I²C-bus interface. The circuit is fully transparent, thus each bit is transferred without modification with only the sequence of words being changed. Words 11 to 14 are transmitted first followed by word 5.

By evaluating the sliced sync signal the circuit can identify the beginning of dataline 16 in the first field. The dataline decoder stage releases the start code detector. When a correct start code is detected (for timing of start code detection see Fig.3) words 5 and 11 to 14 are decoded, checked for biphase errors and stored in a register bank. If no biphase error has occured, the contents of the register bank are transferred to a second register bank by the data valid control signal. If the system has been addressed, this transfer will be delayed until the next start or stop condition of the I²C-bus has been received.

The last bit of correct information on the dataline remains available until it is read via the I²C-bus. Once the stored information has been read it is considered to be no longer valid and the internal new data flag is reset. Subsequently, if the circuit is addressed, the only VPS data that will be sent back is "FFF to F". The same conditions apply after power-up when no data can be read out. New data is available after reception of another error-free dataline 16.

VPS dataline processor SAA4700

PINNING

SYMBOL	PIN	DESCRIPTION
CVBS	1	video signal input (CVBS from TV)
SYNC	2	sync amplitude input (CVBS from TV)
GND1	3	analog ground (0 V)
GND2	4	digital ground (0 V)
C_{black}	5	capacitor for black level
CSO	6	composite sync output
AD	7	address set input
SCL	8	I²C-bus clock line
SDA	9	I²C-bus data line
$\overline{RS}$	10	reset input active LOW
TP	11	test point for line 16 decoder
$\overline{DAV}$	12	data available output active LOW
R_{osc}	13	oscillator resistor for frequency adjustment
CP	14	test point clock pulse
V_{P1}	15	+5 V supply voltage (digital part)
V_{P2}	16	+5 V supply voltage (analog part)
C_{ph}	17	capacitor of phase detector
n.c.	18	not connected

PIN CONFIGURATION

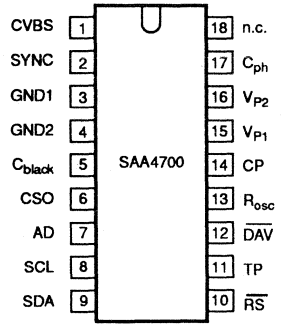


Fig.2 Pin configuration.

External reset
The circuit provides an internal power-on reset. When using this facility pin 10 should be connected to V_P or, if external reset (RESET = LOW) is to be used pin 10 should be prepared by connecting pin 10 via a 10 kΩ pull-up resistor to V_P.

Reset forces the following:

- I²C-bus not to acknowledge
- $\overline{DAV}$ output to go HIGH (pin 12)
- I²C-bus transfer register to "FFF"

CVBS input
The CVBS signal is applied to the sync separator (pin 2) via a decoupling capacitor and to the data slicer (pin1) via an RC high-pass filter. To enable proper storage of the sync value in the decoupling capacitor, the sync generator output resistance should not exceed 1 kΩ.

Black level
The capacitor connected to pin 5 stores the black level value for the adaptive sync slicer.

Composite sync output (CSO)
A composite sync output signal for customer application is provided (pin 6).

$\overline{DAV}$ output
The data available output pin 12 is set LOW after an error free dataline 16 is received. $\overline{DAV}$ returnes to HIGH after the beginning of the next first field. If no valid data is available $\overline{DAV}$ remains HIGH. A short duration pulse of 1 µs (Fig.5) is inserted at the beginning of dataline 16; it will ensure that a HIGH-to-LOW transmission occurs which can then be used for triggering.

5 MHz VCO and phase detector
The resistor connected between pin 13 and V_{P2} determines the current into the voltage controlled oscillator. The RC network connected to pin 17 acts as a low-pass filter for the phase detector.

Power supply
To prevent crosscoupling the circuit is provided with separate ground and supply pins for analog and digital parts (pins 3, 4, 15 and 16).

Table 1 Information per word in dataline 16

word number	content
1	run in
2	start code
3	program source identification (binary coded)
4	program source identification (ASCII sequential)
5	sound and VTR control information
6	program/test picture identification
7	internal information exchange
8	) address assignment of signal distribution
9	)
10	messages/commands
11	)
12	) VTR control / information
13	)
14	)
15	reserve

Table 2 VTR control information of dataline 16

	VTR control information					
Word number	5		11	12	13	14
Bit number	1 8 XXXXXXXX		0 7 XXXXXXXX	8 15 XXXXXXXX	16 23 XXXXXXXX	24 31 XXXXXXXX

	Word 5	AD (1)	Day	Month	Hour	Minute	Nation	Progr. source
Label binary		AD (1)	Day	Month	Hour	Minute	Nation	Progr. source
			Special system code					
System status code		1 X 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1					NC.. .NC	PC...PC
Pause code		1 X 0 0 0 0 0 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1					NC.. .NC	PC...PC
Interrupt code		1 X 0 0 0 0 0 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1					NC.. .NC	PC...PC

Word 5:

Bit1	Bit2	Status
0	0	2-channel
0	1	Mono
1	0	Stereo
1	1	2-channel

Bit3	Bit4	Status
1	0	free
0	1	free

(1) address range; NC = nation code; PC = program source code; X = 0 or 1 (bit)

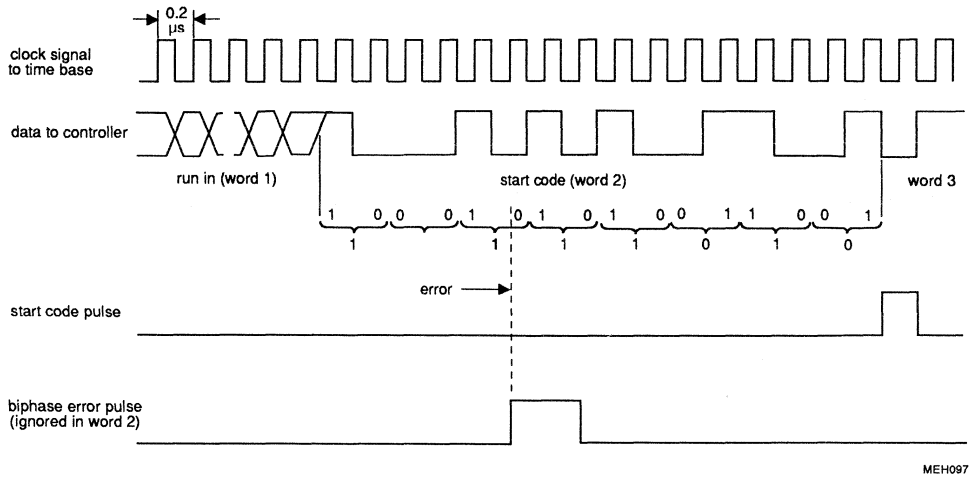


Fig.3 Timing diagram of start code detection.

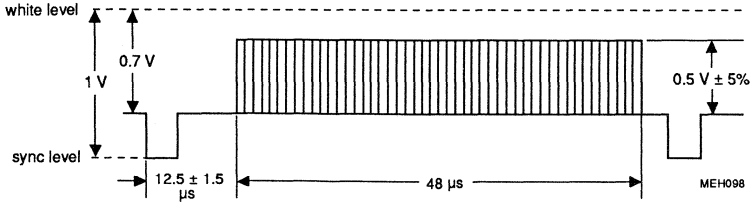


Fig.4 Timing diagram of dataline 16; modulation depth 71.4%.

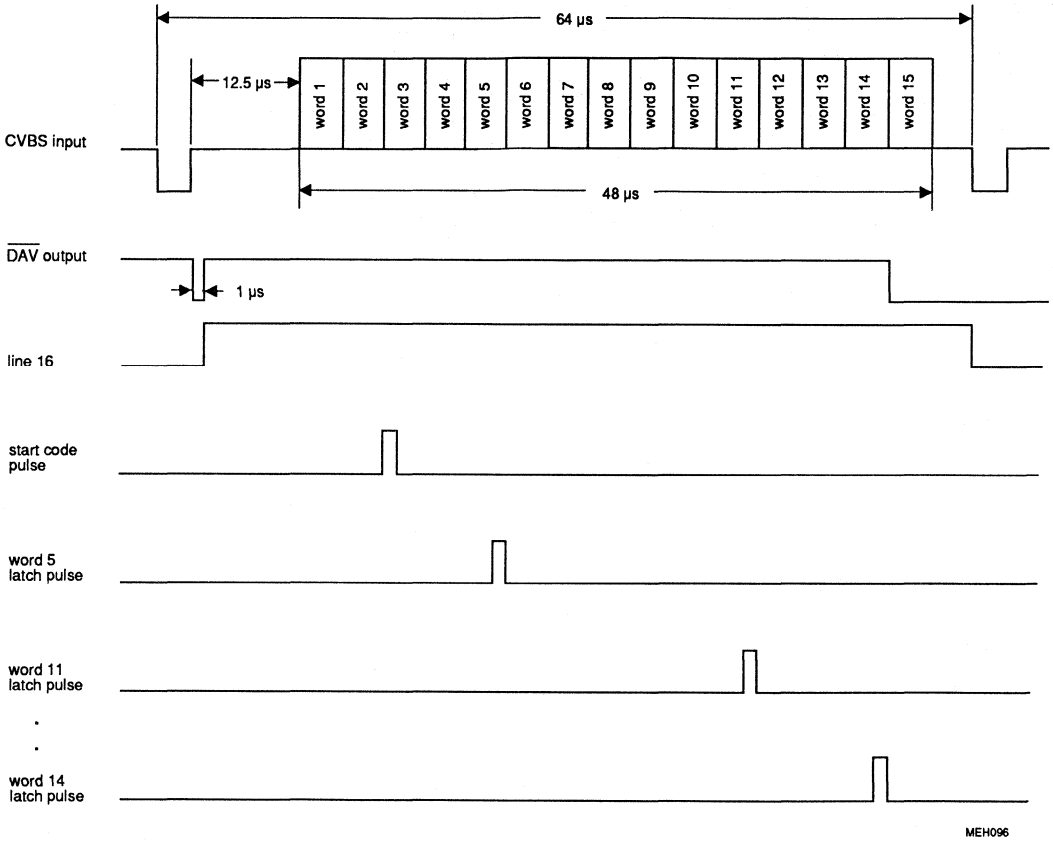


Fig.5 Timing diagram of the data available output and word latch pulses.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Ground pins 3 and 4 as well as supply pins 15 and 16 tied together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 15)	−0.5	6.0	V
V_{P2}	supply voltage (pin 16)	−0.5	6.0	V
T_{stg}	storage temperature range	−20	125	°C
T_{amb}	operating ambient temperature range	0	+70	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	-	78	K/W

CHARACTERISTICS

$V_{P1} = V_{P2} = 5$ V; $T_{amb} = 25$ °C; CVBS signal according to VPS and VPT standard and measurements taken in Fig.1, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}, V_{P2}	supply voltages (pins 15 and 16)		4.5	5	5.5	V
I_P	total supply current	$I_{15} + I_{16}$	-	18	23	mA
CVBS and sync inputs (pins 1 and 2)						
$V_{i\ CVBS}$	CVBS input signal (peak-to-peak value)	sync-to-white note 1; Fig.4	0.5	1	1.4	V
$V_{i\ data}$	data input signal (peak-to-peak value, pin 1)	line 16; Fig.4	250	500	700	mV
$V_{i\ sync}$	sync input signal (peak-to-peak value, pin 2)		100	-	600	mV
R_S	source resistance		-	-	1	kΩ
Composite sync output (pin 6)						
V_{OL}	output voltage LOW		-	-	0.4	V
V_{OH}	output voltage HIGH		2.4	-	-	V
I_{OL}	output current LOW		-	-	200	µA
I_{OH}	output current HIGH		-	-	−500	µA
t_d	sync separator delay time		-	0.3	-	µs
$\overline{\text{DAV}}$ **output** (pin 12)		note 2				
V_{OL}	output voltage LOW		-	-	0.4	V
V_{OH}	output voltage HIGH		2.4	-	-	V
I_{OL}	output current LOW		-	-	500	µA
I_{OH}	output current HIGH		-	0.01	1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCL and SDA (pins 8 and 9)						
V_{IL}	input voltage LOW		-	-	1.5	V
V_{IH}	input voltage HIGH		3	-	-	V
I_I	input current	$0.9V_P$	-	-	±10	µA
C_I	input capacitance		-	-	10	pF
$V_{O\ ACK}$	output voltage during acknowledge on pin 9	I_{OL} = 3 mA	-	-	0.4	V
t_r	rise time		-	-	1	µs
t_f	fall time		-	-	0.3	µs
$t_{p\ L}$	pulse duration LOW		4.7	-	-	µs
$t_{p\ H}$	pulse duration HIGH		4.0	-	-	µs
SCL	clock frequency		-	-	100	kHz
AD set input (pin 7)		note 2				
V_{IL}	input voltage LOW	address 23H	0	-	0.4	V
V_{IH}	input voltage HIGH	address 21H	2.4	-	V_P	V
RESET input (pin 10)		note 2				
V_{IL}	input voltage LOW	reset active	-	-	0.4	V
V_{IH}	input voltage HIGH	reset non-active	2.4	-	-	V
I_{IL}	input current LOW		-	-	−10	µA
I_{IH}	input current HIGH		-	0.01	1	µA

Notes to the characteristics

1. With standard sync and data amplitude of 68% to 75% black-white.
2. If the open collector output $\overline{DAV}$ is used, a pull-up resistor to V_{P1} is necessary.

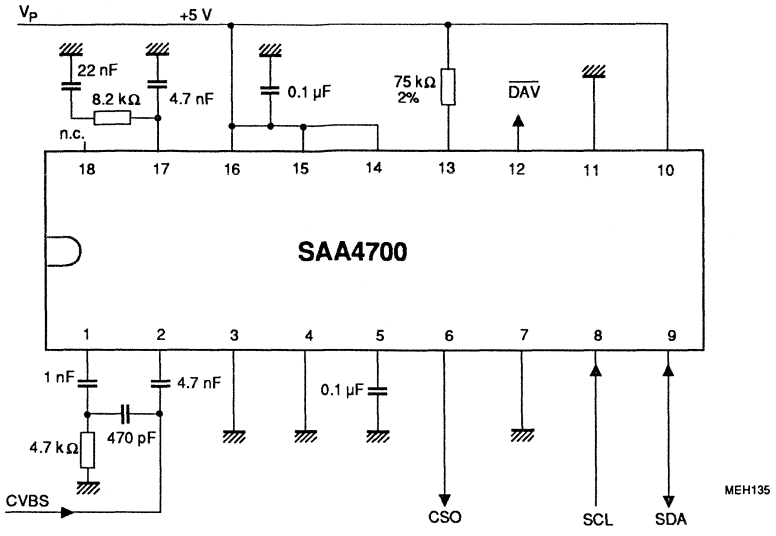


Fig.6 Application circuit.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	DATA	A	DATA	A	DATA	A	DATA	A	DATA	P

S	=	start condition
SLAVE ADDRESS	=	**0010 0001 or 0010 0011** for set input AD = HIGH respectively LOW on pin 7 (the circuit is only a slave transmitter)
A	=	acknowledge, generated by the slave or the master
DATA	=	five data bytes, see words in Table 1
P	=	stop condition respectivily non-acknowledge by the microcontroller

Remarks to I²C-bus transmission
- the MSB of each word is transmitted first
- there is no restriction on the number of words to be transmitted, but if more than five words are requested, the following content will be "FF" continuously.
- Normally every dataline transmission has to be ended with STOP condition by non-acknowledge of the controller.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	March 1991

SAA4700T
VPS dataline processor

FEATURES

- Adaptive sync slicer with buffered composite sync output VCS
- Adaptive data slicer
- Data rate clock regenerator
- Field selection and line 16 decoding
- Startcode and biphase check
- Data valid output
- Storage of data line information in a 40 bit register bank
- I²C-bus transmission

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pins 17 and 18)	4.5	5	5.5	V
I_P	total supply current	-	18	23	mA
$V_{i\ CVBS}$	CVBS input signal sync-to-white (peak-to-peak value)	0.5	1	1.4	V
T_{amb}	operating ambient temperature	0	-	+70	°C

GENERAL DESCRIPTION

The SAA4700T is a bipolar integrated circuit designed for use in dataline receivers and incorporates a dataline slicer and decoder. The slicer extracts the dataline signal from the video signal and regenerates the data clock. It also provides signals for the decoder in order to decode the binary data that is transmitted in line 16 of every first field of the composite video signal (video programming signal and video recording programming by Teletext, VPS and VPT systems). The decoded information out of words 5 and 11 to 14 is accessed via the built-in I²C-bus interface. This information then can be used for programming a video cassette recorder in order to start and stop a recording of a television program at the correct aligned time, regardless of a delay or extension in the transmission time of the required program.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA4700T	20	mini-pack	plastic	SOT163A

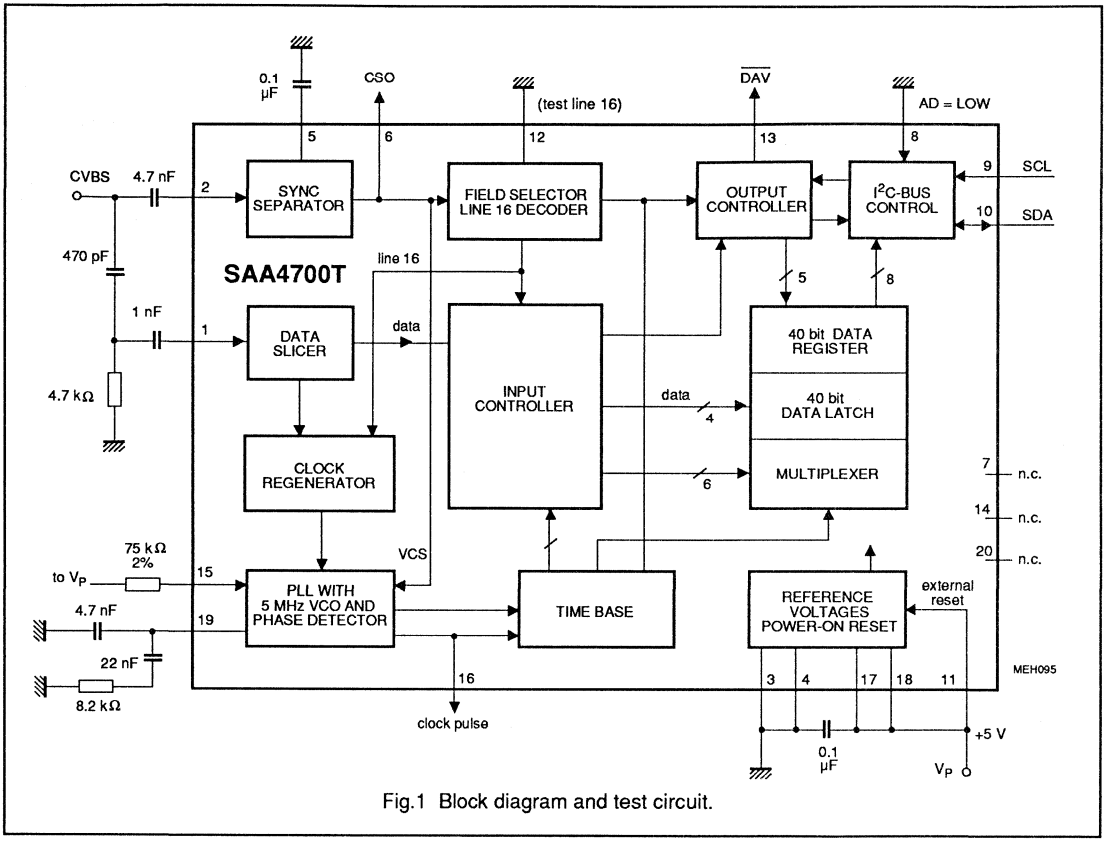


Fig.1 Block diagram and test circuit.

FUNCTIONAL DESCRIPTION

Dataline 16

The information in dataline 16 consists of fifteen 8-bit words; the total information content is shown in Table 1; and the organization of transmitted bytes is shown in Table 2.

Out of the fifteen possible 8-bit words the SAA4700T extracts words 5 and 11 to 14. The contents of these words can be read via the built-in I²C-bus interface. The circuit is fully transparent, thus each bit is transferred without modification with only the sequence of words being changed. Words 11 to 14 are transmitted first followed by word 5.

By evaluating the sliced sync signal the circuit can identify the beginning of dataline 16 in the first field. The dataline decoder stage releases the start code detector. When a correct start code is detected (for timing of start code detection see Fig.3) words 5 and 11 to 14 are decoded, checked for biphase errors and stored in a register bank. If no biphase error has occured, the contents of the register bank are transferred to a second register bank by the data valid control signal. If the system has been addressed, this transfer will be delayed until the next start or stop condition of the I²C-bus has been received.

The last bit of correct information on the dataline remains available until it is read via the I²C-bus. Once the stored information has been read it is considered to be no longer valid and the internal new data flag is reset. Subsequently, if the circuit is addressed, the only VPS data that will be sent back is "FFF to F". The same conditions apply after power-up when no data can be read out. New data is available after reception of another error-free dataline 16.

VPS dataline processor SAA4700T

PINNING

SYMBOL	PIN	DESCRIPTION
CVBS	1	video signal input (CVBS from TV)
SYNC	2	sync amplitude input (CVBS from TV)
GND1	3	analog ground (0 V)
GND2	4	digital ground (0 V)
C_{black}	5	capacitor for black level
CSO	6	composite sync output
n.c.	7	not connected
AD	8	address set input
SCL	9	I²C-bus clock line
SDA	10	I²C-bus data line
$\overline{RS}$	11	reset input active LOW
TP	12	test point for line 16 decoder
$\overline{DAV}$	13	data available output active LOW
n.c.	14	not connected
R_{osc}	15	oscillator resistor for frequency adjustment
CP	16	test point clock pulse
V_{P1}	17	+5 V supply voltage (digital part)
V_{P2}	18	+5 V supply voltage (analog part)
C_{ph}	19	capacitor of phase detector
n.c.	20	not connected

PIN CONFIGURATION

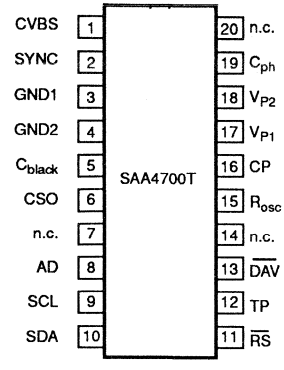


Fig.2 Pin configuration.

External reset
The circuit provides an internal power-on reset. When using this facility pin 11 should be connected to V_P or, if external reset (RESET = LOW) is to be used pin 11 should be prepared by connecting pin 11 via a 10 kΩ pull-up resistor to V_P.

Reset forces the following:

- I²C-bus not to acknowledge
- $\overline{DAV}$ output to go HIGH (pin 13)
- I²C-bus transfer register to "FFF"

CVBS input
The CVBS signal is applied to the sync separator (pin 2) via a decoupling capacitor and to the data slicer (pin1) via an RC high-pass filter. To enable proper storage of the sync value in the decoupling capacitor, the sync generator output resistance should not exceed 1 kΩ.

Black level
The capacitor connected to pin 5 stores the black level value for the adaptive sync slicer.

Composite sync output (CSO)
A composite sync output signal for customer application is provided (pin 6).

$\overline{DAV}$ output
The data available output pin 13 is set LOW after an error free data line 16 is received. $\overline{DAV}$ returnes to HIGH after the beginning of the next first field. If no valid data is available $\overline{DAV}$ remains HIGH.
A short duration pulse of 1 µs (Fig.5) is inserted at the beginning of dataline 16; it will ensure that a HIGH-to-LOW transmission occurs which can then be used for triggering.

5 MHz VCO and phase detector
The resistor connected between pin 15 and V_{P2} determines the current into the voltage controlled oscillator. The RC network connected to pin 19 acts as a low-pass filter for the phase detector.

Power supply
To prevent crosscoupling the circuit is provided with separate ground and supply pins for analog and digital parts (pins 3, 4, 17 and 18).

Table 1 Information per word in dataline 16

word number	content
1	run in
2	start code
3	program source identification (binary coded)
4	program source identification (ASCII sequential)
5	<u>sound and VTR control information</u>
6	program/test picture identification
7	internal information exchange
8	) address assignment of signal distribution
9	)
10	messages/commands
11	)
12	) <u>VTR control / information</u>
13	)
14	)
15	reserve

Table 2 VTR control information of dataline 16

	VTR control information							
Word number	5	11		12		13		14
Bit number	1 8 XXXXXXXX	0 7 XXXXXXXX		8 15 XXXXXXXX		16 23 XXXXXXXX		24 31 XXXXXXXX
Label binary	Word 5: <u>Bit1 Bit2</u> | <u>Status</u> 0 0 | 2-channel 0 1 | Mono 1 0 | Stereo 1 1 | 2-channel <u>Bit3 Bit4</u> | <u>Status</u> 1 0 | free 0 1 | free	AD (1)	Day	Month	Hour	Minute	Nation	Progr. source
			Special system code					
System status code		1 X 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1					NC.. .NC	PC...PC
Pause code		1 X 0 0 0 0 0 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1					NC.. .NC	PC...PC
Interrupt code		1 X 0 0 0 0 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1					NC.. .NC	PC...PC

(1) address range; NC = nation code; PC = program source code; X = 0 or 1 (bit)

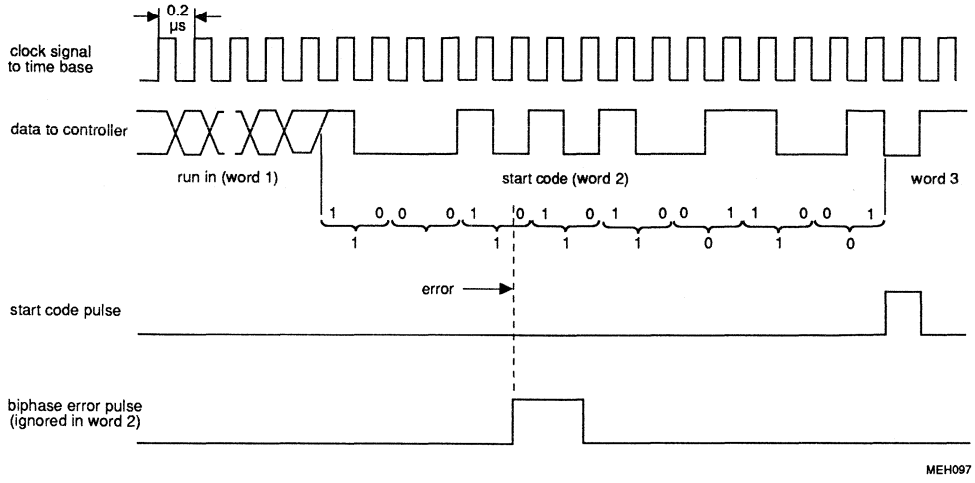


Fig.3 Timing diagram of start code detection.

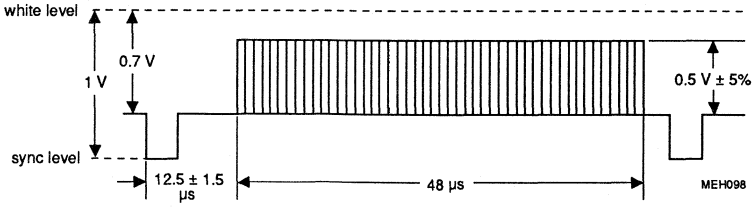


Fig.4 Timing diagram of dataline 16; modulation depth 71.4%.

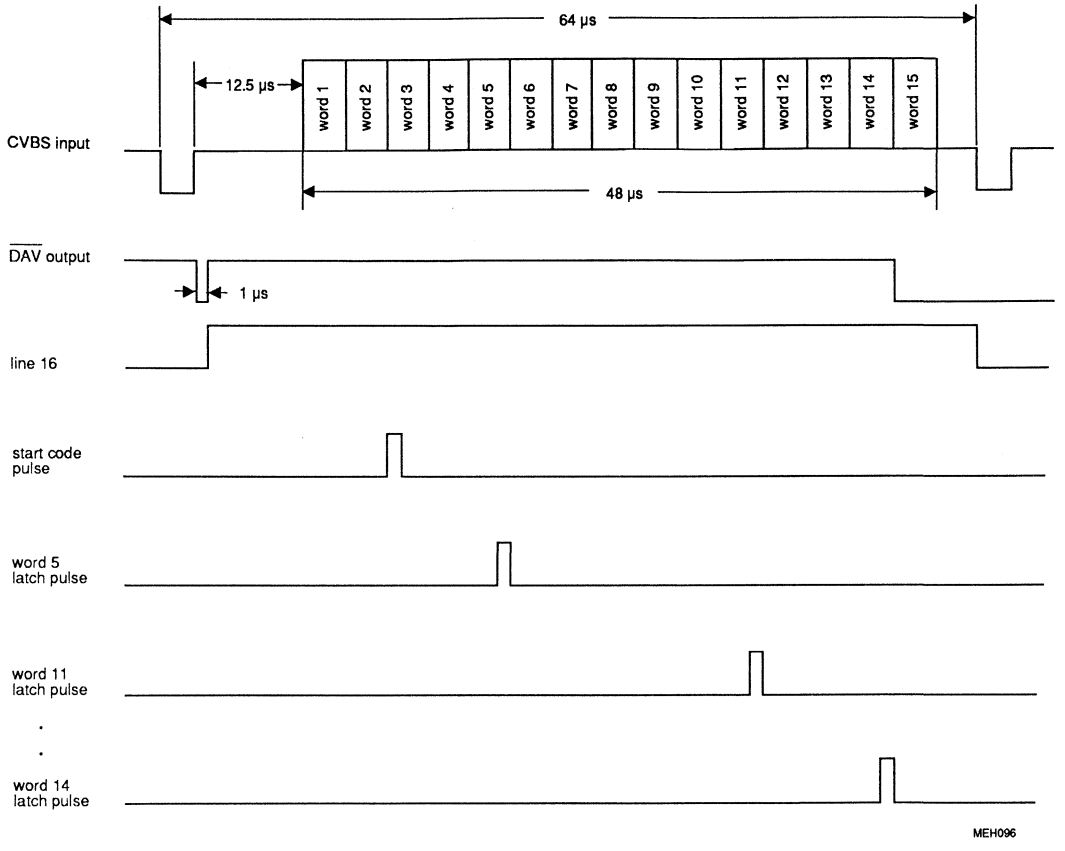


Fig.5 Timing diagram of the data available output and word latch pulses.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Ground pins 3 and 4 as well as supply pins 17 and 18 tied together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 17)	−0.5	6.0	V
V_{P2}	supply voltage (pin 18)	−0.5	6.0	V
T_{stg}	storage temperature range	−20	125	°C
T_{amb}	operating ambient temperature range	0	+70	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	-	130	K/W

CHARACTERISTICS

$V_{P1} = V_{P2} = 5$ V; $T_{amb} = 25$ °C; CVBS signal according to VPS and VPT standard and measurements taken in Fig.1, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}, V_{P2}	supply voltages (pins 17 and 18)		4.5	5	5.5	V
I_P	total supply current	$I_{17} + I_{18}$	-	18	23	mA
CVBS and sync inputs (pins 1 and 2)						
$V_{i\ CVBS}$	CVBS input signal (peak-to-peak value)	sync-to-white note 1; Fig.4	0.5	1	1.4	V
$V_{i\ data}$	data input signal (peak-to-peak value, pin 1)	line 16; Fig.4	250	500	700	mV
$V_{i\ sync}$	sync input signal (peak-to-peak value, pin 2)		100	-	600	mV
R_S	source resistance		-	-	1	kΩ
Composite sync output (pin 6)						
V_{OL}	output voltage LOW		-	-	0.4	V
V_{OH}	output voltage HIGH		2.4	-	-	V
I_{OL}	output current LOW		-	-	200	μA
I_{OH}	output current HIGH		-	-	−500	μA
t_d	sync separator delay time		-	0.3	-	μs
$\overline{\text{DAV}}$ **output** (pin 13)		note 2				
V_{OL}	output voltage LOW		-	-	0.4	V
V_{OH}	output voltage HIGH		2.4	-	-	V
I_{OL}	output current LOW		-	-	500	μA
I_{OH}	output current HIGH		-	0.01	1	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCL and SDA (pins 9 and 10)						
V_{IL}	input voltage LOW		-	-	1.5	V
V_{IH}	input voltage HIGH		3	-	-	V
I_I	input current	$0.9V_P$	-	-	±10	µA
C_I	input capacitance		-	-	10	pF
$V_{O\ ACK}$	output voltage during acknowledge on pin 10	I_{OL} = 3 mA	-	-	0.4	V
t_r	rise time		-	-	1	µs
t_f	fall time		-	-	0.3	µs
$t_{p\,L}$	pulse duration LOW		4.7	-	-	µs
$t_{p\,H}$	pulse duration HIGH		4.0	-	-	µs
SCL	clock frequency		-	-	100	kHz
AD set input (pin 8)		note 2				
V_{IL}	input voltage LOW	address 23H	0	-	0.4	V
V_{IH}	input voltage HIGH	address 21H	2.4	-	V_P	V
RESET input (pin 11)		note 2				
V_{IL}	input voltage LOW	reset active	-	-	0.4	V
V_{IH}	input voltage HIGH	reset non-active	2.4	-	-	V
I_{IL}	input current LOW		-	-	−10	µA
I_{IH}	input current HIGH		-	0.01	1	µA

Notes to the characteristics

1. With standard sync and data amplitude of 68% to 75% black-white.
2. If the open collector output $\overline{DAV}$ is used, a pull-up resistor to V_{P1} is necessary.

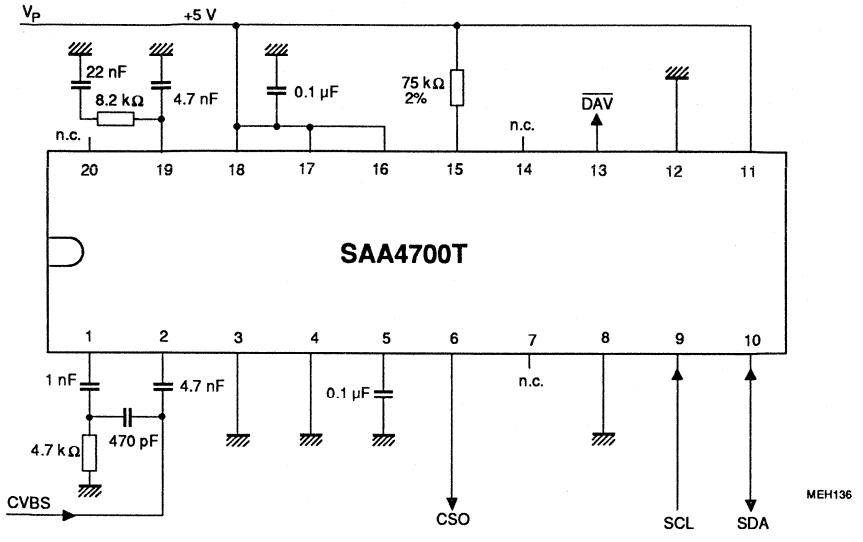


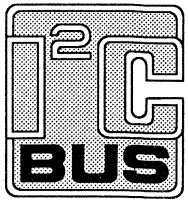
Fig.6 Application circuit.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	DATA	A	DATA	A	DATA	A	DATA	A	DATA	P

S	=	start condition
SLAVE ADDRESS	=	**0010 0001 or 0010 0011** for set input AD = HIGH respectively LOW on pin 8 (the circuit is only a slave transmitter)
A	=	acknowledge, generated by the slave or the master
DATA	=	five data bytes, see words in Table 1
P	=	stop condition respectivily non-acknowledge by the microcontroller

Remarks to I²C-bus transmission
- the MSB of each word is transmitted first
- there is no restriction on the number of words to be transmitted, but if more than five words are requested, the following content will be "FF" continuously.
- Normally every dataline transmission has to be ended with STOP condition by non-acknowledge of the controller.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	March 1991

SAA5191
Teletext video processor

FEATURES

- Adaptive data slicer
- Crystal-controlled data clock regeneration with a bit rate of 6.9375 MHz
- Adaptive sync separator, horizontal phase detector and 13.5 MHz VCO to provide display phase locked loop (PLL)
- TV synchronization at teletext mode

GENERAL DESCRIPTION

The SAA5191 is a bipolar integrated circuit that extracts teletext data from the video signal (CVBS), regenerates the teletext clock (TTC) and synchronizes the text display to the television signals (VCS). This device operates in conjunction with the Digital Video Teletext (back-end) Decoder (DVTB – SAA9042A) or any other compatible device.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 16)	-	12	-	V
I_P	supply current	-	70	-	mA
$V_{i\ CVBS}$	CVBS input signal on pin 27 (peak-to-peak value)				
	at pin 2 LOW	-	1	-	V
	at pin 2 open-circuit	-	2.5	-	V
V_o	output signals TTC and TTD (peak-to-peak value, pins 14, 15)	2.5	3.5	4.5	V
V_{F13}	13.5 MHz clock output signal (peak-to-peak value, pin 17)	1	2	3	V
V_{SYNC}	video sync output signal (peak-to-peak value, pin 1)	-	-	1	V
	SYNC output signal $\overline{TCS}$	200	450	650	mV
VCS	video composite sync level on output pin 25				
	LOW	-	-	0.4	V
	HIGH	2.4	-	5.5	V
T_{amb}	operating ambient temperature	0	-	+70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5191	28	DIL	plastic	SOT117

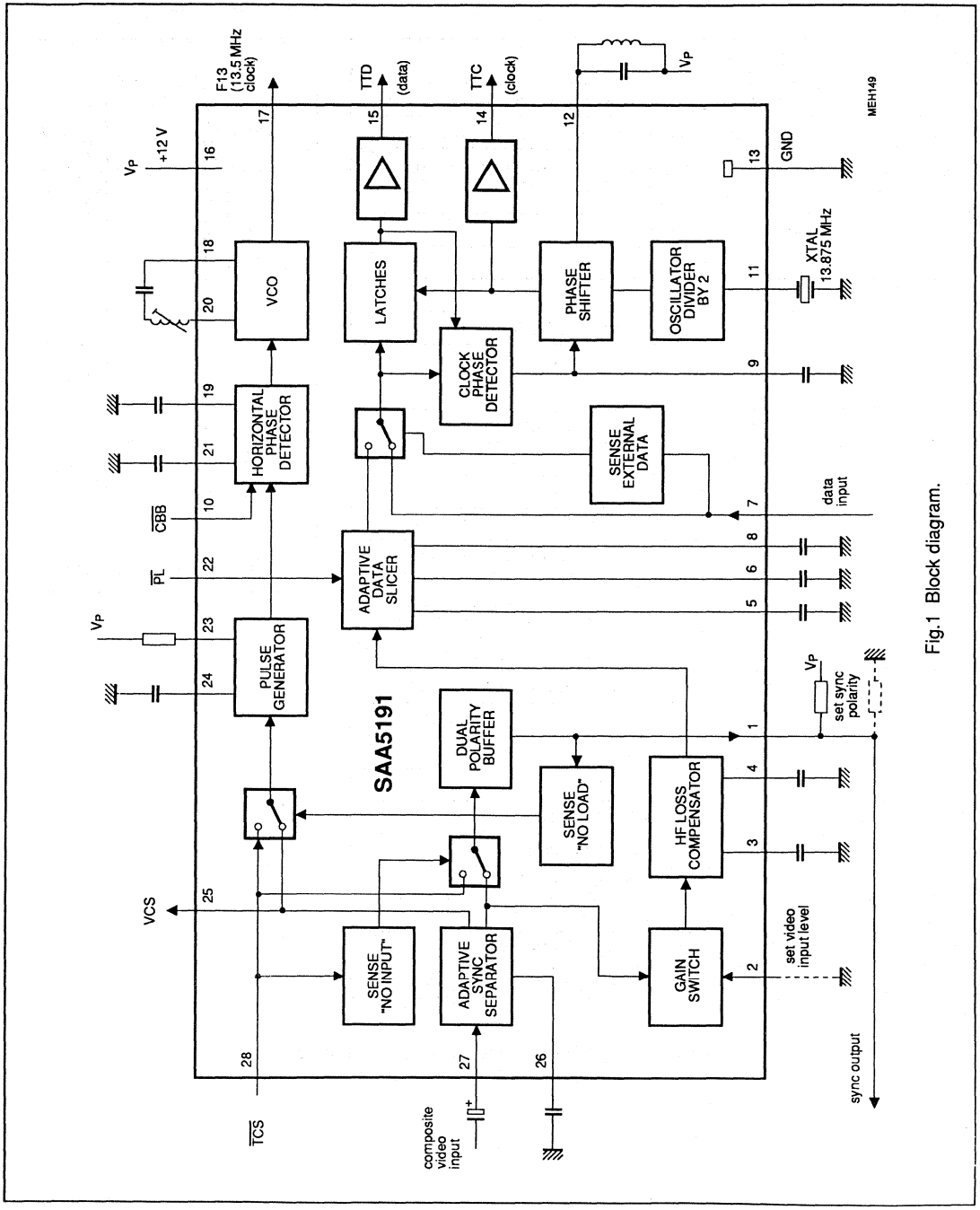


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
STTV	1	sync output signal to TV (positive or negative going)
VILS	2	level select input of video input (LOW equals 1 V)
C_{filt}	3	video filtering capacitor of HF loss compensation
C_{store}	4	HF storage capacitor
C_{ampl}	5	amplitude capacitor
C_{zero}	6	zero level capacitor
EXD	7	external data current input (1)
C_{time}	8	data timing capacitor for the adaptive data slicer
C_{CLK}	9	clock phase detector capacitor
$\overline{CBB}$	10	blanking insertion input
XTAL	11	13.875 MHz crystal (double of data rate)
CLF	12	6.9375 MHz clock frequency filter
GND	13	ground (0 V)
TTC	14	teletext clock output (for computer controlled teletext)
TTD	15	teletext data output (for computer controlled teletext)
V_P	16	+12 V supply voltage
F13	17	13.5 MHz VCO output (for sandcastle generation)
OSCO	18	oscillator output to series LC-circuit or crystal
C_{VCR}	19	short time constant capacitor at video recorder mode (2)
OSCI	20	oscillator input from series LC-circuit or crystal
C_{hor}	21	horizontal phase capacitor / VCR mode
$\overline{PL}$	22	sandcastle input (generated in CCT)
R_T	23	timing resistor for pulse generator
C_T	24	timing capacitor for pulse generator
VCS	25	video composite sync output to CCT
C_{BL}	26	black level capacitor
CVBS	27	composite video input signal from TV
$\overline{TCS}$	28	text-composite/scan-composite sync input ($\overline{TSC}$/$\overline{SCS}$)

PIN CONFIGURATION

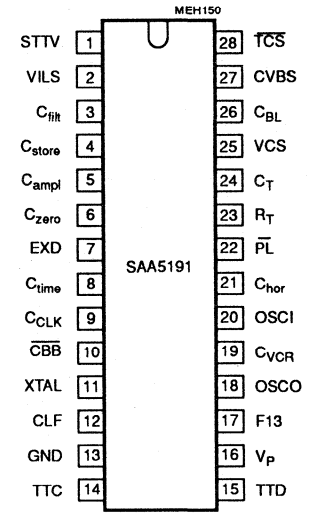


Fig.2 Pin configuration.

Notes to the pinning

(1) Sliced teletext data from external: active HIGH level (current), low impedance input.
(2) While the loop is locking up.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

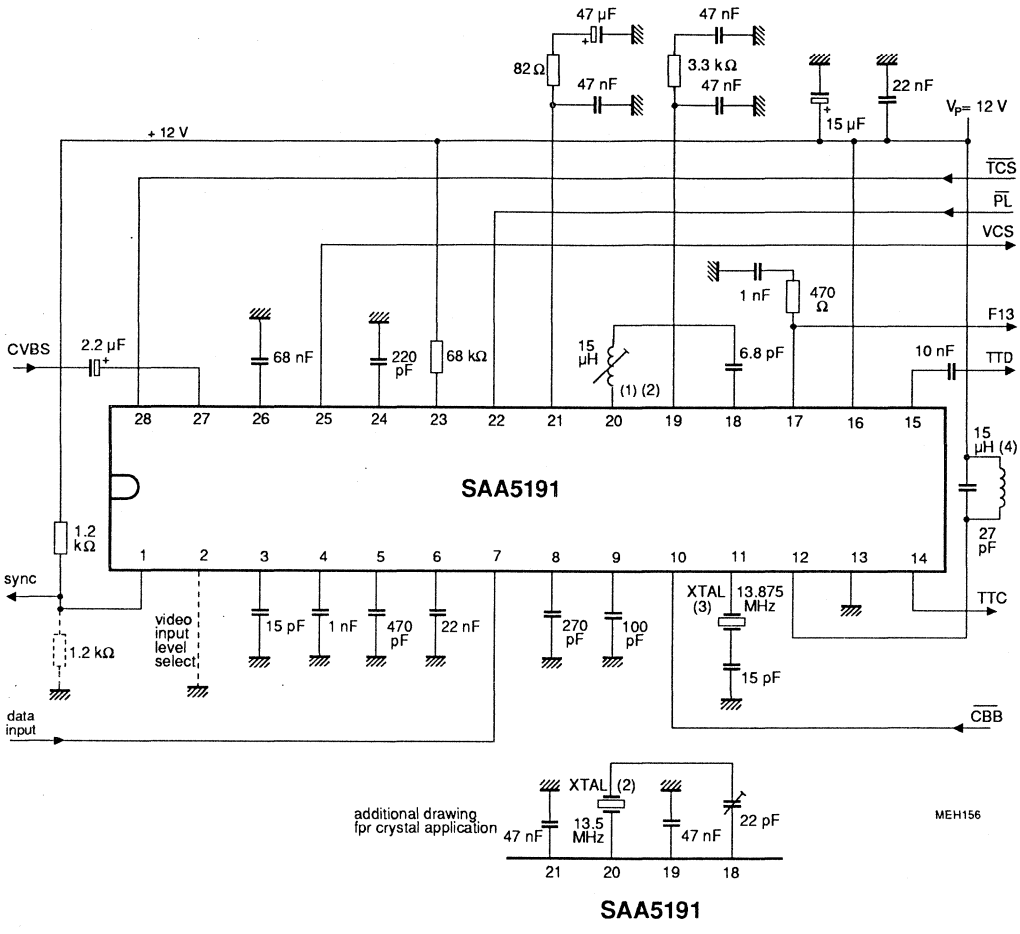
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 16)	0	13.2	V
V_5	voltage on pin 5	0	5.5	V
T_{stg}	storage temperature range	−20	125	°C
T_{amb}	operating ambient temperature range	0	+70	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C and measurements taken in Fig.3, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 16)		10.8	12.0	13.2	V
I_P	supply current		50	70	105	mA
Video input, sync separator and data slicer		$Z_S \leq 250\ \Omega$				
$V_{i\ CVBS}$	input signal sync to white (peak-to-peak value, pin 27)	V_2 = LOW	0.7	1	1.4	V
		V_2 = HIGH	1.75	2.5	3.5	V
	sync amplitude (peak-to-peak value)		0.1	-	1	V
	data slicing level	V_2 = LOW	0.3	0.46	0.7	V
		V_2 = HIGH	0.75	1.15	1.75	V
V_2	input voltage LOW (pin 2)		0	-	0.8	V
	input voltage HIGH	open-circuit equals HIGH	2.0	-	5.5	V
I_2	input current LOW		0	-	−150	µA
	input current HIGH	V_2 < 5.5 V	0	-	1	mA
Teletext data output (TTD)						
V_{22}	phase lock pulse (PL) input voltage (peak-to-peak value, pin 22)	phase locked	0	-	3	V
		phase unlocked	3.9	-	5.5	V
$V_{o\ TTD}$	data output signal on pin 15 (peak-to-peak value)		2.5	3.5	4.5	V
V_{15}	DC output voltage	mean level	3	4	5	V
C_L	load capacitance on pin 15		-	-	40	pF
t_r, t_f	rise and fall time		20	30	45	ns
Teletext clock output (TTC)						
$V_{o\ TTC}$	clock output signal on pin 14 (peak-to-peak value)		2.5	3.5	4.5	V
V_{14}	DC output voltage	mean level	3	4	5	V
C_L	load capacitance on pin 14		-	-	40	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r, t_f	rise and fall time		20	30	45	ns
t_d	delay time of falling edge relative to other edges of TTD		-	-	±20	ns
Text/ scan composite sync input ($\overline{TCS}$/$\overline{SCS}$)						
V_{28}	input voltage LOW for $\overline{TCS}$ (pin 28)		0	-	0.8	V
	input voltage HIGH for $\overline{TSC}$		2.0	-	7.0	V
	input voltage LOW for $\overline{SCS}$		0	-	1.5	V
	input voltage HIGH for $\overline{SCS}$		3.5	-	7.0	V
I_{28}	input current	V_{28} = 0 to 7 V	–40	–70	–100	µA
		V_{28} = 10 to V_P	-	-	±5	µA
SYNC output buffer						
V_o	CVBS sync output signal on pin 1 (peak-to-peak value)	$R_{L\,1}$ = 1.2 kΩ to V_P	-	-	1	V
	$\overline{TCS}$ output signal	$R_{L\,1}$ = 1.2 kΩ to GND	200	450	650	mV
V_1	DC output voltage at positive sync signal	$R_{L\,1}$ = 1.2 kΩ to GND	1.0	1.4	2.0	V
	DC output voltage at negative sync signal	$R_{L\,1}$ = 1.2 kΩ to V_P	9.0	10.1	11.0	V
I_1	output current		-	-	±3	mA
Video composite sync output (VCS)						
V_{25}	output voltage LOW (pin 25)		0	-	0.4	V
	output voltage HIGH		2.4	-	5.5	V
I_{25}	output current LOW		0	-	0.5	mA
	output current HIGH		0	-	–1.5	mA
t_d	sync separator delay time		250	350	400	ns
Horizontal phase detector and 13.5 MHz VCO						
V_{10}	input voltage LOW ($\overline{CBB}$), pin 10	blanking inserted	0	-	0.5	V
	blanking insertion HIGH	no blanking	1.0	-	5.5	V
I_{10}	input current		-	-	–5	µA
V_o	13.5 MHz clock output signal (peak-to-peak value, pin 17)		1	2	3	V
V_{17}	DC output voltage	maximum swing	4	-	8.5	V
C_L	load capacitance on pin 17		-	-	40	pF
t_r, t_f	rise and fall time		10	-	30	ns



(1) inductance 15 µH at 1 kHz, C_o = 2.2 pF. Adjust free-running frequency to 13.5 ± 0.1 MHz or apply 13.5 MHz quarz crystal as shown in additional drawing

(2) Crystal: f = 13.5 MHz (e.g. Philips catalogue number 4322 143 04101); adjustment tolerance $\pm 40 \cdot 10^{-6}$; load capacitance C_L = 22 pF; resonance resistance R_r = 22 pF; typical motional capacitance C_1 = 23 fF; static parallel capacitance C_o = 5.5 pF; frequency tolerance $\pm 30 \cdot 10^{-6}$ in temperature range T = −20 to +70°. Adjust free-running frequency to 13.5 ± 0.5 MHz.

(3) Crystal: f = 13.875 MHz; adjustment tolerance $\pm 40 \cdot 10^{-6}$; load capacitance C_L = 15 pF; typical resonance resistance R_r = 15 Ω (maximum 60 Ω); typical motional capacitance C_1 = 19 fF; static parallel capacitance C_o = 5 pF; frequency tolerance $\pm 30 \cdot 10^{-6}$ in temperature range T = −20 to +70°.

(4) Coil: Fixed inductance 15 µH ±20%, quality factor Q > 20.

Fig.3 Test circuit and application circuit using LC-circuit or a crystal for VCO (clock F13).

TELETEXT VIDEO PROCESSOR

GENERAL DESCRIPTION

The SAA5231 is a bipolar integrated circuit intended as a successor to the SAA5030. It extracts Teletext Data from the video signal, regenerates Teletext Clock and synchronizes the text display to the television syncs. The integrated circuit is intended to work in conjunction with CCT (Computer Controlled Teletext), EUROM or other compatible devices.

Features

- Adaptive data slicer
- Data clock regenerator
- Adaptive sync separator, horizontal phase detector and 6 MHz VCO forming display phase locked loop (PLL)

QUICK REFERENCE DATA

Supply voltage (pin 16)	V_{CC}	typ.	12 V
Supply current (pin 16)	I_{CC}	typ.	70 mA
Video input amplitude (pin 27) (peak-to-peak value)			
pin 2 LOW	$V_{27\text{-}13(p\text{-}p)}$	typ.	1 V
pin 2 HIGH	$V_{27\text{-}13(p\text{-}p)}$	typ.	2,5 V
Storage temperature range	T_{stg}		−20 to + 125 °C
Operating ambient temperature range	T_{amb}		0 to + 70 °C

PACKAGE OUTLINE

28-lead dual in-line; plastic (SOT117).

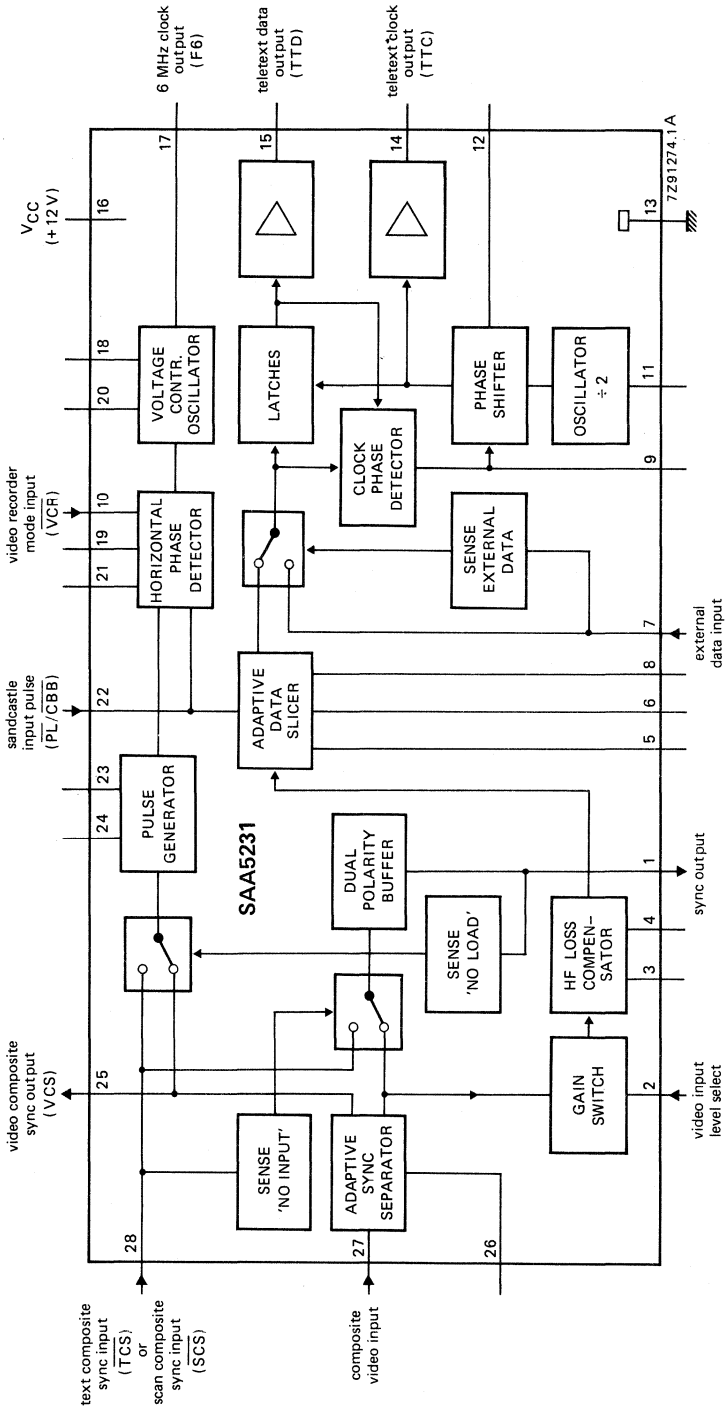


Fig. 1 Block diagram.

PINNING

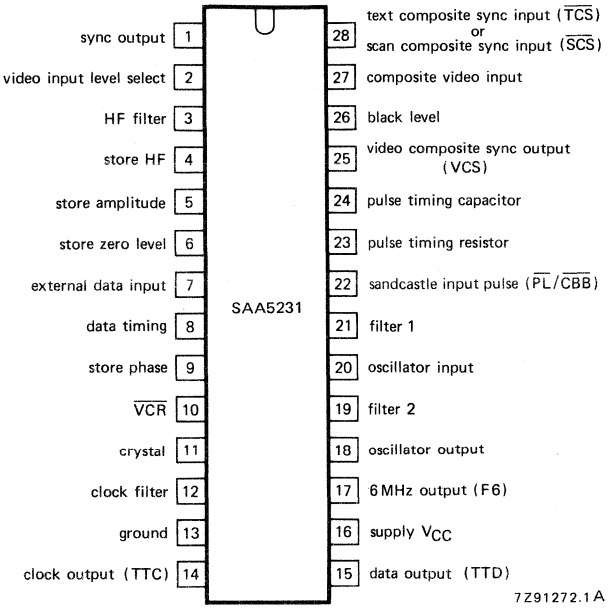


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 16)	V_{CC}	max. 13,2 V
Storage temperature range	T_{stg}	−20 to + 125 °C
Operating ambient temperature	T_{amb}	0 to + 70 °C

CHARACTERISTICS

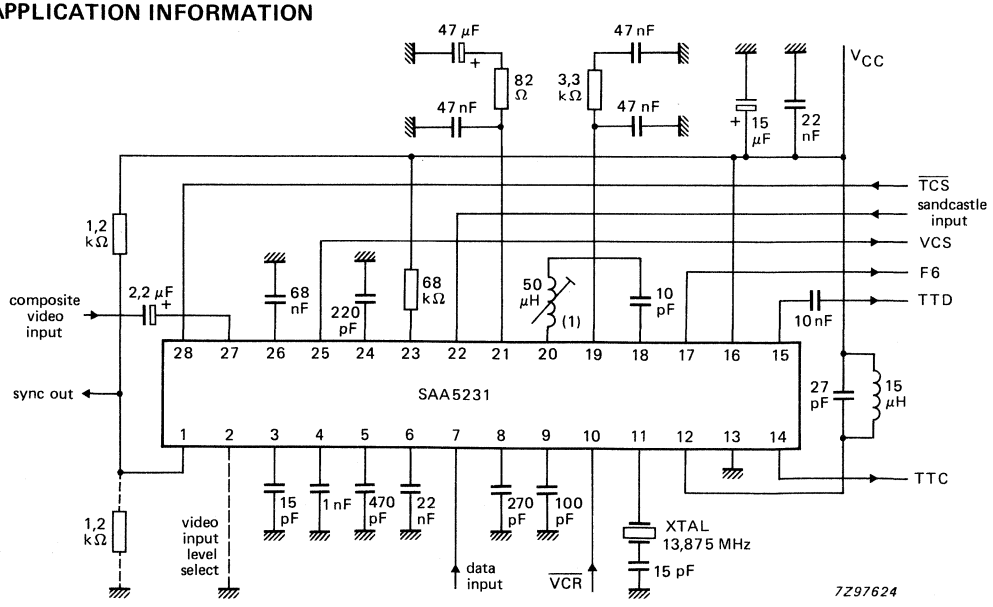
V_{CC} = 12 V; T_{amb} = 25 °C with external components as shown in application circuits unless otherwise stated.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 16)					
Supply voltage	V_{CC}	10,8	12,0	13,2	V
Supply current	I_{CC}	50	70	105	mA
Video input and sync separator					
Video input amplitude (sync to white) (peak-to-peak value)					
video input select level LOW (pin 2)	$V_{27\text{-}13(p\text{-}p)}$	0,7	1	1,4	V
video input select level HIGH (pin 2)	$V_{27\text{-}13(p\text{-}p)}$	1,75	2,5	3,5	V
Source impedance	$\lvert Z_s \rvert$	–	–	250	Ω
Sync amplitude (peak-to-peak value)	$V_{27\text{-}13(p\text{-}p)}$	0,1	–	1	V
Video input level select					
Input voltage LOW	$V_{2\text{-}13}$	0	–	0,8	V
Input voltage HIGH	$V_{2\text{-}13}$	2,0	–	5,5	V
Input current LOW	I_2	0	–	−150	μA
Input current HIGH	I_2	0	–	1	mA
Text composite sync input ($\overline{TCS}$)					
Input voltage LOW	$V_{28\text{-}13}$	0	–	0,8	V
Input voltage HIGH	$V_{28\text{-}13}$	2,0	–	7,0	V
Scan composite sync input ($\overline{SCS}$)					
Input voltage LOW	$V_{28\text{-}13}$	0	–	1,5	V
Input voltage HIGH	$V_{28\text{-}13}$	3,5	–	7,0	V
Select video sync from pin 1					
Input current (pin 28)					
at V_{28} = 0 to 7 V	I_{28}	−40	−70	−100	μA
at V_{28} = 10 V to V_{CC}	I_{28}	−5	–	+ 5	μA
Video composite sync output (VCS)					
Output voltage LOW	$V_{25\text{-}13}$	0	–	0,4	V
Output voltage HIGH	$V_{25\text{-}13}$	2,4	–	5,5	V
D.C. output current LOW	I_{25}	–	–	0,5	mA
D.C. output current HIGH	I_{25}	–	–	−1,5	mA
Sync separator delay time	t_d	0,25	0,35	0,40	μs

parameter	symbol	min.	typ.	max.	unit
Dual polarity buffer output					
$\overline{TCS}$ amplitude (peak-to-peak value)	$V_{1\text{-}13(p\text{-}p)}$	0,20	0,45	0,65	V
Video sync amplitude (peak-to-peak value)	$V_{1\text{-}13(p\text{-}p)}$	–	–	1	V
Output current	I_1	−3	–	+ 3	mA
D.C. output voltage					
R_L to ground (0 V)	$V_{1\text{-}13}$	1,0	1,4	2,0	V
R_L to V_{CC} (12 V)	$V_{1\text{-}13}$	9,0	10,1	11,0	V
Sandcastle input pulse ($\overline{PL}/\overline{CBB}$)					
Phase lock pulse (PL)					
PL on (LOW)	$V_{22\text{-}13}$	0	–	3	V
PL off (HIGH)	$V_{22\text{-}13}$	3,9	–	5,5	V
Blanking pulse (CBB)					
CBB on (LOW)	$V_{22\text{-}13}$	0	–	0,5	V
CBB off (HIGH)	$V_{22\text{-}13}$	1,0	–	5,5	V
Input current	I_{22}	−10	–	+ 10	μA
Phase locked loop (PLL)					
Phase detector timing					
Pulse duration using composite video	t_p	2,0	2,4	2,8	μs
using scan composite sync	t_p	3,0	3,5	4,0	μs
time PL must be LOW to make VCO run-free	t_L	100	–	–	μs
6 MHz clock output (F6)					
A.C. output voltage (peak-to-peak value)	$V_{17\text{-}13(p\text{-}p)}$	1	2	3	V
A.C. and d.c. output voltage range	$V_{17\text{-}13(max)}$	4	–	8,5	V
Rise and fall time	$t_r; t_f$	20	–	40	ns
Load capacitance	$C_{17\text{-}13}$	–	–	40	pF
Video recorder mode input ($\overline{VCR}$)					
VCR-mode on (LOW)	$V_{10\text{-}13}$	0	–	0,8	V
VCR-mode off (HIGH)	$V_{10\text{-}13}$	2,0	–	V_{CC}	V
Input current	I_{10}	−10	–	+ 10	μA

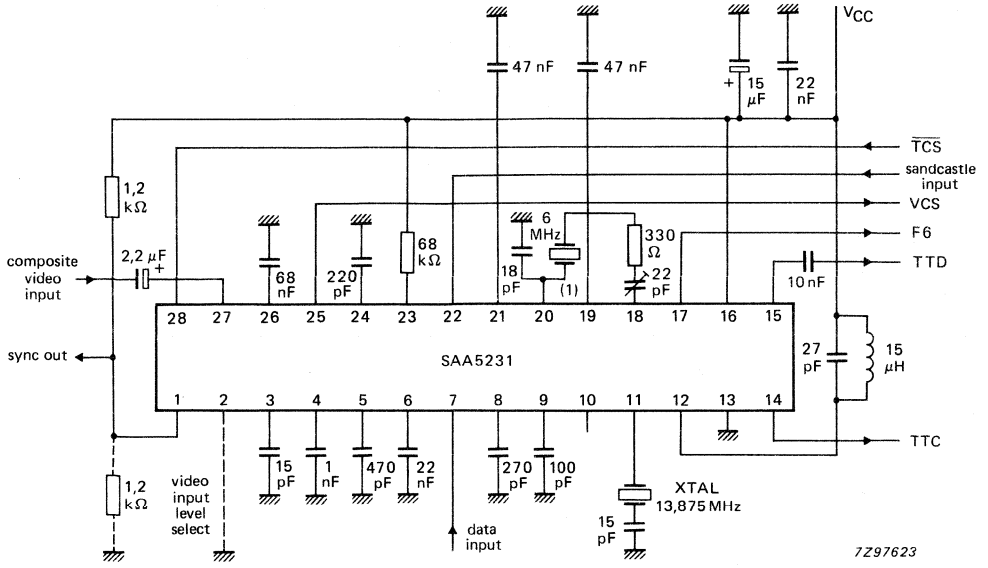
parameter	symbol	min.	typ.	max.	unit
Data slicer					
Data amplitude of video input (pin 27)					
video input level select LOW (pin 2)	V_{27-13}	0,30	0,46	0,70	V
video input level select HIGH (pin 2)	V_{27-13}	0,75	1,15	1,75	V
Teletext clock output					
A.C. output voltage (peak-to-peak value)	$V_{14-13(p-p)}$	2,5	3,5	4,5	V
D.C. output voltage (centre)	V_{14-13}	3,0	4,0	5,0	V
Load capacitance	C_L	–	–	40	pF
Rise and fall times	t_r; t_f	20	30	45	ns
Delay of falling edge relative to other edges of TTD	t_d	–20	0	+ 20	ns
Teletext data output					
A.C. output voltage (peak-to-peak value)	$V_{15-13(p-p)}$	2,5	3,5	4,5	V
D.C. output voltage (centre)	V_{15-13}	3,0	4,0	5,0	V
Load capacitance	C_L	–	–	40	pF
Rise and fall times	t_r; t_f	20	30	45	ns

APPLICATION INFORMATION



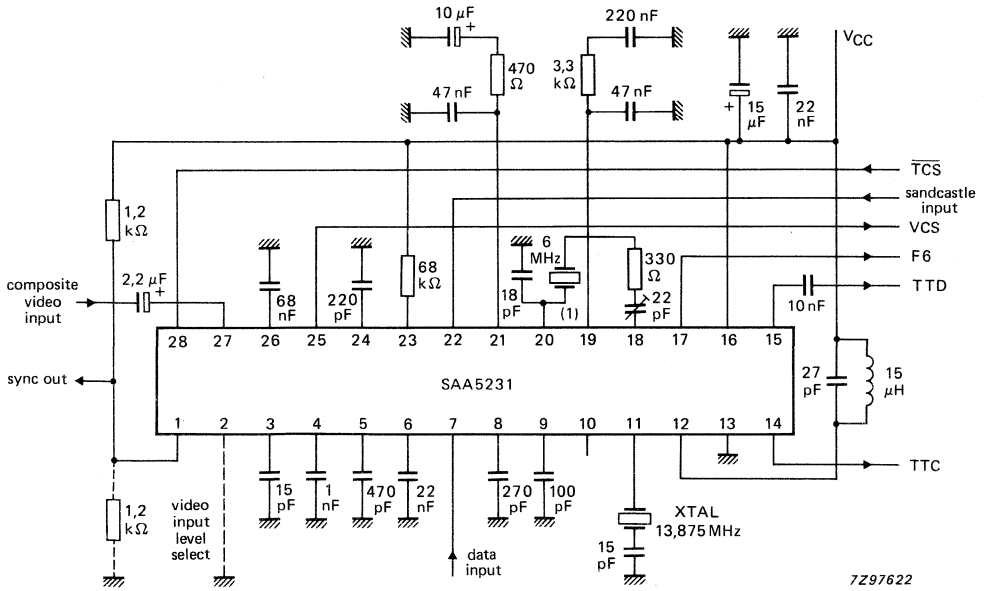
(1) Coil: 50 µH at 1 kHz, C_o = 4 pF. Adjust the free-running frequency to 6000 kHz ± 30 kHz.

Fig. 3a Application circuit using L/C circuit in PLL.



(1) Quartz crystal e.g. catalogue number 4322 143 04101. Adjust the free-running frequency to 6000,2 kHz ± 0,2 kHz.

Fig. 3b Application circuit using quartz crystal in PLL.



(1) Ceramic resonator e.g. Kyocera KBR 6,0 M. Adjust the free-running frequency to 6010 kHz ± 5 kHz.

Fig. 3c Application circuit using ceramic resonator in PLL.

Component specifications

Specifications of some external components in Figs 3a, 3b and 3c.

Quartz crystal 13,875 MHz; Figs 3a, 3b and 3c

Load resonance frequency (f) 13,875 MHz; adjustment tolerance $\pm 40 \cdot 10^{-6}$

Load capacitance (C_L) 20 pF

Temperature range (T) −20 to +70 °C; frequency tolerance maximum $\pm 30 \cdot 10^{-6}$

Resonance resistance (R_r) typical 10 Ω maximum 60 Ω

Motional capacitance (C_1) typical 19 fF

Static parallel capacitance (C_o) typical 5 pF

Fixed inductance Figs 3a, 3b and 3c

Inductance (L) 15 μH ± 20%

Quality factor (Q) minimum 20

Variable inductance Fig. 3a

Inductance (L) 50 μH at 1 kHz

Static parallel capacitance (C_o) typical 4 pF

Quartz crystal Fig. 3b

Preferred type 4322 143 04101

Load resonance frequency (f) 6 MHz; adjustment tolerance $\pm 40 \cdot 10^{-6}$

Load capacitance (C_L) 20 pF

Temperature range (T) −20 to +70 °C; frequency tolerance $\pm 30 \cdot 10^{-6}$

Resonance resistance (R_r) 60 Ω

Motional capacitance (C_1) typical 28 fF

Static parallel capacitance (C_o) typical 7 pF

Ceramic resonator; Fig. 3c

Preferred type KBR 6,0 M, Kyocera

Load resonance frequency (f) 6 MHz; adjustment tolerance ± 0,5%

Load capacitance (C_L) 20 pF

Temperature range (T) −20 to +70 °C; frequency tolerance maximum ± 0,3%

Resonance resistance (R_r) typical 6 Ω

Motional capacitance (C_1) typical 9 pF

Static parallel capacitance (C_o) typical 60 pF

Ageing (10 years) f maximum ± 0,3%

The function is quoted against the corresponding pin number.

1. **Synch output to TV**

   Output with dual polarity buffer, a load resistor to 0 V or + 12 V selects positive-going or negative-going syncs.

2. **Video input level select**

   When this pin is LOW a 1 V video input level is selected. When the pin is not connected it floats HIGH selecting a 2,5 V video input level.

3. **HF filter**

   The video signal for the h.f.-loss compensator is filtered by a 15 pF capacitor connected to this pin.

4. **Store h.f.**

   The h.f. amplitude is stored by a 1 nF capacitor connected to this pin.

5. **Store amplitude**

   The amplitude for the adaptive data slicer is stored by a 470 pF capacitor connected to this pin.

6. **Store zero level**

   The zero level for the adaptive data slicer is stored by a 22 nF capacitor connected to this pin.

7. **External data input**

   Current input for sliced teletext data from external device.
   Active HIGH level (current), low impedance input.

8. **Data timing**

   A 270 pF capacitor is connected to this pin for timing of the adaptive data slicer.

9. **Store phase**

   The output signal from the clock phase detector is stored by a 100 pF capacitor connected to this pin.

10. **Video tape recorder mode ($\overline{\text{VCR}}$)**

    Signal input to command PLL into short time constant mode. Not used in application circuit Fig. 3b or Fig. 3c.

11. **Crystal**

    A 13,875 MHz crystal, 2 x data rate, connected in series with a 15 pF capacitor is applied via this pin to the oscillator and divide-by-two to provide the 6,9375 MHz clock signal.

12. **Clock filter**

    A filter for the 6,9375 MHz clock signal is connected to this pin.

13. **Ground (0 V)**

14. **Teletext clock output (TTC)**

    Clock output for CCT (Computer Controlled Teletext).

APPLICATION INFORMATION (continued)

15. **Teletext data output (TTD)**

Data output for CCT.

16. **Supply voltage V_{CC} (+ 12 V typ.)**

17. **Clock output (F6)**

6 MHz clock output for timing and sandcastle generation in CCT.

18. **Oscillator output (6 MHz)**

A series resonant circuit is connected between this pin and pin 20 to control the nominal frequency of the VCO.

19. **Filter 2**

A filter with a short time constant is connected to this pin for the horizontal phase detector. It is used in the video recorder mode and while the loop is locking up.

20. **Oscillator input (6 MHz)**

See pin 18.

21. **Filter 1**

A filter with a long time constant is connected to this pin for the horizontal phase detector.

22. **Sandcastle input pulse ($\overline{PL}/\overline{CBB}$)**

This input accepts a sandcastle waveform, which is formed from PL and CBB from the CCT. Signal timing is shown in Fig. 4.

23. **Pulse timing resistor**

The current for the pulse generator is defined by a 68 kΩ resistor connected to this pin.

24. **Pulse timing capacitor**

The timing of the pulse generator is determined by a 220 pF capacitor connected to this pin.

25. **Video composite sync output (VCS)**

This output signal is for CCT.

26. **Black level**

The black level for the adaptive sync separator is stored by a 68 nF capacitor connected to this pin.

27. **Composite video input (CVS)**

The composite video signal is input via a 2,2 μF clamping capacitor to the adaptive sync separator.

28. **Text composite sync input ($\overline{\text{TCS}}$)/Scan composite sync input ($\overline{\text{SCS}}$)**

$\overline{\text{TCS}}$ is input from CCT or $\overline{\text{SCS}}$ from external sync circuit. $\overline{\text{SCS}}$ is expected when there is no load resistor at pin 1. If pin 28 is not connected the sync output on pin 1 will be the composite video input at pin 27, internally buffered.

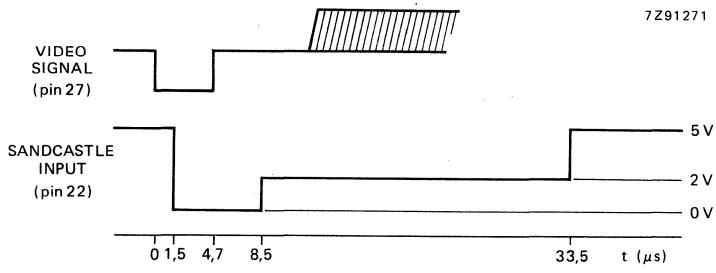


Fig. 4 Sandcastle waveform and timing.

Dual standard VPT decoder and clock calendar

SAA5232

FEATURES

- Digital data slicer
- Separate storage of VPS data (PDC System A) and packet 8/30/2 data (PCD System B) allowing dual standard VPT decoders
- I²C-bus interface with automatic word address increment
- Clock/calendar function with programmable alarm
- Programmable interrupt for data received and alarm
- Low power and low voltage clock/calendar operation
- 256 by 8-bit free static RAM
- SO24L and DIL24 packages

GENERAL DESCRIPTION

Allowing the reception and decoding of both VPS (EBU PDC System A) and packet 8/30/2 (EBU PDC System B) data, the SAA5232 is a dual standard VPS decoder intended for use in manually programmed European video recorders. It incorporates a clock calendar with programmable alarm and permits the reception of real time broadcast switching signals to allow the accurate timing of programme recording.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.5	5	5.5	V
I_{DD}	supply current		–	36	72	mA
V_{DD}bak	supply battery back-up		2	–	–	V
I_{DD}bak	supply current battery back-up	V_{DD_B} = 2 V	–	2	15	µA
V_{syn}	sync amplitude		0.1	0.3	0.6	V
V_{vid}	video amplitude		0.7	1	1.4	V
f_{vpt}	crystal frequency VPT decoder		–	27	–	MHz
f_{clk}	crystal frequency clock calendar		–	32.768	–	kHz

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5232P	24	DIL	plastic	SOT101
SAA5232T	24	mini-pack	plastic	SOT137

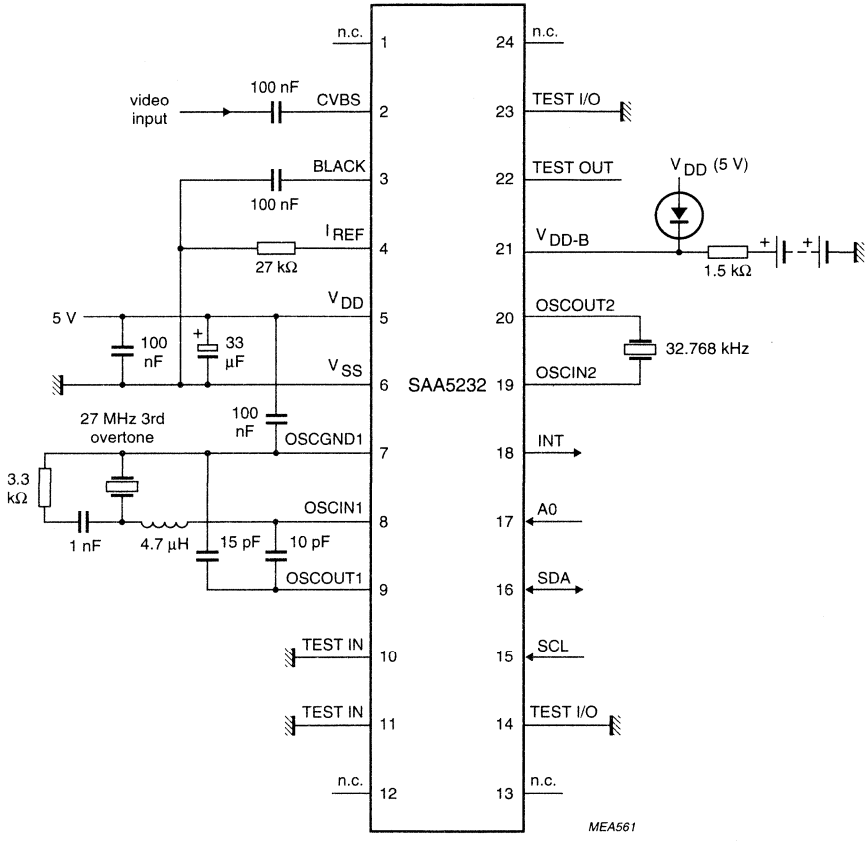


Fig.1 Application diagram.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Dual standard VPT decoder SAA5233

FEATURES

- Digital data slicer
- Separate storage of VPS data (PDC System A) and packet 8/30/2 data (PDC System B) allowing dual standard VPT decoders
- I²C-bus interface with automatic word address increment
- Programmable interrupt for data received
- Programmable error level detection
- DIL16 and SO16L packages

GENERAL DESCRIPTION

Allowing the reception and decoding of both VPS (EBU PDC System A) and packet 8/30/2 data (EBU PDC System B) data, the SAA5233 is a dual standard PDC decoder intended for use in manually programmed European video recorders. It permits the reception of real time broadcast switching signals to facilitate the accurate timing of programme recording.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5	5.5	V
I_{DD}	supply current	–	30	60	mA
f_{xtal}	crystal frequency	–	27	–	MHz
V_{syn}	sync amplitude	0.1	0.3	0.6	V
V_{vid}	video amplitude	0.7	1	1.4	V
T_{amb}	operating ambient temperature	–20	–	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5233P	16	DIL	plastic	SOT38
SAA5233T	16	mini-pack	plastic	SOT162

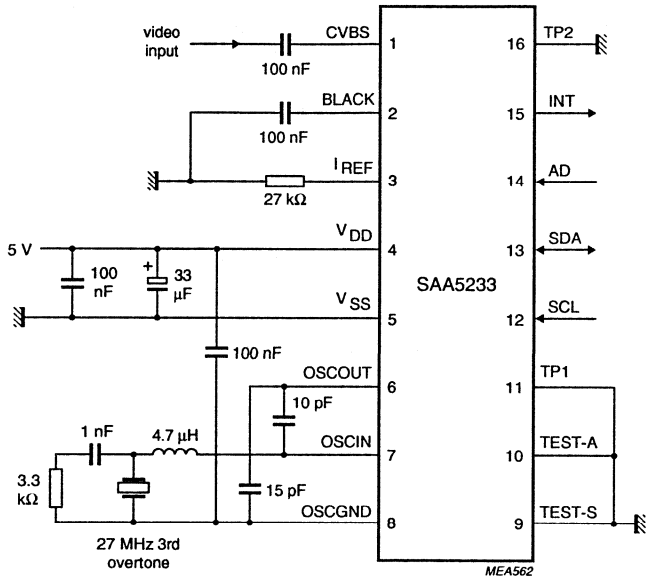


Fig.1 Application diagram.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

ENHANCED COMPUTER CONTROLLED TELETEXT CIRCUITS
(ECCT)

GENERAL DESCRIPTION

The SAA5243 series are MOS N-channel integrated circuits which perform all the digital logic functions of a 625-line World System Teletext decoder. The SAA5243 series operate in conjunction with the teletext video processor SAA5231, standard static RAMs and are controlled via the 2-wire I²C-bus. The devices can be used to provide videotex display conforming to a serial character attribute protocol.

Features

- Microcomputer controlled for flexibility
- High quality flicker-free display using a 12 x 10 character matrix
- Field flyback (lines 2 to 22), or full channel (all lines) data acquisition
- Up to four simultaneous page requests enabling acquisition during one magazine cycle
- Direct interface up to 8 K bytes static RAM
- Automatic language section of up to seven different languages
- 25th display row for software generated status messages
- Cursor control for videotex/telesoftware
- 7-bits parity or 8-bit data acquisition
- Extension packet reception option
- Standard I²C-bus slave transceiver (slave address 0010001)
- Single 5 volt power supply
- Mask programmable character sets
- Slave sync mode operation
- $\overline{\text{Odd}}$/even field output for de-interlaced displays

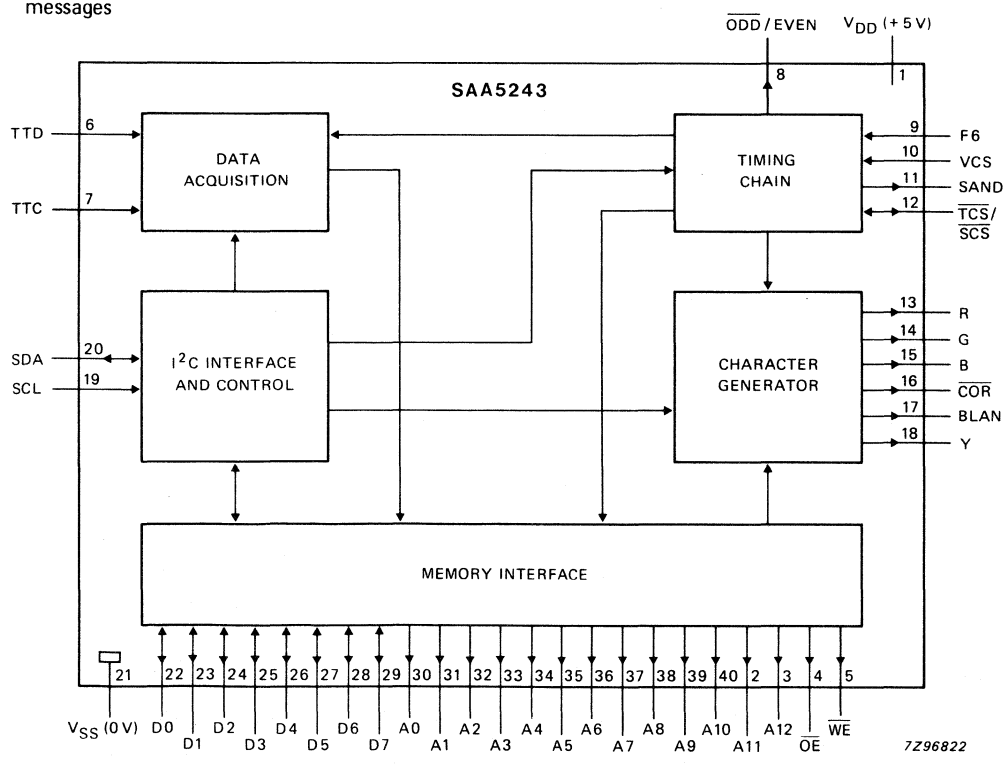


Fig.1 Block diagram.

PACKAGE OUTLINE 40-lead DIL; plastic (SOT129).

ORDERING INFORMATION

type number	version
SAA5243P/E/M2	West European languages
SAA5243P/H	East European languages
SAA5243P/K	Arabic and English languages
SAA5243P/L	Arabic and Hebrew languages
SAA5243P/T	West European and Turkish languages

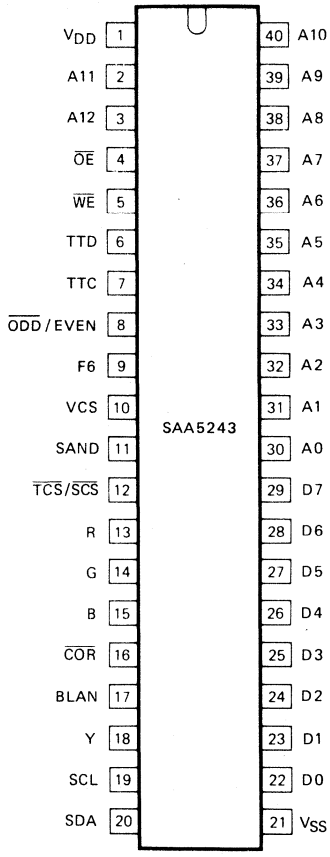


Fig.2 Pinning diagram.

PINNING

1	V_{DD}	**Power supply**: + 5 V power supply pin.
2, 3, 40	A11, A12, A10	**Chapter Address**: three outputs that select which 1 K byte chapter of external RAM is being accessed for any read or write cycle.
4	$\overline{OE}$	**Output Enable**: active low output signal used to control the reading of the external RAM. It occurs continuously at a 1 MHz rate.

5	$\overline{WE}$	**Write Enable**: active low output signal used to control the writing of data to the external RAM. It occurs for a valid write cycle only and is interleaved with the read cycles.
6	TTD	**Teletext Data**: input from the SAA5231 Video Input Processor (VIP2). It is clamped to V_{SS} for 4 to 8 μs of each television line to maintain the correct DC level following the external AC coupling.
7	TTC	**Teletext Clock**: 6.9375 MHz clock input from the SAA5231. It is internally AC coupled to an active clamp input buffer.
8	$\overline{ODD}$/EVEN	**$\overline{Odd}$/Even**: for interlaced mode, the output changes once per field at 2 μs before the end of line 311 (624). The output is high for even fields and low for odd fields.
9	F6	**Character display clock**: 6 MHz clock input from the SAA5231. It is internally AC coupled to an active clamp input buffer.
10	VCS	**Video Composite Sync**: input from the SAA5231 derived from the incoming video signal. Sync pulses are active high.
11	SAND	**Sandcastle**: 3-level sandcastle output to the SAA5231 containing the phase locking and colour burst blanking information.
12	$\overline{TCS}$/$\overline{SCS}$	**Text Composite Sync/Scan Composite Sync**: as an output an active low composite sync waveform (TCS) with interlaced or non-interlaced format (see Fig.6) which is fed to the SAA5231 to drive the display timebases. Alternatively this pin can act as an input for an active low composite sync waveform (SCS) to 'slave' the display timing circuits.
13, 14, 15	R, G, B	**Red, Green, Blue**: these 3 open drain outputs are the character video signals to the television display circuits. They are active high and contain character and background information.
16	$\overline{COR}$	**Contrast Reduction**: open drain, active low output which allows selective contrast reduction of the television picture to enhance a mixed mode display.
17	BLAN	**Blanking**: open drain, active high output which controls the blanking of the television picture for a normal text display and for a mixed display.
18	Y	**Character foreground**: open drain, active high video output signal containing all the foreground information displayed on the television screen (e.g. for driving a display printer).
19	SCL	**Serial Clock**: input signal which is the I^2C-bus clock from the microcontroller.
20	SDA	**Serial Data**: is the I^2C-bus data line. It is an input/output function with an open drain output.
21	V_{SS}	**Ground**: 0 volts.
22-29	D0-D7	**8 RAM data lines**: 3-state input/output pins which carry the data bytes to and from the external RAM.
30-39	A0-A9	**RAM address**: 10 output signals that determine which byte location within a 1 K byte chapter of external RAM is accessed for any read or write cycle.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range	pin 1	V_{DD}	−0.3	7.5	V
Input voltage range					
VCS, SDA, SCL, D0-D7		V_I	−0.3	7.5	V
TTC, TTD, F6, $\overline{TCS}/\overline{SCS}$		V_I	−0.3	10.0	V
Output voltage range					
SAND, A0-A12, $\overline{OE}$, $\overline{WE}$, D0-D7, SDA, $\overline{ODD}$/EVEN, R, G, B, BLAN, $\overline{COR}$, Y		V_O	−0.3	7.5	V
$\overline{TCS}/\overline{SCS}$		V_O	−0.3	10.0	V
Storage temperature range		T_{stg}	−20	+125	°C
Operating ambient temperature range		T_{amb}	−20	+70	°C

CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 1)	V_{DD}	4.5	5.0	5.5	V
Supply current (pin 1)	I_{DD}	–	160	270	mA
INPUTS (note 1)					
TTD (note 2)					
External coupling capacitor	C_{ext}	–	–	50	nF
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	2.0	–	7.0	V
Input data rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input data set-up time (note 4)	t_{DS}	40	–	–	ns
Input data hold time (note 4)	t_{DH}	40	–	–	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
TTC; F6 (note 5)					
DC input voltage range	V_I	−0.3	–	+ 10.0	V
AC input voltage (peak-to-peak value) F6	$V_{I(p-p)}$	1.0	–	7.0	V
AC input voltage (peak-to-peak value) TTC	$V_{I(p-p)}$	1.5	–	7.0	V
Input peaks relative to 50% duty cycle	± V_P	0.2	–	3.5	V
TTC clock frequency	f_{TTC}	–	6.9375	–	MHz
F6 clock frequency	f_{F6}	–	6.0	–	MHz
Clock rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
VCS					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 5.5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SCL					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.0	–	V_{DD}	V
SCL clock frequency	f_{SCL}	0	–	100	kHz
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5.5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
INPUT/OUTPUTS (note 6)					
$\overline{TCS}$ (output)/$\overline{SCS}$ (input)					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.5	–	10.0	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 0 to 10 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 0.4 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
at I_{OH} = 0.1 mA	V_{OH}	2.4	–	6.0	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SDA (note 7)					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5.5 V with output off	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	0	–	0.5	V
Output fall time between 3.0 V and 1.0 V levels	t_f	–	–	200	ns
Load capacitance	C_L	–	–	400	pF

parameter	symbol	min.	typ.	max.	unit
INPUT/OUTPUTS (continued)					
D0-D7 (note 8)					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD}	V
Input leakage current at V_I = 0 V to 5.5 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
OUTPUTS (note 6)					
A0-A12; $\overline{OE}$; $\overline{WE}$ (note 8)					
Output voltage LOW at I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
$\overline{ODD}$/EVEN					
Output voltage LOW at I_{OL} = 0.4 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SAND (note 9)					
Output voltage LOW at I_{OL} = 0.2 mA	V_{OL}	0	–	0.25	V
Output voltage INTERMEDIATE at I_{OL} = ± 10 μA	V_{OI}	1.1	–	3.1	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SAND (continued)					
Output voltage HIGH at I_{OH} = 0 to −10 μA	V_{OH}	4.0	–	V_{DD}	V
Output rise time V_{OL} to V_{OI} between 0.4 V and 0.9 V levels	t_{r1}	–	–	400	ns
Output rise time V_{OI} to V_{OH} between 3.3 V and 3.8 V levels	t_{r2}	–	–	200	ns
Output fall time V_{OH} to V_{OL} between 3.8 V and 0.4 V levels	t_f	–	–	50	ns
Load capacitance	C_L	–	–	30	pF
R; G; B; $\overline{\text{COR}}$; BLAN; Y (note 10)					
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	0	–	0.4	V
Output voltage LOW at I_{OL} = 5 mA	V_{OL}	0	–	1.0	V
Pull-up voltage as seen at pin	V_{PU}	–	–	6.0	V
Output fall time with a load resistor of 1.2 kΩ to 6 V and measured between 5.5 V and 1.5 V	t_f	–	–	20	ns
Skew delay between outputs with a load resistor of 1.2 kΩ to 6 V and measured on the falling edges at 3.5 V	t_{SK}	–	–	20	ns
Load capacitance	C_L	–	–	25	pF
Output leakage current at V_{PU} = 0 to 6 V with output off	I_{LO}	–	–	10	μA
TIMING					
I²C-bus (note 11)					
Clock low period	t_{LOW}	4	–	–	μs
Clock high period	t_{HIGH}	4	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	170	–	–	ns
Stop set-up time from clock high	$t_{SU;STO}$	4	–	–	μs
Start set-up time following a stop	t_{BUF}	4	–	–	μs
Start hold time	$t_{HD;STA}$	4	–	–	μs
Start set-up time following clock low-to-high transition	$t_{SU;STA}$	4	–	–	μs

parameter	symbol	min.	typ.	max.	unit
TIMING (continued)					
Memory interface (note 12)					
Cycle time	t_{CY}	–	500	–	ns
Address change to $\overline{OE}$ LOW	t_{OE}	60	–	–	ns
Address active time	t_{ADDR}	450	500	–	ns
$\overline{OE}$ pulse duration	t_{OEW}	320	–	–	ns
Access time from $\overline{OE}$ to data valid	t_{ACC}	–	–	200	ns
Data hold time from $\overline{OE}$ HIGH or address change	t_{DH}	0	–	–	ns
Address change to $\overline{WE}$ LOW	t_{WE}	40	–	–	ns
$\overline{WE}$ pulse duration	t_{WEW}	200	–	–	ns
Data set-up time to $\overline{WE}$ HIGH	t_{DS}	100	–	–	ns
Data hold time from $\overline{WE}$ HIGH	t_{DHWE}	20	–	–	ns
Write recovery time	t_{WR}	25	–	–	ns

Notes to the characteristics

1. All inputs are protected against static charge under normal handling.
2. The TTD input incorporates an internal clamping diode in addition to the active clamping transistor (see Fig.3).
3. Rise and fall times between 10% and 90% levels.
4. Teletext input data set-up and hold times are with respect to a 50% duty cycle level of the rising edge of the teletext clock input (TTC). Data stable 1 $\geqslant$ 2.0 V; data stable 0 $\leqslant$ 0.8 V (see Fig.4).
5. The TTC and F6 inputs have internal clamping diodes and are AC coupled (see Fig.3).
6. All outputs and input/outputs are protected against static charge under normal handling and connection to V_{DD} and V_{SS}.
7. For details of I^2C-bus timing see Fig.8.
8. For details of RAM timing see Fig.9.
9. For details of synchronization timing see Fig.5.
10. For details of display output timing see Fig.7.
11. The I^2C-bus timings are referred to V_{IH} = 3 V and V_{IL} = 1.5 V. For waveforms see Fig.8.
12. The memory interface timings are referred to V_{IL} = 1.5 V. For waveforms see Fig.9.

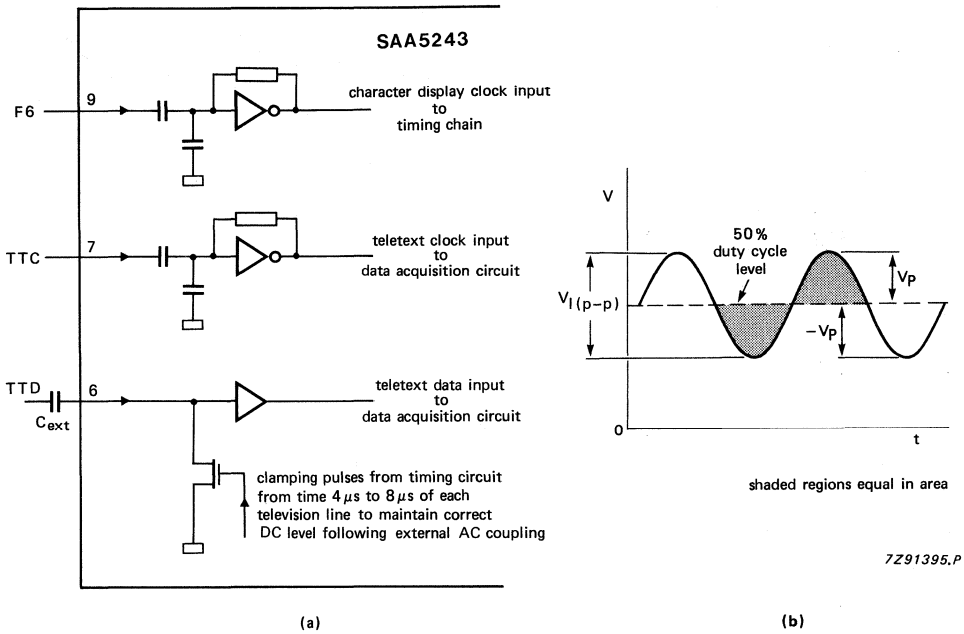
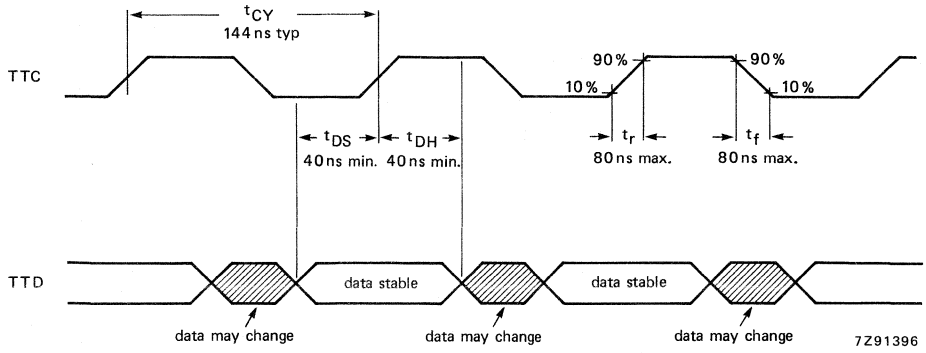


Fig.3 (a) F6, TTC and TTD input circuitry (b) input waveform parameters.



Data stable: 1 is $\geqslant$ 2.0 V; 0 is $\leqslant$ 0.8 V.

Fig.4 Teletext data input timing.

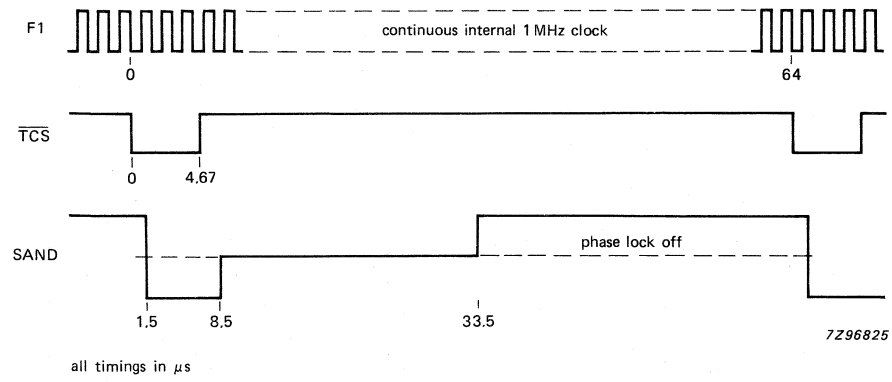
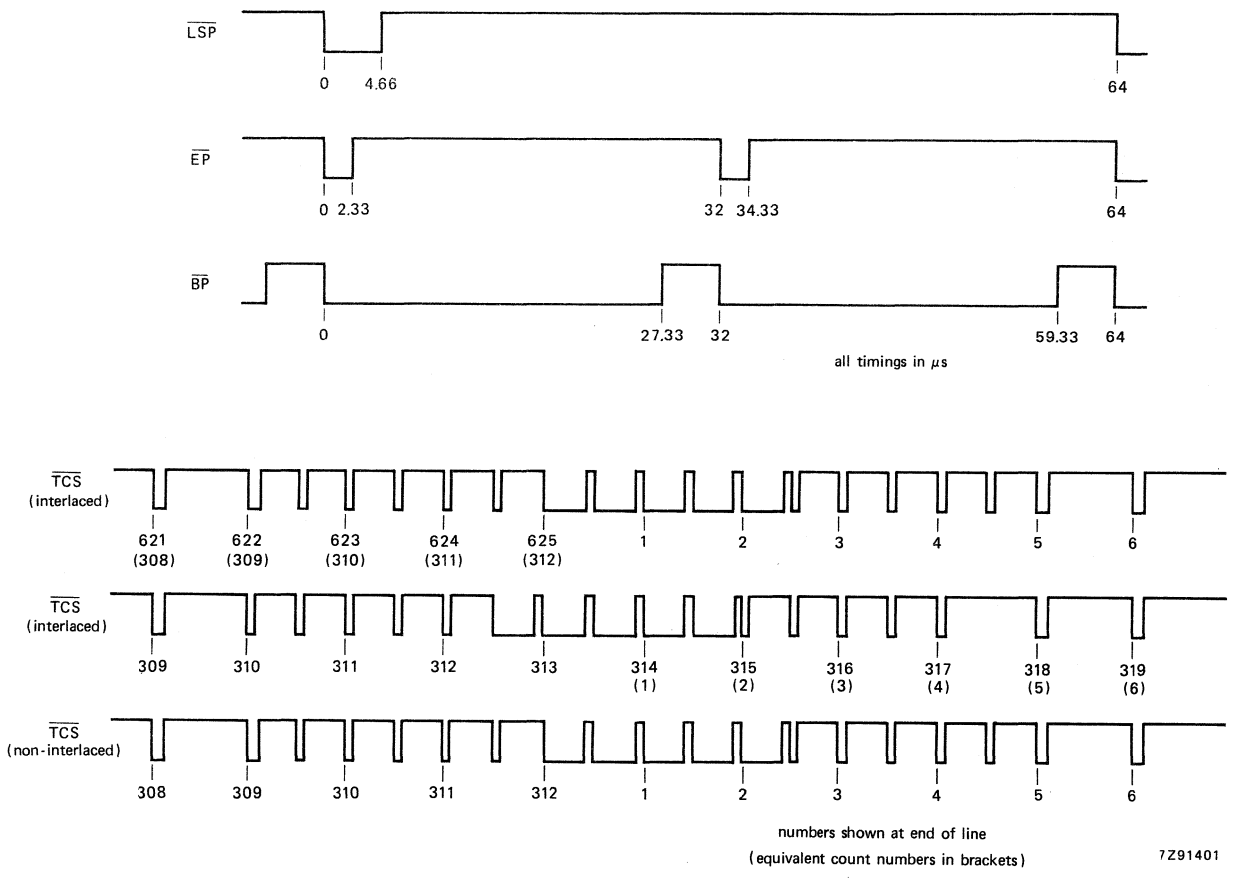


Fig.5 Synchronization timing.



Line sync pulses ($\overline{LSP}$), equalizing pulses ($\overline{EP}$) and broad pulses ($\overline{BP}$) are combined to provide the text composite sync waveform ($\overline{TCS}$) as shown. All timings measured from falling edge of $\overline{LSP}$ with a tolerance of ± 100 ns.

Fig.6 Composite sync waveforms.

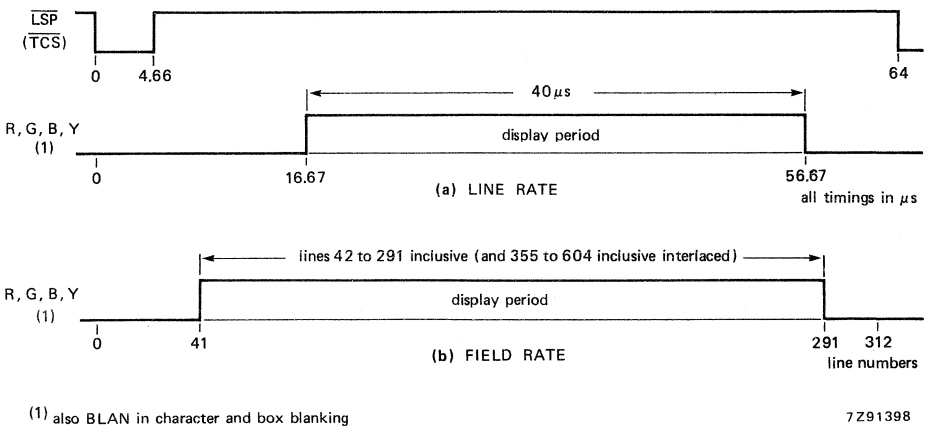


Fig.7 Display output timing (a) line rate (b) field rate.

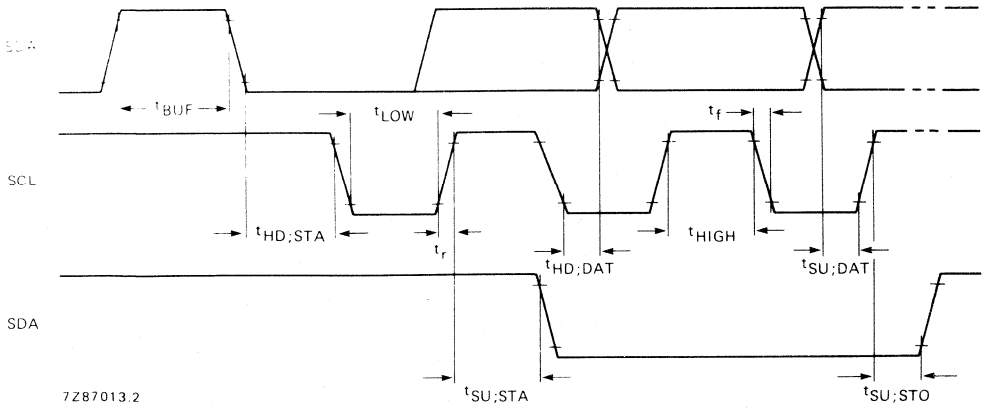


Fig.8 I²C-bus timing.

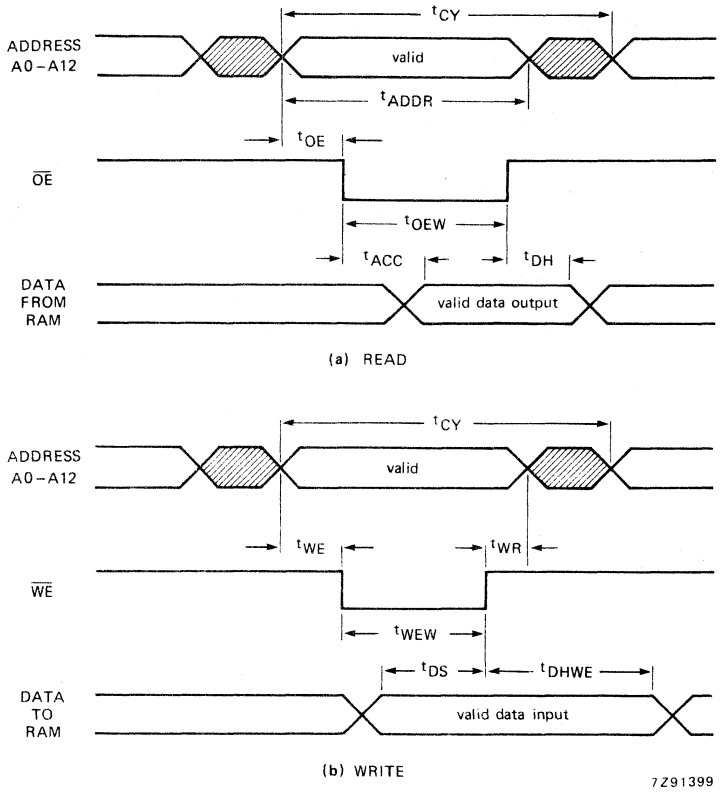
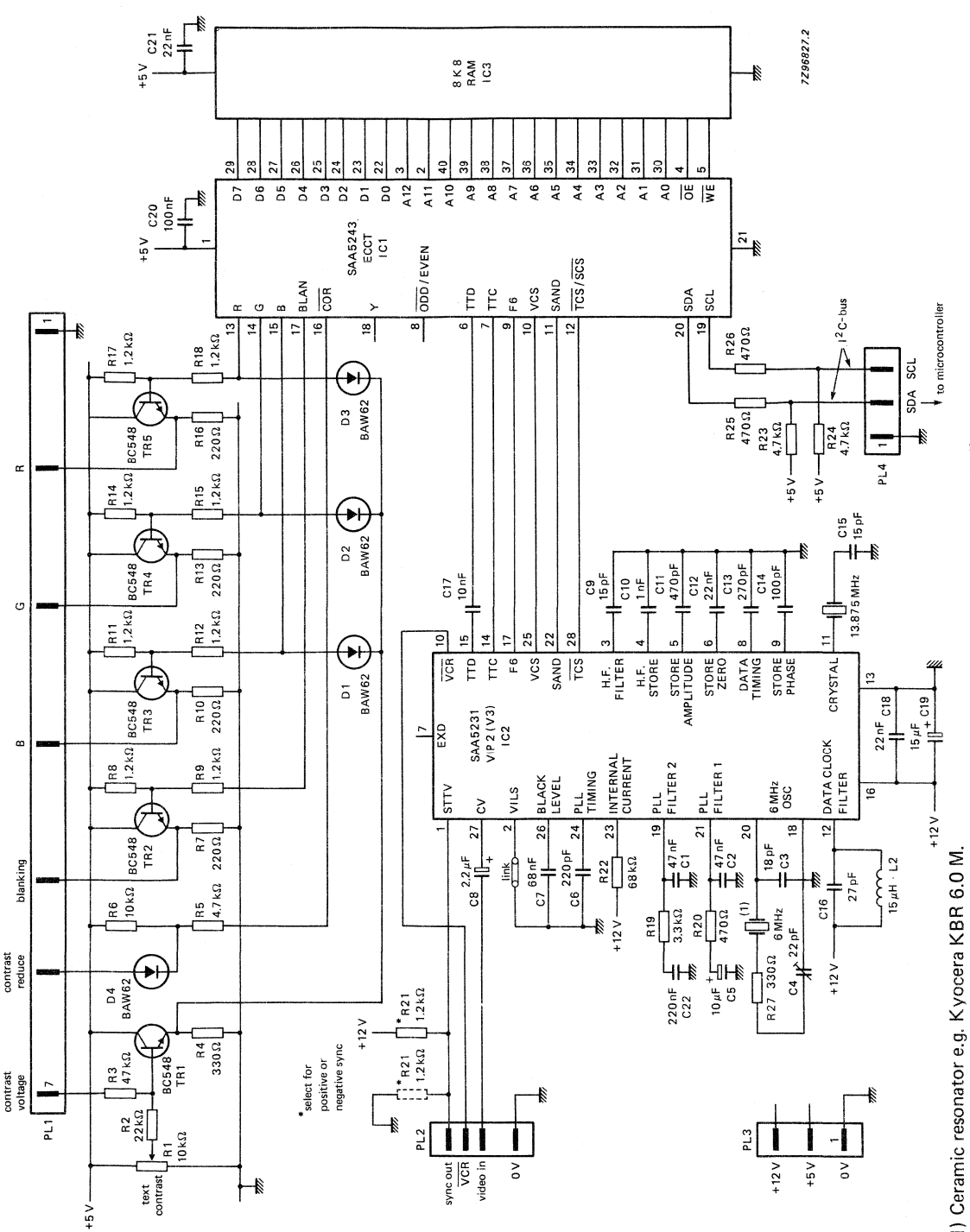


Fig.9 Memory interface timing (a) read (b) write.

APPLICATION INFORMATION



(1) Ceramic resonator e.g. Kyocera KBR 6.0 M.

Fig. 10 ECCT based multi··ge decoder circuit diagram.

APPLICATION INFORMATION (continued)

ECCT page memory organization

The organization of a page memory is shown in Fig.11. The ECCT provides an additional row compared with first generation decoders bringing the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page as broadcast and row 24 is the extra row available for user-generated status messages.

A MORE DETAILED DESCRIPTION OF ECCT OPERATION AND APPLICATION IS AVAILABLE ON REQUEST.

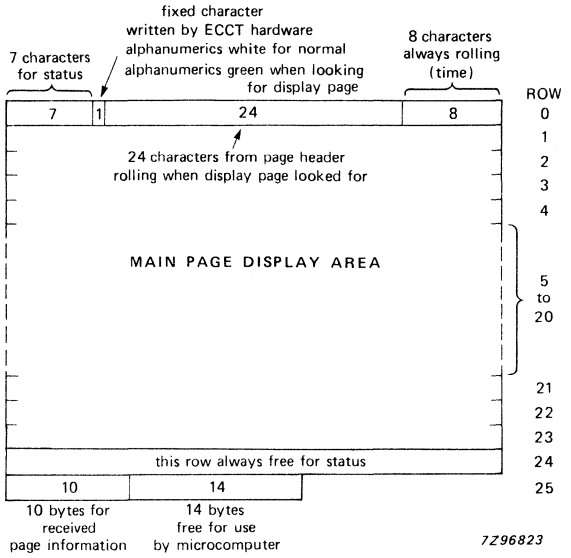


Fig.11 Page memory organization.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

MAG	magazine	page number	MU	minutes units	page sub-code
PU	page units		MT	minutes tens	
PT	page tens		HU	hours units	
PBLF	page being looked for		HT	hours tens	
$\overline{\text{FOUND}}$	LOW for page has been found		C4-C14	transmitted control bits	
HAM.ER	Hamming error in corresponding byte				

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by ECCT to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of row 25 contain control data relating to the received page. Seven digits are used to identify a page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

Register maps

ECCT mode registers R1 to R11 are shown in Table 2. R1 to R10 are WRITE only; R11 is READ/WRITE.
Register map (R3), for page requests, is shown in detail in Table 3.

Table 2 ECCT register map

D7	D6	D5	D4	D3	D2	D1	D0		
TA	$\overline{7+P}$/ 8 BIT	ACQ. $\overline{ON}$/OFF	EXTENSION PACKET ENABLE	$\overline{DEW}$/ FULL FIELD	TCS ON	T1	T0	R1	Mode
—	BANK SELECT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0	R2	Page request address
—	—	—	PRD4	PRD3	PRD2	PRD1	PRD0	R3	Page request data
—	—	—	—	—	A2	A1	A0	R4	Display chapter
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R5	Display control (normal)
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R6	Display control (newsflash/subtitle)
STATUS ROW $\overline{BTM}$/TOP	CURSOR ON	$\overline{CONCEAL}$/ REVEAL	$\overline{TOP}$/ BOTTOM	$\overline{SINGLE}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	R7	Display mode
—	—	—	—	CLEAR MEM.	A2	A1	A0	R8	Active chapter
—	—	—	R4	R3	R2	R1	R0	R9	Active row
—	—	C5	C4	C3	C2	C1	C0	R10	Active column
D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)	R11	Active data

— bit does not exist

Notes to Table 2

The arrows shown on the right of the register map indicate that the register auto-increments to the next one on the following I^2C transmission byte. TA and TB must be logic 0 for normal operation.
All bits in registers R1 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R5 and R6 which are set to logic 1.
All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha white' (00000111) as the acquisition circuit is enabled but all pages are on hold.

APPLICATION INFORMATION (continued)

Table 2 (continued)

Where:

R1 Mode

T0, T1	interlace/non-interlace 312/313 line control
TCS ON	text composite sync or direct sync select
$\overline{\text{DEW}}$/FULL FIELD	field-flyback or full channel mode
$\overline{7+P}$/8 BIT	7 bits with parity checking or 8-bit mode
TA, TB	test bits; 0 for normal operation
R2 Page request address	
START COLUMN	start column for page request data
ACQ CCT	selects one of four acquisition circuits
BANK SELECT	selects bank of four pages being addressed for acquisition
R3 Page request data	see Table 3
R4 Display chapter	determines which of the 8 pages is displayed
R5, R6 Display control	for normal and newsflash/subtitle
PON	picture on
TEXT	text on
COR	contrast reduction on
BKGND	background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 Display mode

BOX ON 0 (1-23, 24)	boxing function allowed on row 0 (row 1-23, 24)
STATUS ROW $\overline{\text{BTM}}$/TOP	row 25 displayed above or below the main text
R8 to R11	active chapter, row, column and data information written to or read from page memory via the I^2C-bus.

Table 3 Register map for page requests (R3)

Start Column	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

Abbreviations are as for Table 1 except for DO CARE bits.
When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
There are four groups of data shown in Table 3, one for each acquisition circuit (four simultaneous page requests).
Columns auto-increment on successive I^2C transmission bytes.

APPLICATION INFORMATION (continued)

CHARACTER SETS

Several versions of the ECCT are available, offering a variety of character sets. The full character sets are shown in Tables 4a to 4d.

The world system teletext specification allows the selection of national character sets via the page header transmission bits, C12 to C14. These bits are automatically decoded by the ECCT, the resulting character sets are shown in Tables 6a to 6d. For certain languages, control software processing of the extension packet data may be required for optimum useage of the range of available characters. See Fig. 12 for alphanumeric and graphic options.

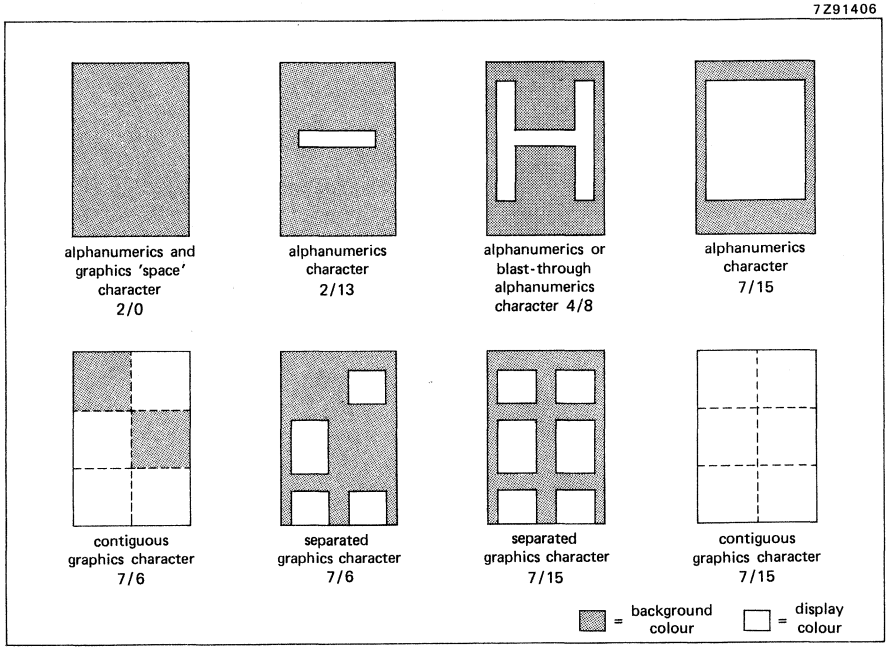


Fig.12 Alphanumeric and graphic options.

Table 4a Character data input decoding, West European languages (SAA5243P/E/M2)

BITS b_8				0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
b_7				0	0	0	0	0	0	1	1	1		1		0	0	1	1	1	1
b_6				0	0	1	1	1	1	0	0	1		1		0	0	0	0	1	1
b_5				0	1	0	1	1	1	0	1	0		1		0	1	0	1	0	1
b_4	b_3	b_2	b_1	row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0	0	0	0	0	alpha - numerics black	graphics black																
0	0	0	1	1	alpha - numerics red	graphics red																
0	0	1	0	2	alpha - numerics green	graphics green																
0	0	1	1	3	alpha - numerics yellow	graphics yellow																
0	1	0	0	4	alpha - numerics blue	graphics blue																
0	1	0	1	5	alpha - numerics magenta	graphics magenta																
0	1	1	0	6	alpha - numerics cyan	graphics cyan																
0	1	1	1	7	alpha - numerics white **	graphics white																
1	0	0	0	8	flash	conceal display																
1	0	0	1	9	steady **	contiguous graphics **																
1	0	1	0	10	end box **	separated graphics																
1	0	1	1	11	start box	ESC *																
1	1	0	0	12	normal height **	black back - ground **																
1	1	0	1	13	double height	new back - ground																
1	1	1	0	14	SO *	hold graphics																
1	1	1	1	15	SI *	release graphics **																

MBA429

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

APPLICATION INFORMATION (continued)

Table 4b Character data input decoding, East European languages (SAA5243P/H)

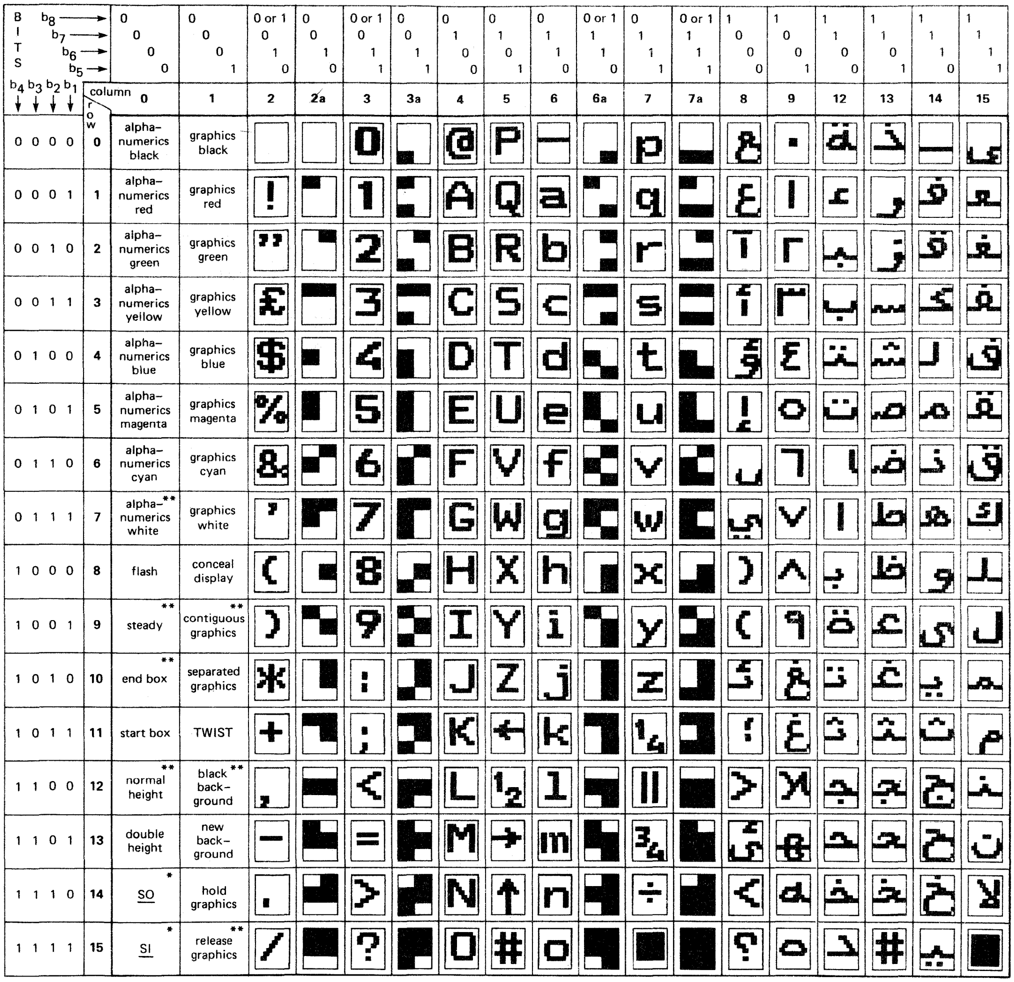
BITS b_8	0	0	0 or 1	0	0 or 1	0	0	0	0	0	1	1	1	1	1	1
b_7	0	0	0	0	1	1	1	1	1	1	0	0	1	1	1	1
b_6	0	0	1	1	1	1	0	0	1	1	0	0	1	1	1	1
b_5	0	1	0	0	0	0	0	1	1	1	0	1	0	0	1	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓ row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha-numerics black	graphics black															
0 0 0 1	1	alpha-numerics red	graphics red															
0 0 1 0	2	alpha-numerics green	graphics green															
0 0 1 1	3	alpha-numerics yellow	graphics yellow															
0 1 0 0	4	alpha-numerics blue	graphics blue															
0 1 0 1	5	alpha-numerics magenta	graphics magenta															
0 1 1 0	6	alpha-numerics cyan	graphics cyan															
0 1 1 1	7	alpha-** numerics white	graphics white															
1 0 0 0	8	flash	conceal display															
1 0 0 1	9	** steady	** contiguous graphics															
1 0 1 0	10	** end box	separated graphics															
1 0 1 1	11	start box	* ESC															
1 1 0 0	12	** normal height	black ** background															
1 1 0 1	13	double height	new background															
1 1 1 0	14	* SO	hold graphics															
1 1 1 1	15	* SI	** release graphics															

7Z22497.5

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Table 4c Character data input decoding, Arabic and English languages (SAA5243P/K)


B I T S
b8 b7 b6 b5
b4 b3 b2 b1
column
row
0 1 2 2a 3 3a 4 5 6 6a 7 7a 8 9 12 13 14 15
alpha-numerics black
graphics black
alpha-numerics red
graphics red
alpha-numerics green
graphics green
alpha-numerics yellow
graphics yellow
alpha-numerics blue
graphics blue
alpha-numerics magenta
graphics magenta
alpha-numerics cyan
graphics cyan
alpha-numerics white**
graphics white
flash
conceal display
steady**
contiguous graphics**
end box**
separated graphics
start box
TWIST
normal height**
black back-ground**
double height
new back-ground
SO*
hold graphics
SI*
release graphics**

7Z22660.4

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

APPLICATION INFORMATION (continued)

Table 4d Character data input decoding, Arabic and Hebrew languages (SAA5243P/L)

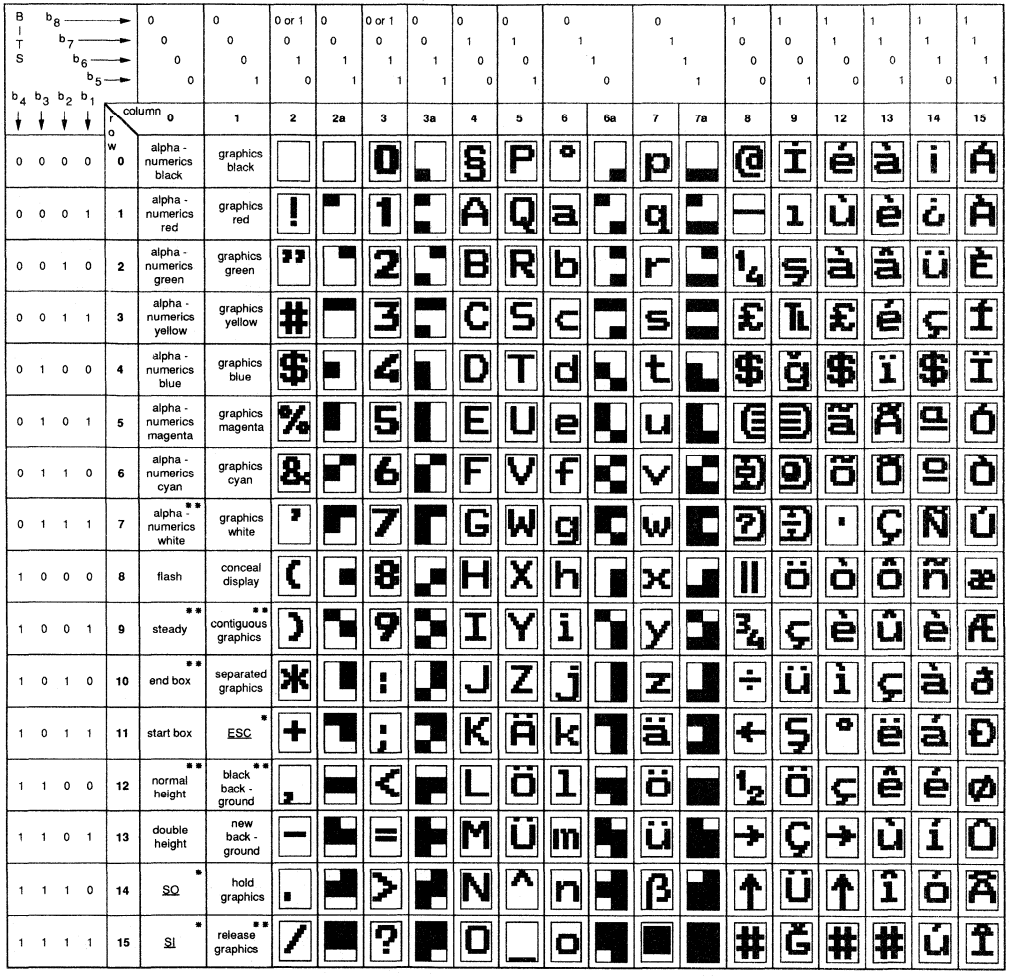
BITS b_8	0	0	0 or 1	0	0 or 1	0	0	0	0	0 or 1	0	0 or 1	1	1	1	1	1	1
b_7	0	0	0	0	0	0	1	1	1	1	1	1	0	0	1	1	1	1
b_6	0	0	1	1	1	1	0	0	1	1	1	1	0	0	0	0	1	1
b_5	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓ row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha-numerics black	graphics black															
0 0 0 1	1	alpha-numerics red	graphics red															
0 0 1 0	2	alpha-numerics green	graphics green															
0 0 1 1	3	alpha-numerics yellow	graphics yellow															
0 1 0 0	4	alpha-numerics blue	graphics blue															
0 1 0 1	5	alpha-numerics magenta	graphics magenta															
0 1 1 0	6	alpha-numerics cyan	graphics cyan															
0 1 1 1	7	alpha-** numerics white	graphics white															
1 0 0 0	8	flash	conceal display															
1 0 0 1	9	** steady	** contiguous graphics															
1 0 1 0	10	** end box	separated graphics															
1 0 1 1	11	start box	TWIST															
1 1 0 0	12	** normal height	black ** back-ground															
1 1 0 1	13	double height	new back-ground															
1 1 1 0	14	* SO	hold graphics															
1 1 1 1	15	* SI	** release graphics															

7Z22679.4

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Table 4e Character data input decoding, West European and Turkish languages (SAA5243P/T)



MBA428

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

APPLICATION INFORMATION (continued)

Table 4f Character data input decoding, Baltic and Cyrillic Russian (SAA5243P/R)

BITS b_8				0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
b_7				0	0	0	0	0	0	1	1	1		1		0	0	1	1	1	1
b_6				0	0	1	1	1	1	0	0	1		1		0	0	0	0	1	1
b_5				0	1	0	1	1	1	0	1	0		1		0	1	0	1	0	1
b_4	b_3	b_2	b_1	row \ column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0	0	0	0	0	alpha - numerics black	graphics black															
0	0	0	1	1	alpha - numerics red	graphics red															
0	0	1	0	2	alpha - numerics green	graphics green															
0	0	1	1	3	alpha - numerics yellow	graphics yellow															
0	1	0	0	4	alpha - numerics blue	graphice blue															
0	1	0	1	5	alpha - numerics magenta	graphics magenta															
0	1	1	0	6	alpha - numerics cyan	graphics cyan															
0	1	1	1	7	alpha - numerics white **	graphics white															
1	0	0	0	8	flash	conceal display															
1	0	0	1	9	steady **	contiguous graphics **															
1	0	1	0	10	end box **	separated graphics															
1	0	1	1	11	start box	ESC *															
1	1	0	0	12	normal height **	black back - ground **															
1	1	0	1	13	double height	new back - ground															
1	1	1	0	14	SO *	hold graphics															
1	1	1	1	15	SI *	release graphics **															

MBA648

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Notes to Table 4

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Codes may be referred to by column and row. For example 2/5 refers to %.
3. Black represents displayed colour. White represents background.
4. Character rectangle shown as follows: □
5. National option characters are shown in Table 6.
6. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters (for /E and /H character tables only) to combine with character 8/5.
7. With bit 8 = 0 national option character will be decoded according to the setting of control bits C12 to C14 (see Table 6).

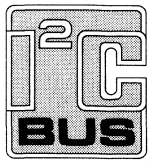
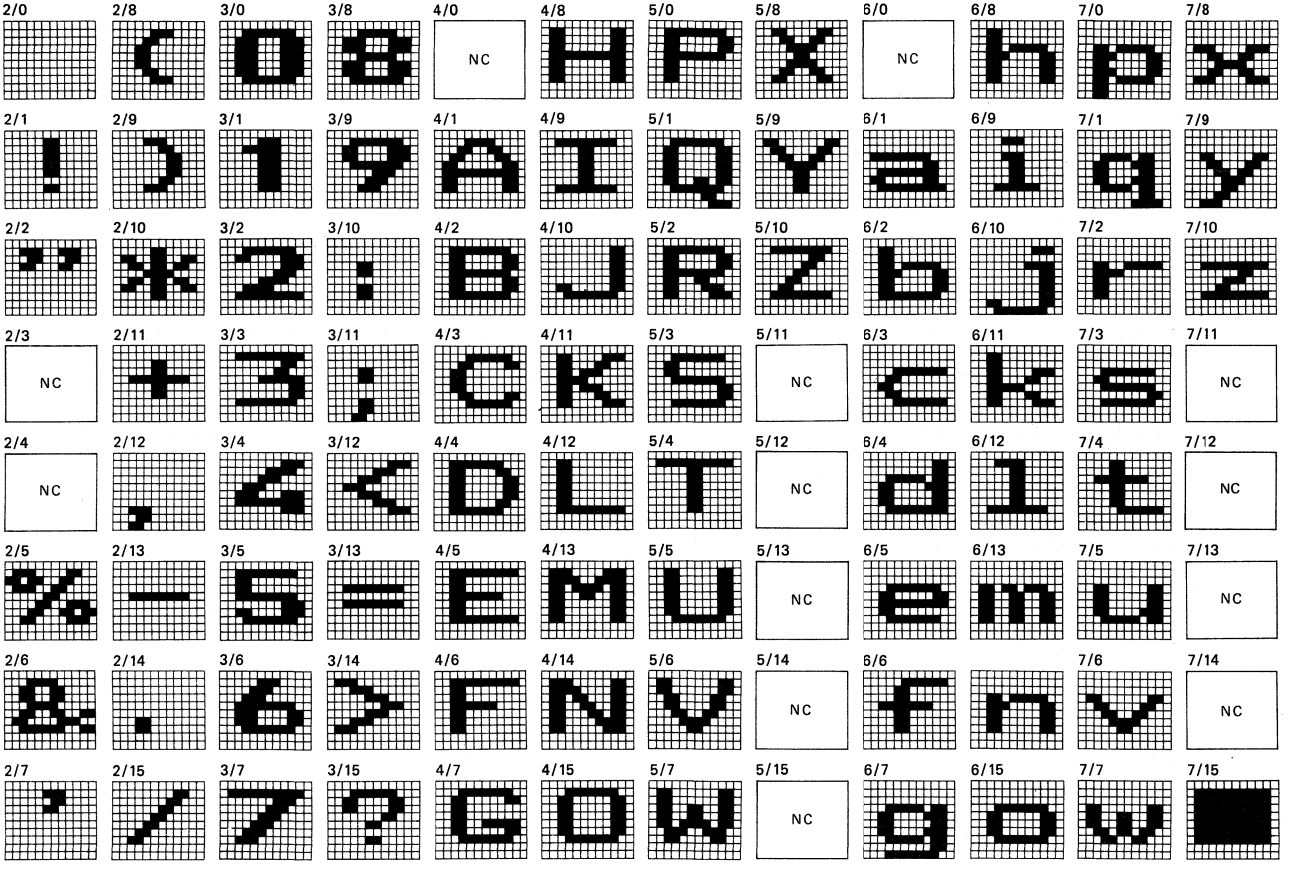


Table 5 SAA5243 basic character matrix



Where: NC national option character position.

APPLICATION INFORMATION (continued)

Table 6a SAA5243P/E/M2 national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN/ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

7Z22659.2

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 5.

Table 6b SAA5243P/H national option character set

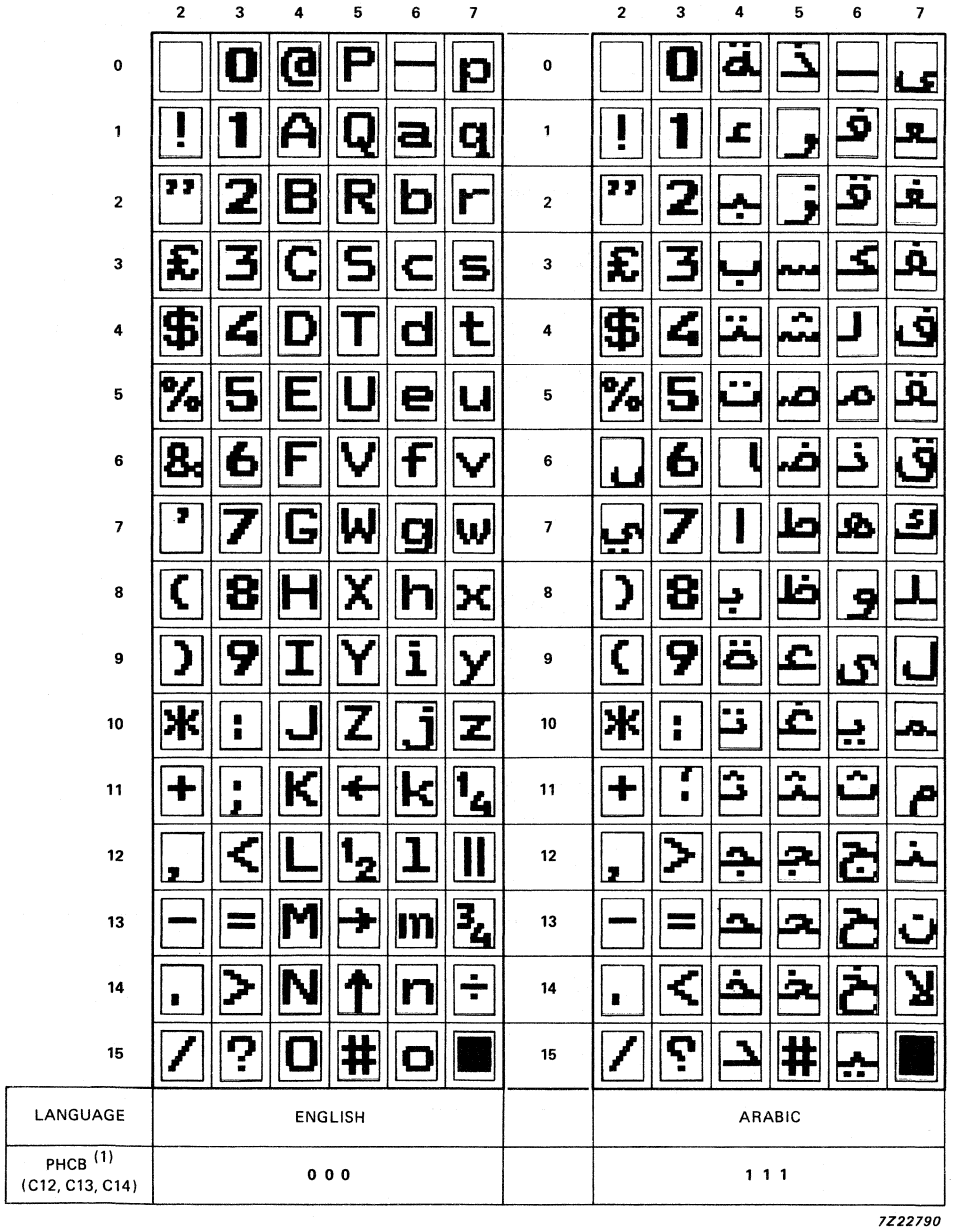
LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN/ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
POLISH	0	0	0	#	ń	ą	Ż	Ś	Ł	ć	ó	ę	ż	ś	ł	ź
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
SERBO-CROAT	1	0	1	#	½	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
CZECHOSLOVAK	1	1	0	#	ů	č	ť	ž	ý	í	ř	é	á	ě	ú	š
RUMANIAN	1	1	1	#	¤	Ţ	Â	Ş	Ă	Î	ı	ţ	â	ş	ă	î

7Z22658.1

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to German. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 5.

APPLICATION INFORMATION (continued)

Table 6c SAA5243P/K national option character set

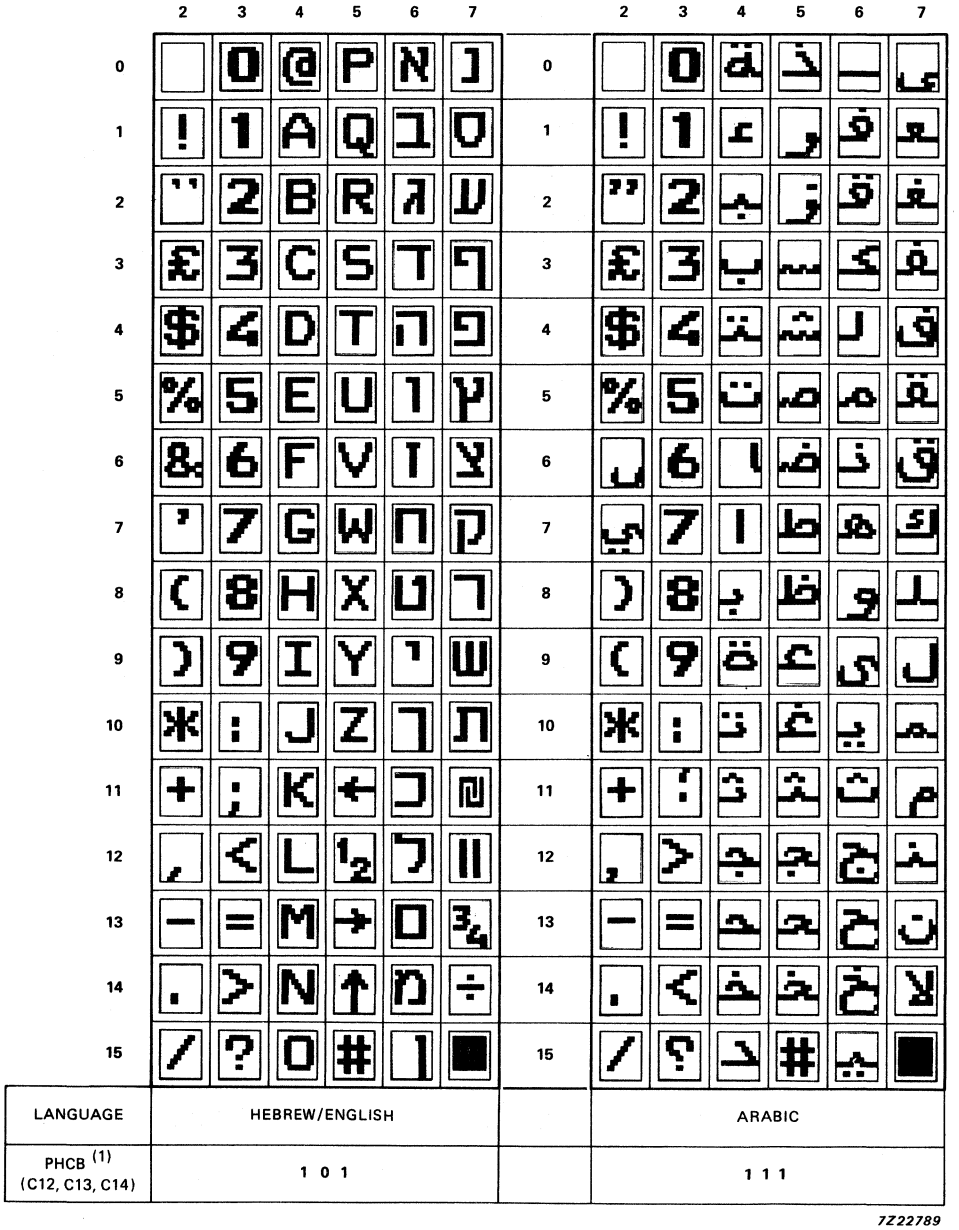


LANGUAGE	ENGLISH	ARABIC
PHCB (1) (C12, C13, C14)	0 0 0	1 1 1

7Z22790

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English.

Table 6d SAA5243P/L national option character set



(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English.

APPLICATION INFORMATION (continued)

Table 6e SAA5243P/T national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
TURKISH	1	1	0	₺	ğ	İ	Ş	Ö	Ç	Ü	Ğ	ı	ş	ö	ç	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MBA430

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 5.

Table 6f SAA5243R/L national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ESTONIAN	0	1	0	#	Õ	Š	Ä	Ö	Ž	Ü	õ	š	ä	ö	ž	ü
LETTISH / LITHUANIAN	0	1	1	#	$	Š	ė	ę	Ž	č	ū	š	ą	ų	ž	į
RUSSIAN	1	0	0		0	Ю	П	ю	п							
				!	1	А	Я	а	я							
				"	2	Б	Р	б	р							
				#	3	Ц	С	ц	с							
				$	4	Д	Т	д	т							
				%	5	Е	У	е	у							
				ы	6	Ф	Ж	ф	ж							
				'	7	Г	В	г	в							
				(	8	Х	Ь	х	ь							
				)	9	И	Ъ	и	ъ							
				*	:	Й	З	й	з							
				+	;	К	Ш	к	ш							
				,	<	Л	Э	л	э							
				−	=	М	Щ	м	щ							
				.	>	Н	Ч	н	ч							
				/	?	О	Ы	о	■							

MBA647

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English.

Integrated VIP and teletext decoder (IVT1.1)

SAA5244A

FEATURES

- Complete teletext decoder including page memory in a single 40-pin DIL package
- Single +5 V power supply
- Digital data slicer and display clock phase-locked loop reduces peripheral components to a minimum
- Both video and scan related synchronization modes are supported
- On board single page memory including extension packets for FASTEXT
- Single page acquisition system
- RGB interface to standard colour decoder ICs, push-pull output drive
- Data capture performance similar to SAA5231 (VIP2)
- Simple software control via I²C-bus
- Option for five national languages
- 32 supplementary characters for on-screen displays
- Optional storage of packet 24 in the display memory
- Page links in packets 27 and 8/30 are Hamming decoded
- Separate text and video signal quality detectors, 625/525 video status and language version all readable via I²C-bus
- Automatic ODD/$\overline{\text{EVEN}}$ output control with manual override
- Control of display PLL free-run and rolling header via I²C-bus
- VCS to SCS mode for stable 525 line status display

DESCRIPTION

The Integrated VIP and Teletext (IVT1.1) is a teletext decoder (contained within a single-chip package) for decoding 625-line based World System Teletext transmissions. The teletext decoder hardware is based on a reduced function version of the device SAA5246 (IVT1.0).

The Video Input Processor (VIP) section of the device uses mixed analog and digital designs for the data slicer and the display clock phase-locked loop functions. As a result the number of external components is greatly reduced and no critical or adjustable components are required. A single page static RAM is incorporated in the device thereby giving a genuine single-chip teletext decoder device.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5244AP	40	DIL	plastic	SOT129
SAA5244AP	42	SDIL	plastic	SOT270
SAA5244AGP	44	QFP	plastic	SOT205A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5	5.5	V
I_{DD}	supply current	–	74	148	mA
V_{syn}	sync amplitude	0.1	0.3	0.6	V
V_{vid}	video amplitude	0.7	1	1.4	V
f_{XTAL}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature range	−20	–	70	°C

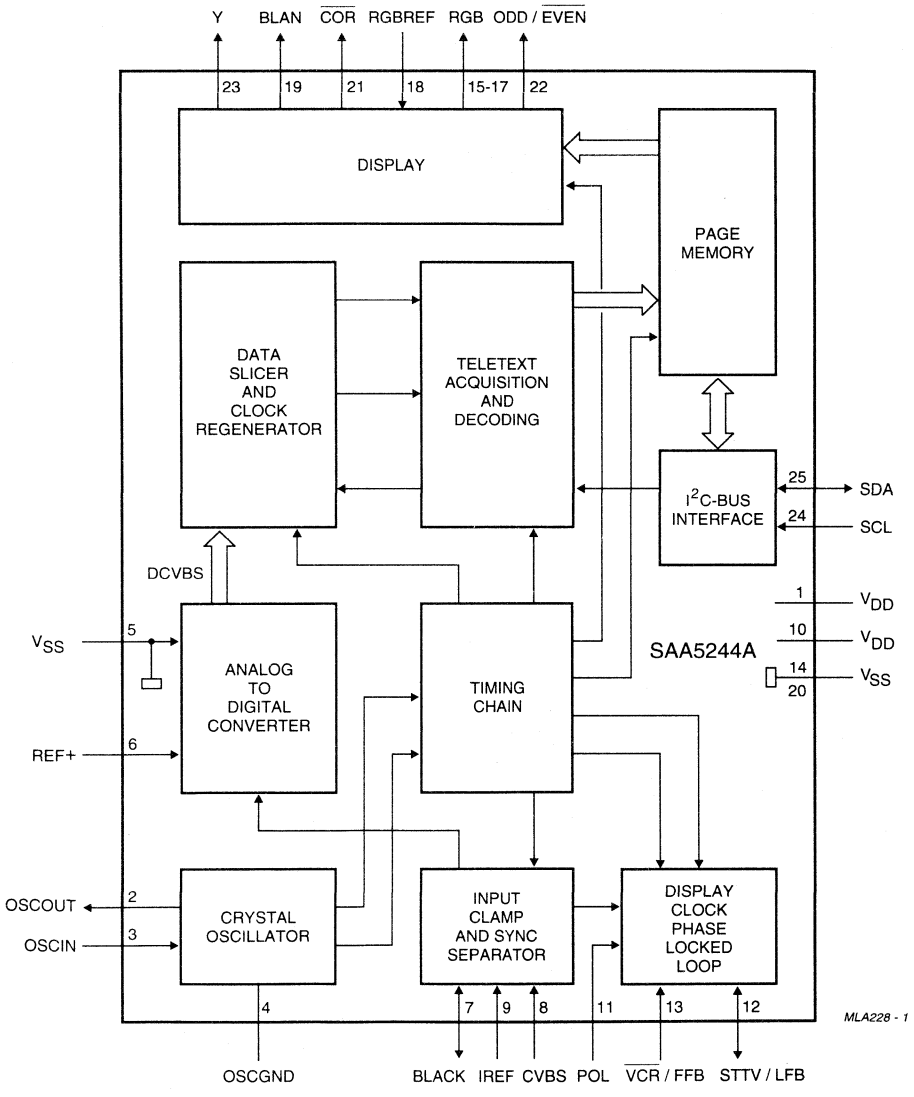


Fig.1 Block diagram for SOT129 (DIL40) package.

PINNING

SYMBOL	SOT129	SOT270	SOT205A	DESCRIPTION
V_{DD}	1	1	18	+5 V supply
OSCOUT	2	2	19	27 MHz crystal oscillator output
OSCIN	3	3	20	27 MHz crystal oscillator input
OSCGND	4	4	21	0 V crystal oscillator ground
V_{SS}	5	5	22	0 V ground
REF–	–	6	–	negative reference voltage for the ADC. The pin should be connected to 0 V
REF+	6	7	23	positive reference voltage for the ADC. The pin should be connected to +5 V
BLACK	7	8	24	video black level storage pin, connected to ground via a 100 nF capacitor
CVBS	8	9	25	composite video input pin. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor
IREF	9	10	26	reference current input pin, connected to ground via a 27 kΩ resistor
V_{DD}	10	11	27	+5 V supply
POL	11	12	28	STTV/LFB/FFB polarity selection pin
STTV/LFB	12	13	29	sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode)
$\overline{VCR}$/FFB	13	14	32	PLL time constant switch/field flyback input pin. Function controlled by an internal register bit (scan sync mode)
V_{SS}	14	15	33	0 V ground
R	15	16	34	dot rate character output of the RED colour information
G	16	17	35	dot rate character output of the GREEN colour information
B	17	18	36	dot rate character output of the BLUE colour information
RGBREF	18	19	37	input DC voltage to define the output high level on the RGB pins
BLAN	19	20	38	dot rate fast blanking output
V_{SS}	20	21	39	0 V ground
$\overline{COR}$	21	22	40	programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages; open drain output
ODD/$\overline{EVEN}$	22	23	41	25 Hz output synchronized with the CVBS input's field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents
Y	23	24	42	dot rate character output of teletext foreground colour information; open drain output

SYMBOL	SOT129	SOT270	SOT205A	DESCRIPTION
SCL	24	25	43	serial clock input for the I²C-bus. It can still be driven during power-down of the device
SDA	25	26	44	serial data port for the I²C-bus; open drain output. It can still be driven during power-down of the device
n.c.	–	27, 31, 32	4 to 7 30, 31	not connected
i.c.	26 to 40	28 to 30 33 to 42	1 to 3 8 to 17	internally connected. Must be left open-circuit in application

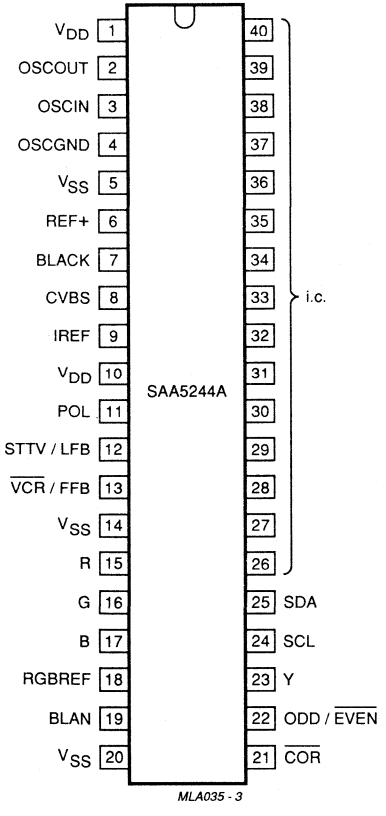


Fig.2 Pin configuration; SOT129 (DIL40).

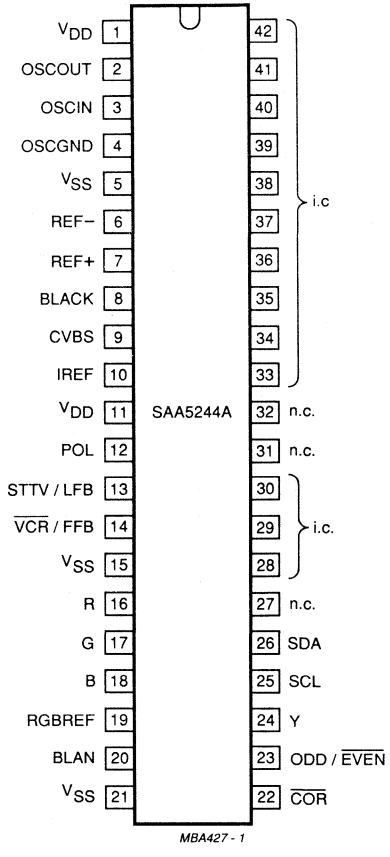


Fig.3 Pin configuration; SOT270 (SDIL42).

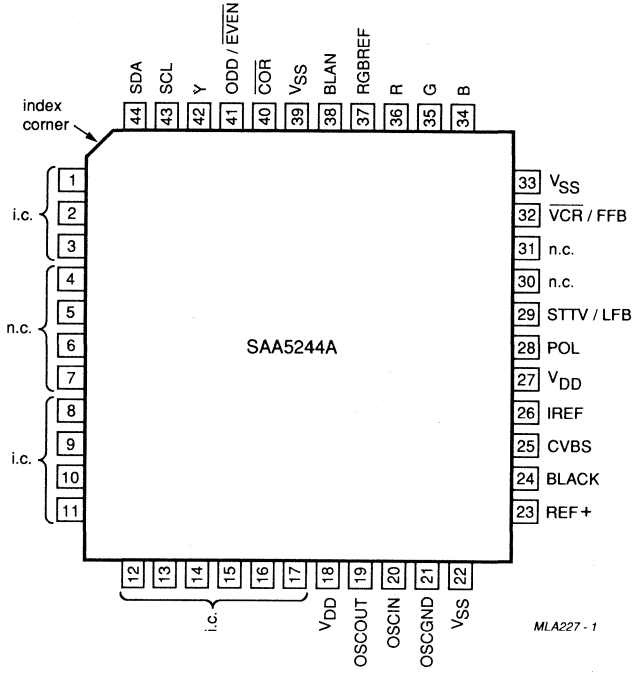


Fig.4 Pin configuration; SOT205A (QFPL44).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	−0.3	6.5	V
V_I	input voltage (any input)	−0.3	V_{DD}+0.5	V
V_O	output voltage (any output)	−0.3	V_{DD}+0.5	V
I_O	output current (each output)	−	±10	mA
I_{IOK}	DC input or output diode current	−	±20	mA
T_{amb}	operating ambient temperature range	−20	70	°C
T_{stg}	storage temperature range	−55	125	°C
V_{stat}	electrostatic handling human body model (note 1)	−2000	2000	V

Note

1. The human body model ESD simulation is equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor; this produces a single discharge transient. Reference Philips Semiconductors test method UZW-B0/FQ-A302 (compatible with MIL-STD method 3015.7).

Failure Rate

The failure rate at T_{amb} = 55 °C will be a maximum of 1000 FITS (1 FIT = 1 x 10^{-9} failures per hour).

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = −20 to +70 °C, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range (V_{DD}-V_{SS})		4.5	5	5.5	V
I_{DD}	total supply current		–	74	148	mA
Inputs						
CVBS						
V_{syn}	sync amplitude		0.1	0.3	0.6	V
t_{syn}	delay from CVBS to TCS output from STTV buffer (nominal video, average of leading/trailing edge)		−150	0	150	ns
t_{syd}	change in sync delay between all black and all white video input at nominal levels		0	–	25	ns
$V_{vid(p-p)}$	video input amplitude (peak-to-peak)		0.7	1	1.4	V
	display PLL catching range		±7	–	–	%
Z_{src}	source impedance		–	–	250	Ω
C_I	input capacitance		–	–	10	pF
IREF						
R_g	resistor to ground		–	27	–	kΩ
POL						
V_{IL}	input voltage LOW		−0.3	–	0.8	V
V_{IH}	input voltage HIGH		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	µA
C_I	input capacitance		–	–	10	pF
LFB						
V_{IL}	input voltage LOW		−0.3	–	0.8	V
V_{IH}	input voltage HIGH		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	µA
I_I	input current	note 1	−1	–	1	mA
t_{LFB}	delay between LFB front edge and input video line sync		–	250	–	ns
$\overline{VCR}$/FFB						
V_{IL}	input voltage LOW		−0.3	–	0.8	V
V_{IH}	input voltage HIGH		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	µA
I_I	input current	note 1	−1	–	1	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
RGBREF (NOTE 2)						
V_I	input voltage		−0.3	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	µA
I_{DC}	DC current		–	–	10	mA
SCL						
V_{IL}	input voltage LOW		−0.3	–	1.5	V
V_{IH}	input voltage HIGH		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	µA
f_{SCL}	clock frequency		0	–	100	kHz
t_r	input rise time	10% to 90%	–	–	2	µs
t_f	input fall time	90% to 10%	–	–	2	µs
C_I	input capacitance		–	–	10	pF
Inputs/outputs						
CRYSTAL OSCILLATOR (OSCIN; OSCOUT)						
f_{XTAL}	crystal frequency		–	27	–	MHz
G_v	small signal voltage gain		3.5	–	–	–
G_m	mutual conductance	f = 100 kHz	1.5	–	–	mA/V
C_I	input capacitance		–	–	10	pF
C_{FB}	feedback capacitance		–	–	5	pF
BLACK						
C_{blk}	storage capacitor to ground		–	100	–	nF
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	µA
SDA						
V_{IL}	input voltage LOW		−0.3	–	1.5	V
V_{IH}	input voltage HIGH		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	µA
C_I	input capacitance		–	–	10	pF
t_r	input rise time	10% to 90%	–	–	2	µs
t_f	input fall time	90% to 10%	–	–	2	µs
V_{OL}	output voltage LOW	I_{OL} = 3 mA	0	–	0.5	V
t_f	output fall time	3 to 1 V	–	–	200	ns
C_L	load capacitance		–	–	400	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
STTV						
G_{stt}	gain of STTV relative to video input		0.9	1.0	1.1	
V_{tcs}	TCS amplitude		0.2	0.3	0.45	V
V_{DCs}	DC shift between TCS output and nominal video output		–	–	0.15	V
I_O	output drive current		–	–	3.0	mA
C_L	load capacitance		–	–	100	pF
R, G AND B						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	–	0.2	V
V_{OH}	output voltage HIGH	I_{OH} = −1.6 mA; RGBREF ≤ V_{DD}−2 V	RGBREF −0.25 V	RGBREF	RGBREF +0.25 V	V
$\|Z_o\|$	output impedance		–	–	200	Ω
C_L	load capacitance		–	–	50	pF
I_{DC}	DC current		–	–	−3.3	mA
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
BLAN						
V_{OL}	output voltage LOW	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −0.2 mA; V_{DD} = 4.5 V	1.1	–	–	V
V_{OH}	output voltage HIGH	I_{OH} = 0 mA; V_{DD} = 5.5 V	–	–	2.8	V
V_{OH}	allowed voltage at pin	with external pull-up	–	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
ODD/$\overline{\text{EVEN}}$						
V_{OL}	output voltage LOW	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −1.6 mA	V_{DD}−0.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
$\overline{COR}$ AND Y (OPEN DRAIN)						
V_{OH}	pull-up voltage at pin		–	–	V_{DD}	V
V_{OL}	output voltage LOW	I_{OL} = 5 mA	0	–	1.0	V
C_L	load capacitance		–	–	25	pF
t_f	output fall time	load resistor of 1.2 kΩ to V_{DD}; measured between V_{DD} −0.5 and 1.5 V	–	–	50	ns
I_{LO}	output leakage current	V_I = 0 to V_{DD}	−10	–	10	μA
T_{SK}	skew delay between display outputs R, G, B, $\overline{COR}$, Y and BLAN		–	–	20	ns
Timing						
I²C-BUS						
t_{LOW}	clock LOW period		4	–	–	μs
t_{HIGH}	clock HIGH period		4	–	–	μs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		170	–	–	ns
$t_{SU;STO}$	set-up time from clock HIGH to STOP		4	–	–	μs
t_{BUF}	START set-up time following a STOP		4	–	–	μs
$t_{HD;STA}$	START hold time		4	–	–	μs
$t_{SU;STA}$	START set-up time following clock LOW-to-HIGH transition		4	–	–	μs

Notes to the characteristics

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. Series current limiting resistors must be used to limit the input currents to ± 1 mA.
2. RGBREF is the positive supply for the RGB output pins and it must be able to source the I_{OH} current from the R, G and B pins. The leakage specification on RGBREF only applies when there is no current load on the RGB pins.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

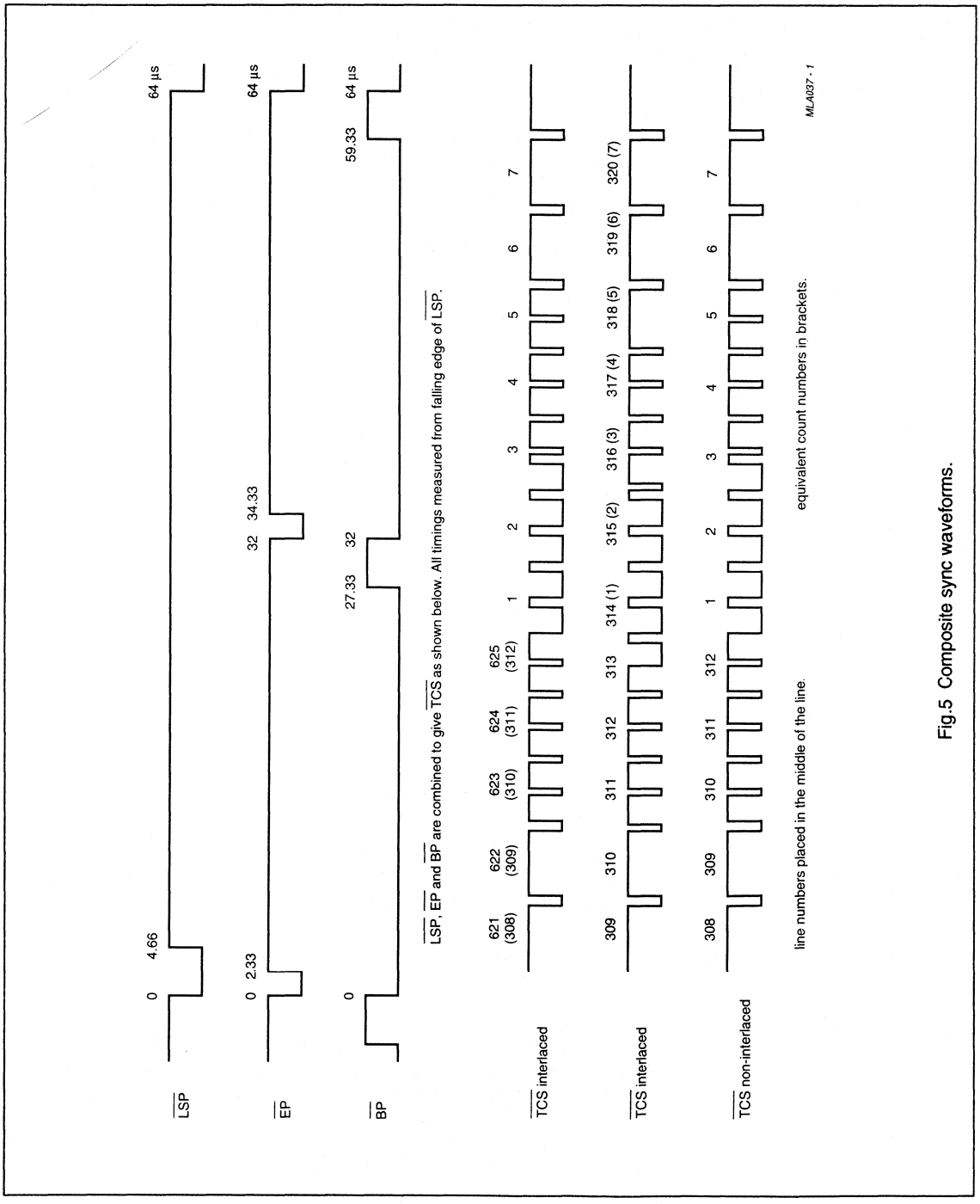


Fig.5 Composite sync waveforms.

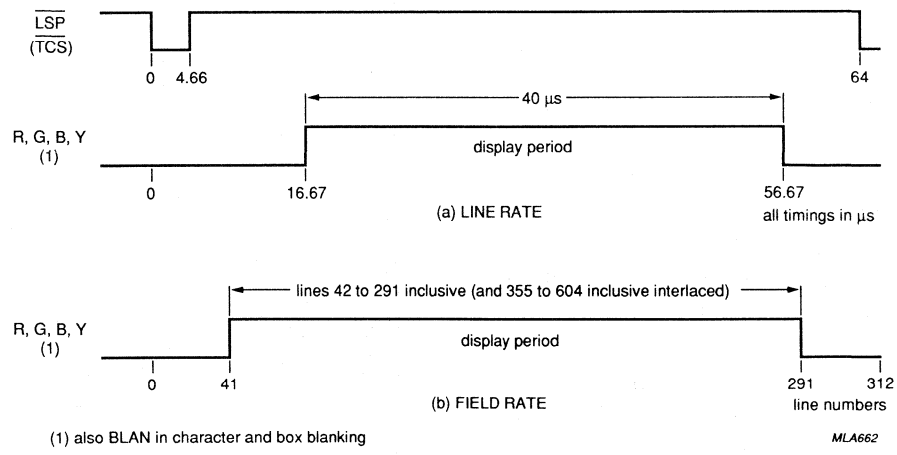


Fig.6 Display output timing (a) line rate (b) field rate.

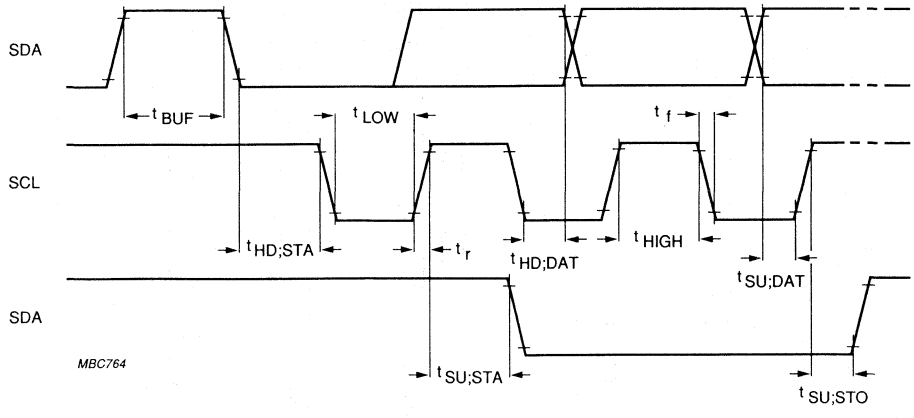


Fig.7 I²C-bus timing.

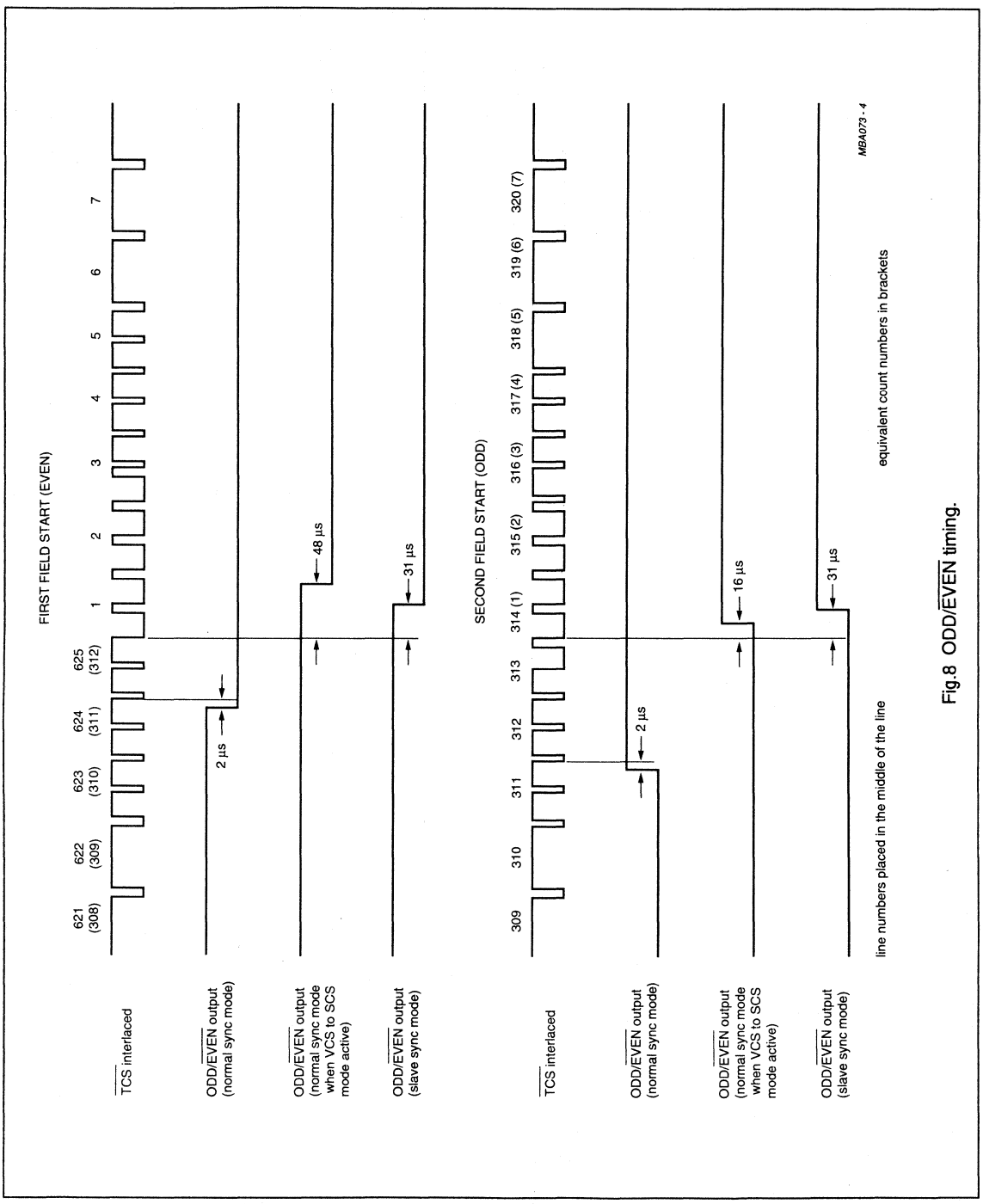
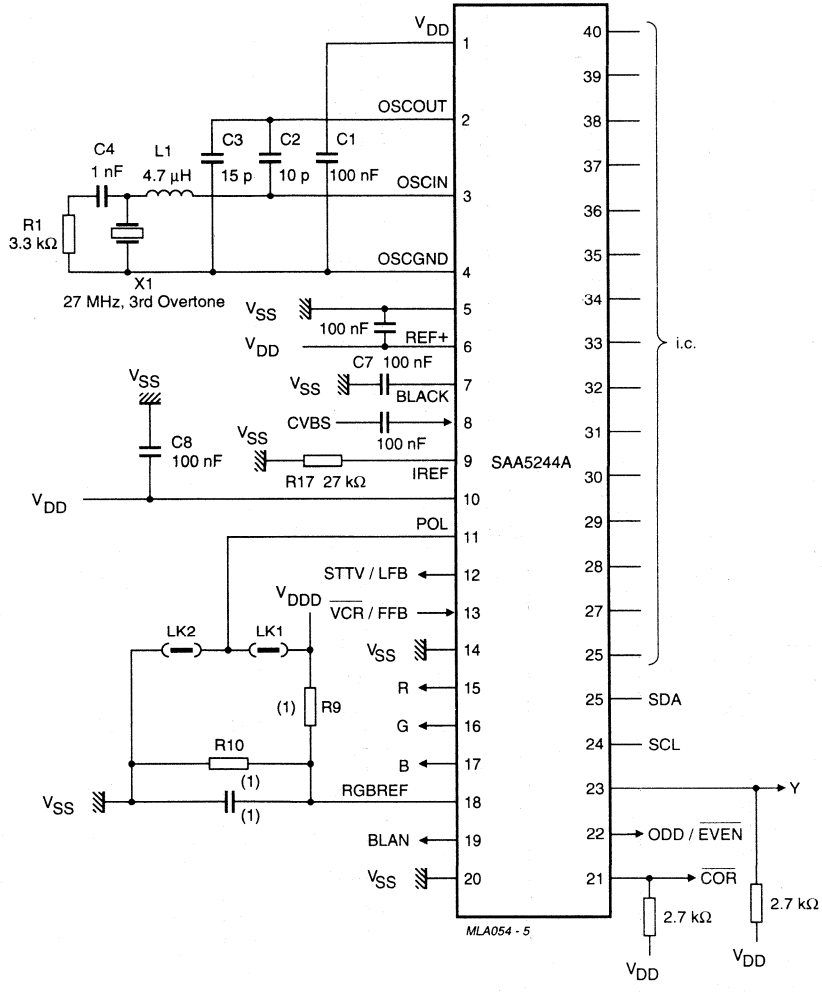


Fig.8 ODD/$\overline{\text{EVEN}}$ timing.

APPLICATION INFORMATION



(1) Value dependent on application.

Fig.9 Application diagram.

SAA5244A page memory organization

The organization of the page memory is shown in Fig.10. The device provides an additional row as compared with first generation decoders; this brings the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page; row 24 is available for software generated status messages and FLOF/FASTEXT prompt information.

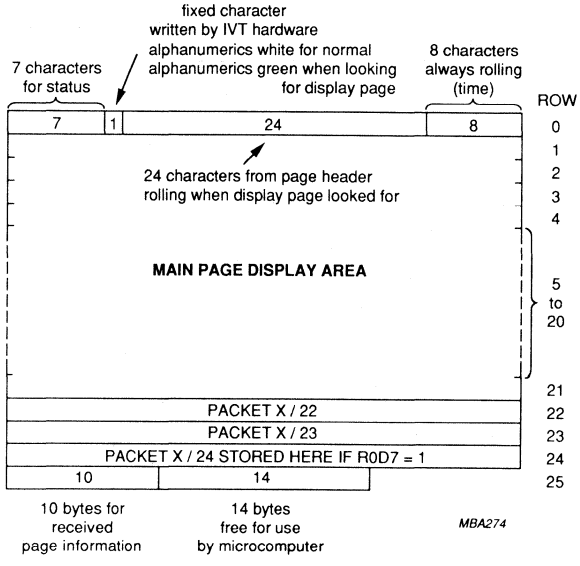


Fig.10 Basic page memory organization.

Row 0:

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by SAA5244A to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25:

The first 10 bytes of row 25 contain control data relating to the received page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

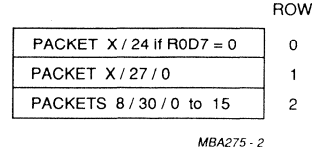


Fig.11 Organization of the extension memory.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

Page number

MAG magazine
PU page units
PT page tens

PBLF page being looked for
$\overline{\text{FOUND}}$ LOW for page has been found
HAM.ER Hamming error in corresponding byte

Page sub-code

MU minutes units
MT minutes tens
HU hours units
HT hours tens

C4-C14 transmitted control bits.

Register maps

SAA5244A mode registers R0 to R11 are shown in Table 2. R0 to R10 are WRITE only; R11 is READ/WRITE. Register map (R3), for page requests, is shown in detail in Table 3.

Table 2 Register map

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
Adv. control	0	X24 POS	FREE RUN PLL	AUTO ODD/$\overline{\text{EVEN}}$	DISABLE HDR ROLL	–	DISABLE ODD/$\overline{\text{EVEN}}$	–	$\overline{\text{R11}}$/R11B SELECT
Mode	1	VCS TO SCS	–	ACQ $\overline{\text{ON}}$/OFF	–	$\overline{\text{DEW}}$/ FULL FIELD	TCS ON	T1	T0
Page request address	2	–	–	–	–	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request data	3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
		–	–	–	–	–	–	–	–
Display control (normal)	5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash /subtitle)	6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	7	STATUS TOP	CURSOR ON	REVEAL ON	BOTTOM HALF	DOUBLE HEIGHT	BOX 24	BOX 1-23	BOX 0
		–	–	–	–	–	–	–	–
Cursor row	9	SUPPL. BLAST	CLEAR MEM.	A0	R4	R3	R2	R1	R0
Cursor column	10	SUPPL. ROW 24	SUPPL. ROW 0	C5	C4	C3	C2	C1	C0
Cursor data	11	–	D6	D5	D4	D3	D2	D1	D0
Device status	11B	$\overline{\text{625}}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	TEXT SIGNAL QUALITY	VCS SIGNAL QUALITY

Notes to Table 2

1. – indicates these bits are inactive and must be written to logic 0 for future compatibility.
2. All bits in registers R0 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R1, R5 and R6 which are set to logic 1.
3. All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha' white (00000111) as the acquisition circuit is enabled but the page is on hold.
4. TB must be set to logic 0 for normal operation.
5. The I^2C slave address is 0010001

Register description

R0 ADVANCED CONTROL - auto increments to Register 1

$\overline{R11}$/R11B SELECT	Selects reading of R11 or R11B
DISABLE ODD/$\overline{EVEN}$	Forces ODD/$\overline{EVEN}$ output LOW when logic 1
DISABLE HDR ROLL	Disables green rolling header and time
AUTO ODD/$\overline{EVEN}$	When set forces ODD/$\overline{EVEN}$ low if any TV picture displayed, if DISABLE ODD/$\overline{EVEN}$ = 0
FREE RUN PLL	Will force the PLL to free run in all conditions
X24 POS	Automatic display of FASTEXT prompt row when logic 1

R1 MODE - auto increments to Register 2

T0, T1	Interlace/non-interlace 312/313 line control (see Table 4)
TCS ON	Text composite sync or direct sync select
$\overline{DEW}$/FULL FIELD	Field-flyback or full channel mode
ACQ $\overline{ON}$/OFF	Aquisition circuits turned off when logic 1
VCS TO SCS	When logic 1 enables display of messages with 60 Hz input signal

R2 PAGE REQUEST ADDRESS - auto increments to Register 3

COL SC0 - SC2	Point to start column for page request data (see Table 3)
TB	Must be logic 0 for normal operation

R3 PAGE REQUEST DATA - does not auto increment (see Table 3)

R5 NORMAL DISPLAY CONTROL - auto increments to Register 6

R6 NEWSFLASH/SUBTITLE DISPLAY CONTROL - auto increments to Register 7

PON	Picture on
TEXT	Text on
COR	Contrast reduction on
BKGND	Background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 DISPLAY MODE - does not auto increment

BOX ON 0	Boxing function allowed on Row 0
BOX ON 1-23	Boxing function allowed on Row 1-23
BOX ON 24	Boxing function allowed on Row 24
DOUBLE HEIGHT	To display double height text
BOTTOM HALF	To select bottom half of page when DOUBLE HEIGHT = 1
REVEAL ON	To reveal concealed text
CURSOR ON	To display cursor
STATUS TOP	Row 25 displayed above or below the main text

R9 CURSOR ROW - auto increments to Register 10

R0 to R4	Active row for data written to or read from memory via the I²C-bus
A0	Selects display memory page (when = 0) or extension packet memory (when = 1)
CLEAR MEM.	When set to 1, clears the display memory. This bit is automatically reset
SUPPL. BLAST	When set to 1, column 4b and 5b (of Table 6) are mapped into 4 and 5 respectively, replacing blast-through alphanumerics in graphics mode

R10 CURSOR COLUMN - auto increments to Register 11 or 11B

C0 to C5	Active column for data written to or read from memory via the I²C-bus
SUPPL. ROW 0	When set to 1, column 4b and 5b (of Table 6) are mapped into columns 6 and 7 respectively, just for row 0 columns 0 to 7
SUPPL. ROW 24	When set to 1, column 4b and 5b (of Table 6) are mapped into columns 6 and 7 respectively just for row 24

R11 CURSOR DATA - does not auto increment

D0 to D6	Data read from/written to memory via I²C, at location pointed to by R9 and R10. This location automatically increments each time R11 is accessed

R11B DEVICE STATUS - does not auto increment

VCS SIGNAL QUALITY	Indicates that the video signal quality is good and PLL is phase locked to input video when = 1
TEXT SIGNAL QUALITY	If a good teletext signal is being received when = 1
ROM VER R0 to R4	Indicated language/ROM variant. For Western European = 01000
$\overline{625}$/525 SYNC	If the input video is a 525 line signal when = 1

Table 3 Register map for page requests (R3)

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

1. Abbreviations are as for Table 1 except for DO CARE bits.
2. When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
3. If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
4. Columns auto-increment on successive I²C-bus transmission bytes.

Table 4 Interlace/non-interlace 312/313 line control (T0 and T1)

T1	T0	RESULT
0	0	interlaced 312.5/312.5 lines
0	1	non-interlaced 312/313 lines (note 1)
1	0	non-interlaced 312/312 lines (note 1)
1	1	scan-locked

Note to Table 4

1 Reverts to interlaced mode if a newsflash or subtitle is being displayed.

Table 5 Crystal characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Crystal (27 MHz, 3rd overtone)					
C1	series capacitance	–	1.7	–	pF
C0	parallel capacitance	–	5.2	–	pF
C_L	load capacitance	–	20	–	pF
Rr	resonant resistance	–	–	50	Ω
R1	series resistance	–	20	–	Ω
Xa	ageing	–	–	±5	10^{-6}/yr
Xj	adjustment tolerance	–	–	±25	10^{-6}
Xd	drift	–	–	±25	10^{-6}

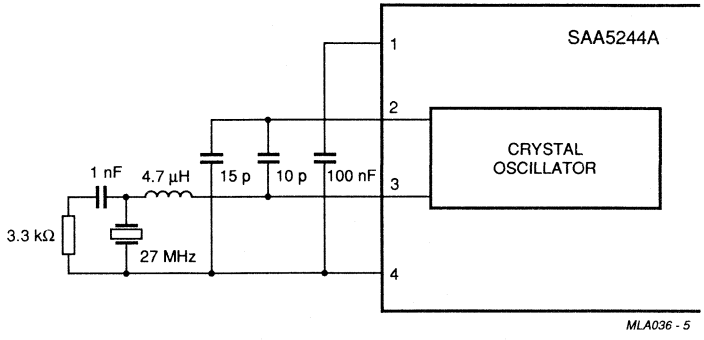


Fig.12 Crystal oscillator application diagram.

CLOCK SYSTEMS

Crystal oscillator

The crystal is a conventional 2-pin design operating at 27 MHz. It is capable of oscillating with both fundamental and third overtone mode crystals. External components should be used to suppress the fundamental output of the third overtone, as shown in Fig.12. The crystal characteristics are given in Table 5.

Character sets

The WST specification allows the selection of national character sets via the page header transmission bits, C12 to C14. The basic 96 character sets differ only in 13 national option characters as indicated in Table 8 with reference to their table position in the basic character matrix illustrated in Table 7. The SAA5244A automatically decodes transmission bits C12 to C14. Table 6 illustrates the character matrixs.

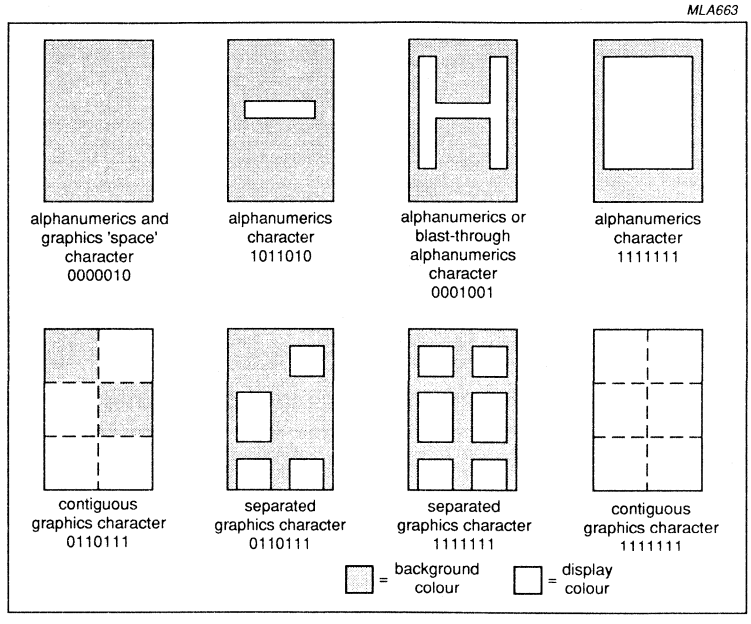
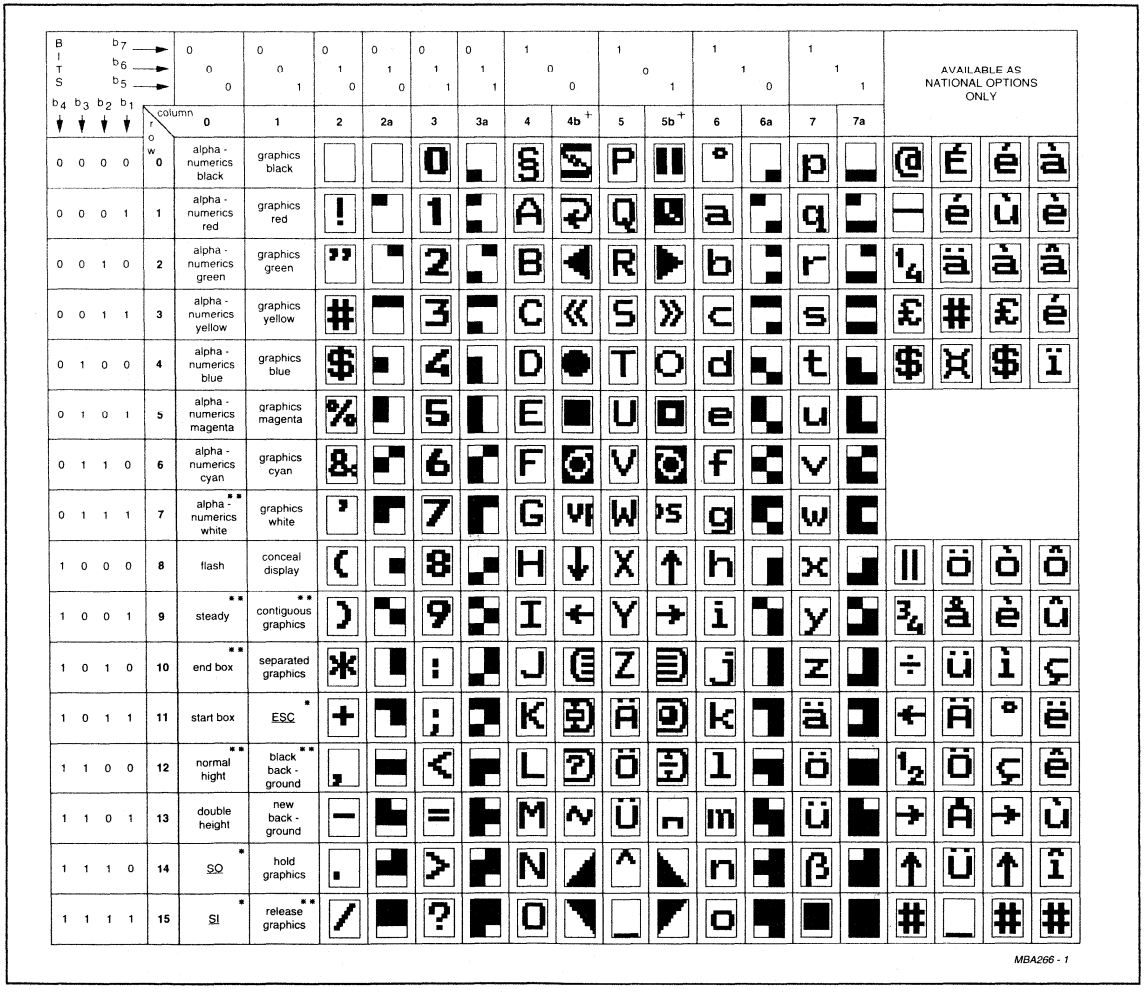


Fig.13 Character format.

Table 6 SAA5244P/A character data input decoding



For character version number (01000) see Register 11B.

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

\+ Columns 4b and 5b can only be accessed when supplementary character bits are set (see Registers 9 and 10).

Notes to Table 6

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Characters may be referred to by column and row, For example 2/5 refers to %.
3. Black represents displayed colour. White represents backgound.
4. Character rectangle shown as follows: 
5. The SAA5244A national option characters are illustrated in Table 8.
6. Characters 4b/11, 4b/12, 5b/10, 5b/11 and 5b/12 are special characters for combining with character 4b/10.
7. National option characters will be developed according to the setting of control bits C12 to C14. These will be mapped into the basic code table into positions shown in Table 8.
8. Columns 4b and 5b are mapped into 4 and 5 respectively (replacing blast-through alphanumerics in the graphics mode) when enabled by R9 bit D7 set to 1.
9. Columns 4b and 5b are mapped into columns 6 and 7 respectively when enabled by R10 bit D6 (row 0 columns 0 to 7) and R10 bit D7 (row 24) set to 1.
10. Columns 2a, 3a, 6a and 7a are displayed in graphics mode.

Table 7 SAA5244A Basic character matrix

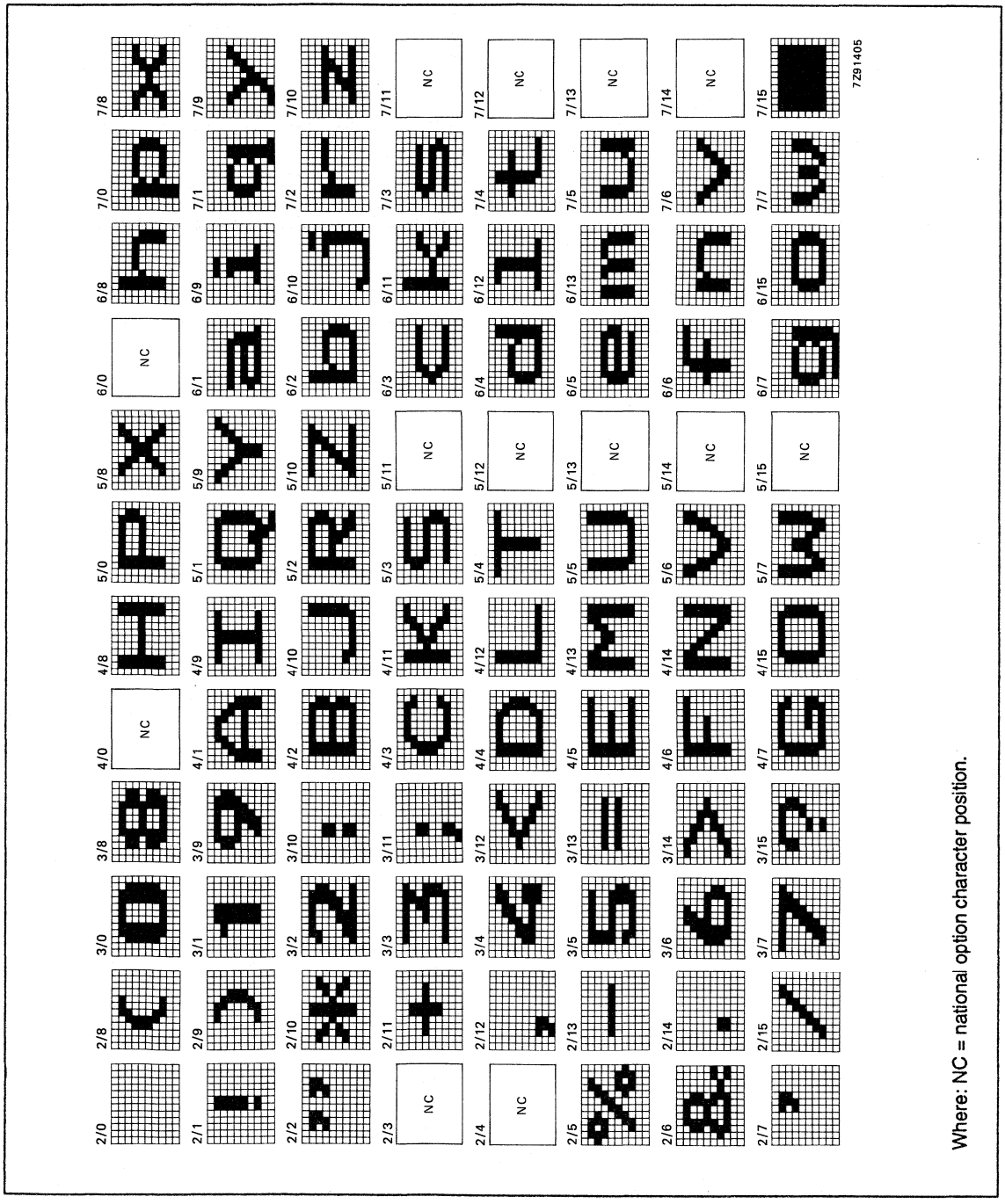


Table 8 SAA5244A national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)													
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç

MLA664

(1) PHCB are the Page Header Control Bits. Other combinations default to English.

ENHANCED COMPUTER CONTROLLED TELETEXT CIRCUIT

(USECCT)

GENERAL DESCRIPTION

The SAA5245 is a MOS N-channel integrated circuit which performs all the digital logic functions of a 525-line World System Teletext decoder. It operates in conjunction with the teletext video processor SAA5231, standard static RAMs and is controlled via the 2-wire I²C-bus The device can be used to provide videotex display conforming to a serial character attribute protocol.

Features

- Microcomputer controlled for flexibility
- High quality flicker-free display using a 12 x 8 character matrix
- Field flyback (lines 5 to 19), or full channel (all lines) data acquisition
- Up to four simultaneous page requests enabling acquisition during one magazine cycle
- Direct interface up to 8 K bytes static RAM
- Automatic language selection of up to seven different languages
- 25th display row for software generated status messages
- Automatic processing of gearing function
- Cursor control for videotex/telesoftware
- 7-bits parity or 8-bit data acquisition
- Extension packet reception option
- Standard I²C-bus slave transceiver (slave address 0010001)
- Single 5 volt power supply
- Mask programmable character sets
- Slave sync mode operation
- Odd/even field output for de-interlaced displays

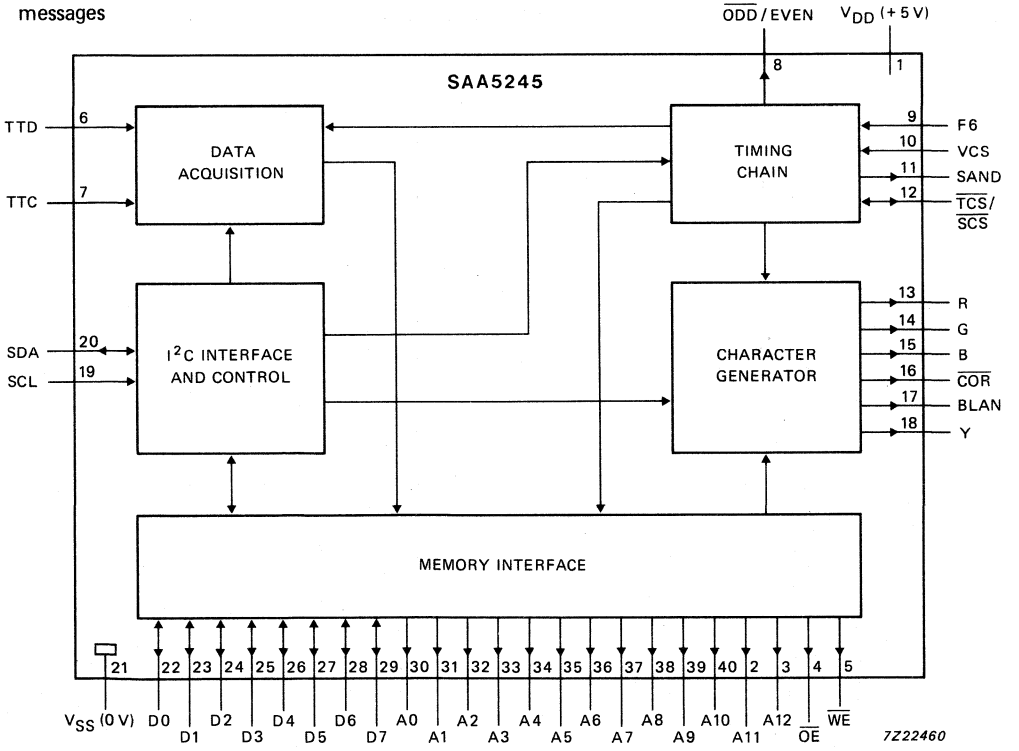


Fig. 1 Block diagram.

PACKAGE OUTLINE

40-lead DIL; plastic (SOT129).

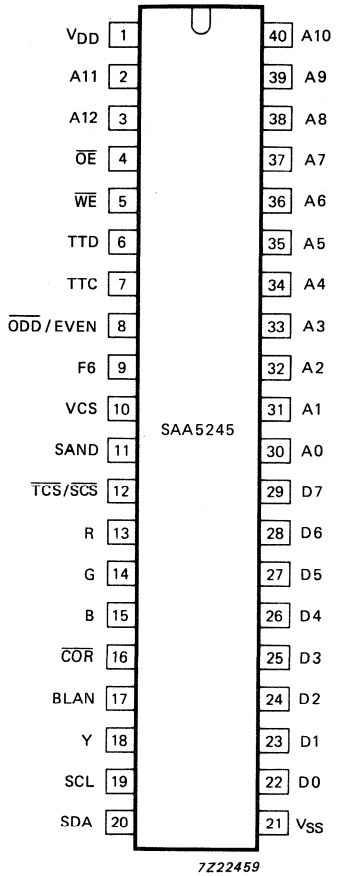


Fig. 2 Pinning diagram.

PINNING

1	V_{DD}	**Power supply**: + 5 V power supply pin.
2, 3, 40	A11, A12, A10	**Chapter Address**: three outputs that select which 1 K byte chapter of external RAM is being accessed for any read or write cycle.
4	$\overline{OE}$	**Output Enable**: active low output signal used to control the reading of the external RAM. It occurs continuously at a 1 MHz rate.
5	$\overline{WE}$	**Write Enable**: active low output signal used to control the writing of data to the external RAM. It occurs for a valid write cycle only and is interleaved with the read cycles.
6	TTD	**Teletext Data**: input from the SAA5231 Video Input Processor (VIP2). It is clamped to V_{SS} for 4 to 8 μs of each television line to maintain the correct DC level following the external AC coupling.

7	TTC	**Teletext Clock**: 5.727 MHz clock input from the SAA5231. It is internally AC coupled to an active clamp input buffer.
8	$\overline{\text{ODD}}$/EVEN	**$\overline{\text{Odd}}$/Even:** for interlaced mode, the output changes once per field at 2 μs before the end of line 1 (263). The output is high for even fields and low for odd fields.
9	F6	**Character display clock:** 6.042 MHz clock input from the SAA5231. It is internally AC coupled to an active clamp input buffer.
10	VCS	**Video Composite Sync:** input from the SAA5231 derived from the incoming video signal. Sync pulses are active high.
11	SAND	**Sandcastle:** 3-level sandcastle output to the SAA5231 containing the phase locking and colour burst blanking information.
12	$\overline{\text{TCS}}$/$\overline{\text{SCS}}$	**Text Composite Sync/Scan Composite Sync:** as an output an active low composite sync waveform (TCS) with interlaced or non-interlaced format (see Fig. 6) which is fed to the SAA5231 to drive the display timebases. Alternatively this pin can act as an input for an active low composite sync waveform (SCS) to 'slave' the display timing circuits.
13, 14, 15	R, G, B	**Red, Green, Blue:** these 3 open drain outputs are the character video signals to the television display circuits. They are active high and contain character and background information.
16	$\overline{\text{COR}}$	**Contrast Reduction:** open drain, active low output which allows selective contrast reduction of the television picture to enhance a mixed mode display.
17	BLAN	**Blanking:** open drain, active high output which controls the blanking of the television picture for a normal text display and for a mixed display.
18	Y	**Character foreground:** open drain, active high video output signal containing all the foreground information displayed on the television screen (e.g. for driving a display printer).
19	SCL	**Serial Clock:** input signal which is the I^2C-bus clock from the microcontroller.
20	SDA	**Serial Data:** is the I^2C-bus data line. It is an input/output function with an open drain output.
21	V_{SS}	**Ground:** 0 volts.
22-29	D0-D7	**8 RAM data lines:** 3-state input/output pins which carry the data bytes to and from the external RAM.
30-39	A0-A9	**RAM address:** 10 output signals that determine which byte location within a 1 K byte chapter of external RAM is accessed for any read or write cycle.

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 1)	V_{DD}	−0.3	+ 7.5	V
Input voltage range				
VCS, SDA, SCL, D0 - D7	V_I	−0.3	+ 7.5	V
TTC, TTD, F6, $\overline{TCS}/\overline{SCS}$	V_I	−0.3	+ 10.0	V
Output voltage range				
SAND, A0 - A12, $\overline{OE}$, $\overline{WE}$, D0 - D7, SDA, $\overline{ODD}$/EVEN				
R, G, B, BLAN, $\overline{COR}$, Y	V_O	−0.3	+ 7.5	V
$\overline{TCS}/\overline{SCS}$	V_O	−0.3	+ 10.0	V
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−20	+ 70	°C

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CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 1)	V_{DD}	4.5	5.0	5.5	V
Supply current (pin 1)	I_{DD}	–	160	270	mA
INPUTS (note 1)					
TTD (note 2)					
External coupling capacitor	C_{ext}	–	–	50	nF
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	2.0	–	7.0	V
Input data rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input data set-up time (note 4)	t_{DS}	40	–	–	ns
Input data hold time (note 4)	t_{DH}	40	–	–	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
TTC; F6 (note 5)					
DC input voltage range	V_I	−0.3	–	+ 10.0	V
AC input voltage (peak-to-peak value) F6	$V_{I(p-p)}$	1.0	–	7.0	V
AC input voltage (peak-to-peak value) TTC	$V_{I(p-p)}$	1.5	–	7.0	V
Input peaks relative to 50% duty cycle	± V_P	0.2	–	3.5	V
TTC clock frequency	f_{TTC}	–	5.727	–	MHz
F6 clock frequency	f_{F6}	–	6.042	–	MHz
Clock rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
VCS					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 5.5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SCL					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.0	–	V_{DD}	V
SCL clock frequency	f_{SCL}	0	–	100	kHz
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5.5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
INPUT/OUTPUTS (note 6)					
$\overline{TCS}$ (output)/$\overline{SCS}$ (input)					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.5	–	10.0	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 0 to 10 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 0.4 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
at I_{OH} = 0.1 mA	V_{OH}	2.4	–	6.0	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SDA (note 7)					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5.5 V with output off	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	0	–	0.5	V
Output fall time between 3.0 V and 1.0 V levels	t_f	–	–	200	ns
Load capacitance	C_L	–	–	400	pF

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
INPUT/OUTPUTS (continued)					
D0-D7 (note 8)					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD}	V
Input leakage current at V_I = 0 V to 5.5 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
OUTPUTS (note 6)					
A0-A12; $\overline{OE}$; $\overline{WE}$ (note 8)					
Output voltage LOW at I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
$\overline{ODD}$/EVEN					
Output voltage LOW at I_{OL} = 0.4 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SAND (note 9)					
Output voltage LOW at I_{OL} = 0.2 mA	V_{OL}	0	–	0.25	V
Output voltage INTERMEDIATE at I_{OL} = ± 10 μA	V_{OI}	1.1	–	3.1	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SAND (continued)					
Output voltage HIGH at I_{OH} = 0 to −10 μA	V_{OH}	4.0	–	V_{DD}	V
Output rise time V_{OL} to V_{OI} between 0.4 V and 0.9 V levels	t_{r1}	–	–	400	ns
Output rise time V_{OI} to V_{OH} between 3.3 V and 3.8 V levels	t_{r2}	–	–	200	ns
Output fall time V_{OH} to V_{OL} between 3.8 V and 0.4 V levels	t_f	–	–	50	ns
Load capacitance	C_L	–	–	30	pF
R; G; B; $\overline{\text{COR}}$; BLAN; Y (note 10)					
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	0	–	0.4	V
Output voltage LOW at I_{OL} = 5 mA	V_{OL}	0	–	1.0	V
Pull-up voltage as seen at pin	V_{PU}	–	–	6.0	V
Output fall time with a load resistor of 1.2 kΩ to 6 V and measured between 5.5 V and 1.5 V	t_f	–	–	20	ns
Skew delay between outputs with a load resistor of 1.2 kΩ to 6 V and measured on the falling edges at 3.5 V	t_{SK}	–	–	20	ns
Load capacitance	C_L	–	–	25	pF
Output leakage current at V_{PU} = 0 to 6 V with output off	I_{LO}	–	–	10	μA
TIMING					
I²C-bus (note 11)					
Clock low period	t_{LOW}	4	–	–	μs
Clock high period	t_{HIGH}	4	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	170	–	–	ns
Stop set-up time from clock high	$t_{SU;STO}$	4	–	–	μs
Start set-up time following a stop	t_{BUF}	4	–	–	μs
Start hold time	$t_{HD;STA}$	4	–	–	μs
Start set-up time following clock low-to-high transition	$t_{SU;STA}$	4	–	–	μs

parameter	symbol	min.	typ.	max.	unit
TIMING (continued)					
Memory interface (note 12)					
Cycle time	t_{CY}	–	495	–	ns
Address change to $\overline{OE}$ LOW	t_{OE}	60	–	–	ns
Address active time	t_{ADDR}	450	495	–	ns
$\overline{OE}$ pulse duration	t_{OEW}	320	–	–	ns
Access time from $\overline{OE}$ to data valid	t_{ACC}	–	–	200	ns
Data hold time from $\overline{OE}$ HIGH or address change	t_{DH}	0	–	–	ns
Address change to $\overline{WE}$ LOW	t_{WE}	40	–	–	ns
$\overline{WE}$ pulse duration	t_{WEW}	200	–	–	ns
Data set-up time to $\overline{WE}$ HIGH	t_{DS}	100	–	–	ns
Data hold time from $\overline{WE}$ HIGH	t_{DHWE}	20	–	–	ns
Write recovery time	t_{WR}	25	–	–	ns
QUALITY (note 13)					
Failure rate					
Failure rate at T_{amb} = 55 °C (1×10^{-6} failures per hour)		–	–	1000	FITS

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Notes to the characteristics

1. All inputs are protected against static charge under normal handling.
2. The TTD input incorporates an internal clamping diode in addition to the active clamping transistor (see Fig. 3).
3. Rise and fall times between 10% and 90% levels.
4. Teletext input data set-up and hold times are with respect to a 50% duty cycle level of the rising edge of the teletext clock input (TTC). Data stable 1 $\geqslant$ 2.0 V; data stable 0 $\leqslant$ 0.8 V (see Fig. 4).
5. The TTC and F6 inputs have internal clamping diodes and are AC coupled (see Fig. 3).
6. All outputs and input/outputs are protected against static charge under normal handling and connection to V_{DD} and V_{SS}.
7. For details of I^2C-bus timing see Fig. 8.
8. For details of RAM timing see Fig. 9.
9. For details of synchronization timing see Fig. 5.
10. For details of display output timing see Fig. 7.
11. The I^2C-bus timings are referred to V_{IH} = 3 V and V_{IL} = 1.5 V. For waveforms see Fig. 8.
12. The memory interface timings are referred to V_{IL} = 1.5 V. For waveforms see Fig. 9.
13. This device shall meet the requirements of the Elcoma General Quality and Specification for ICs: URV - 4 - 2 - 59/601 (LSI).

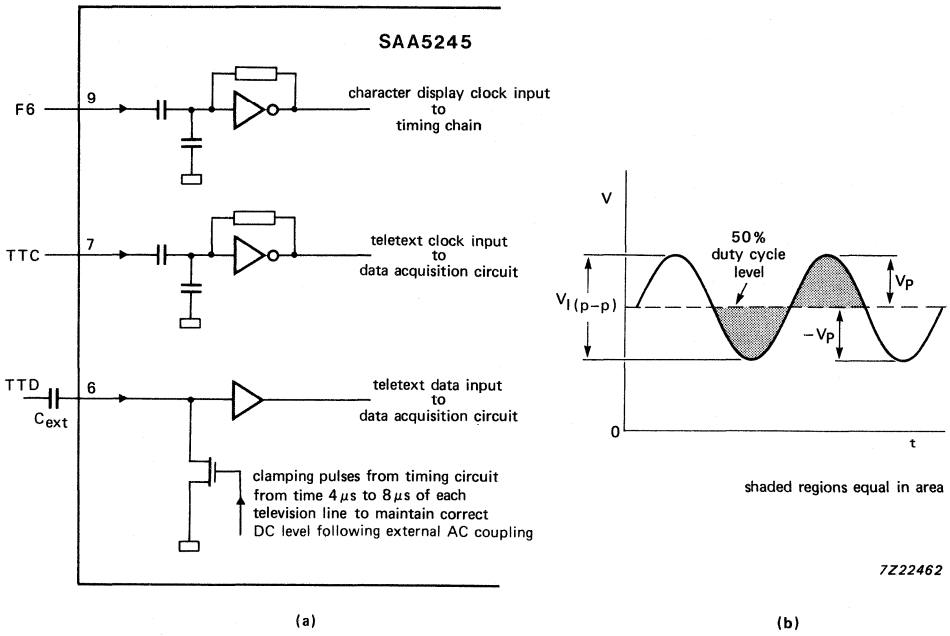
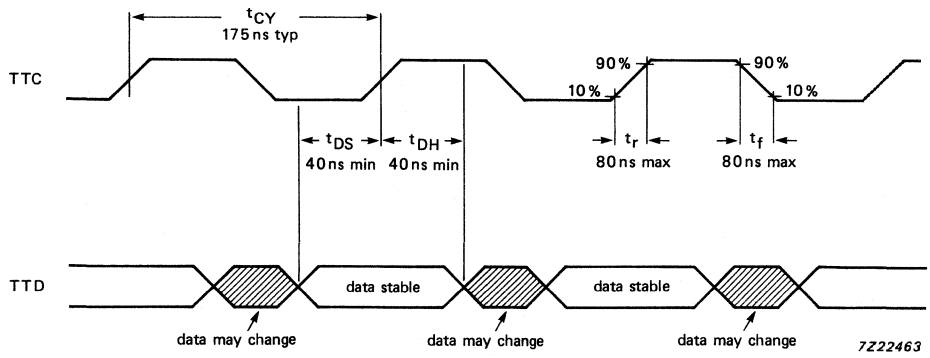


Fig. 3 (a) F6, TTC and TTD input circuitry (b) input waveform parameters.



Data stable: 1 is $\geqslant$ 2.0 V; 0 is $\leqslant$ 0.8 V.

Fig. 4 Teletext data input timing.

DEVELOPMENT DATA

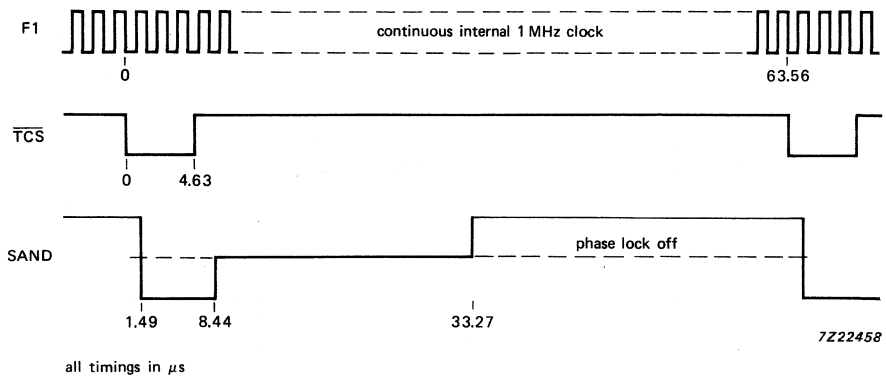
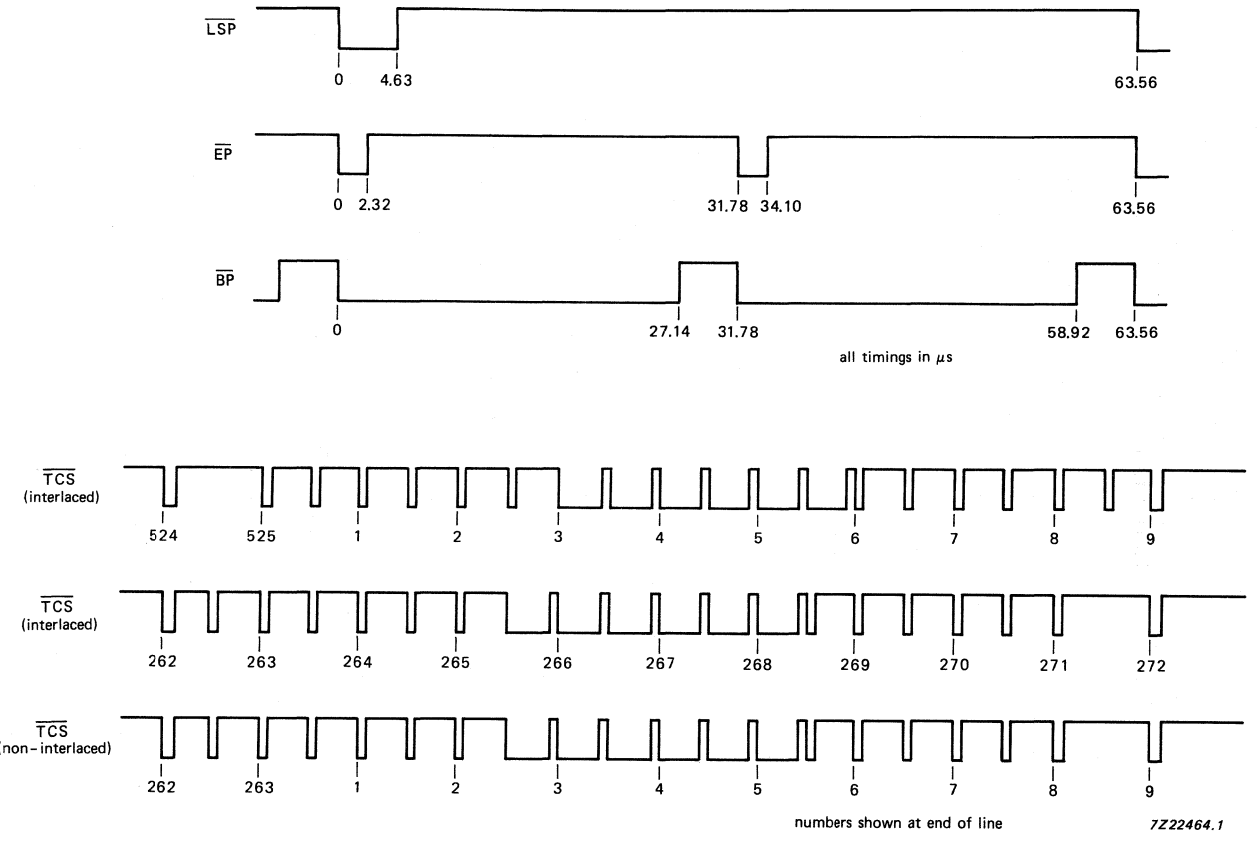


Fig. 5 Synchronization timing.



Line sync pulses ($\overline{\text{LSP}}$), equalizing pulses ($\overline{\text{EP}}$) and broad pulses ($\overline{\text{BP}}$) are combined to provide the text composite sync waveform ($\overline{\text{TCS}}$) as shown. All timings measured from falling edge of $\overline{\text{LSP}}$ with a tolerance of ± 100 ns.

Fig. 6 Composite sync waveforms (525-line version).

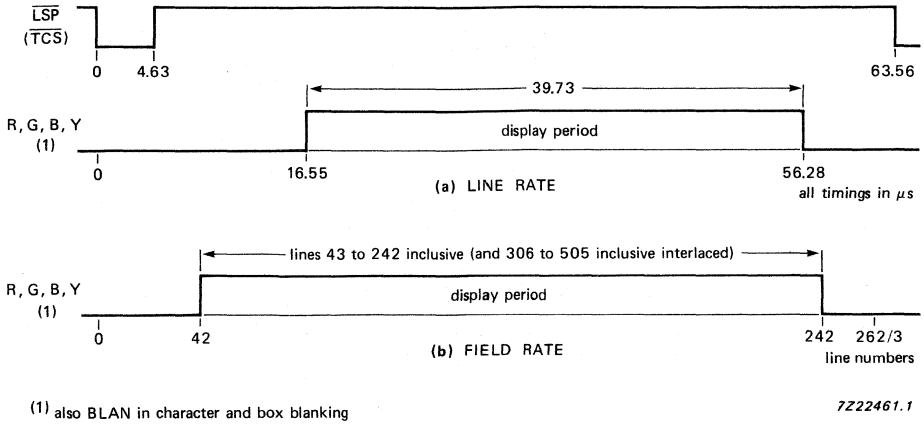


Fig. 7 Display output timing (a) line rate (b) field rate.

DEVELOPMENT DATA

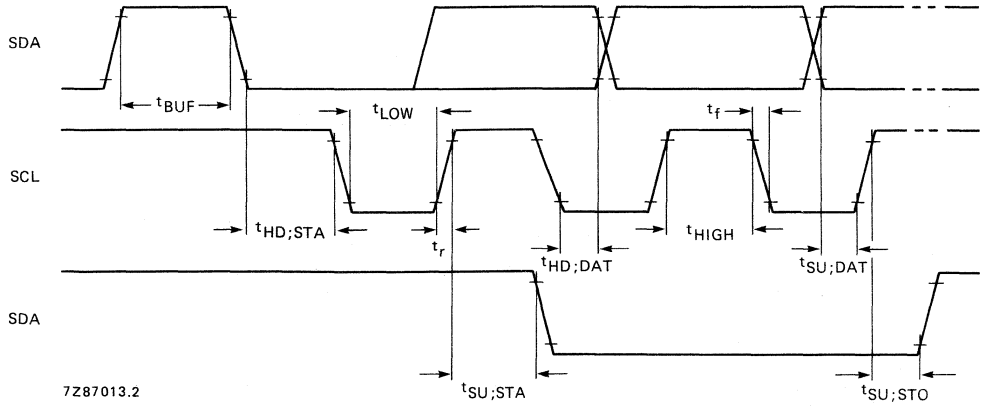


Fig. 8 I²C-bus timing.

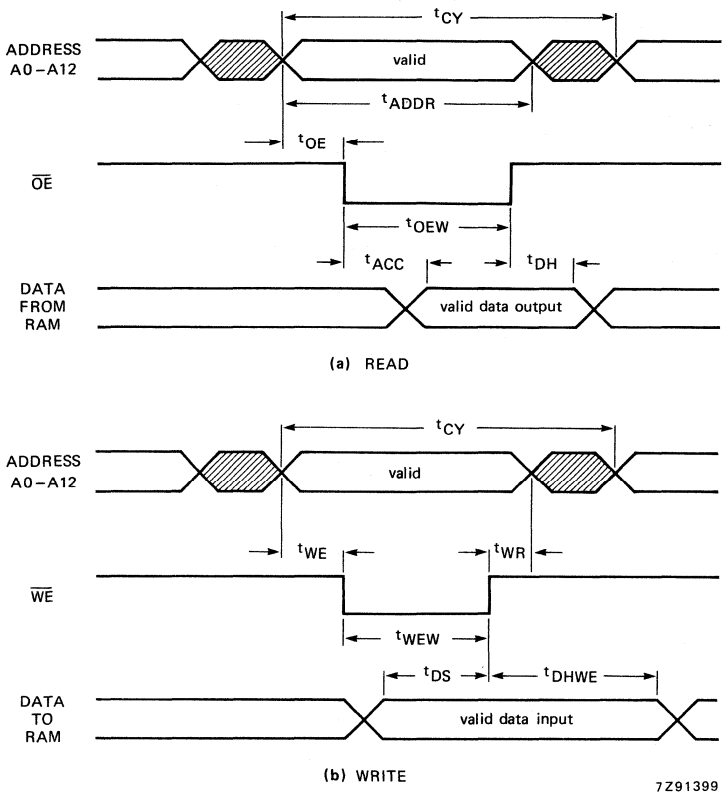


Fig. 9 Memory interface timing (a) read (b) write.

DEVELOPMENT DATA

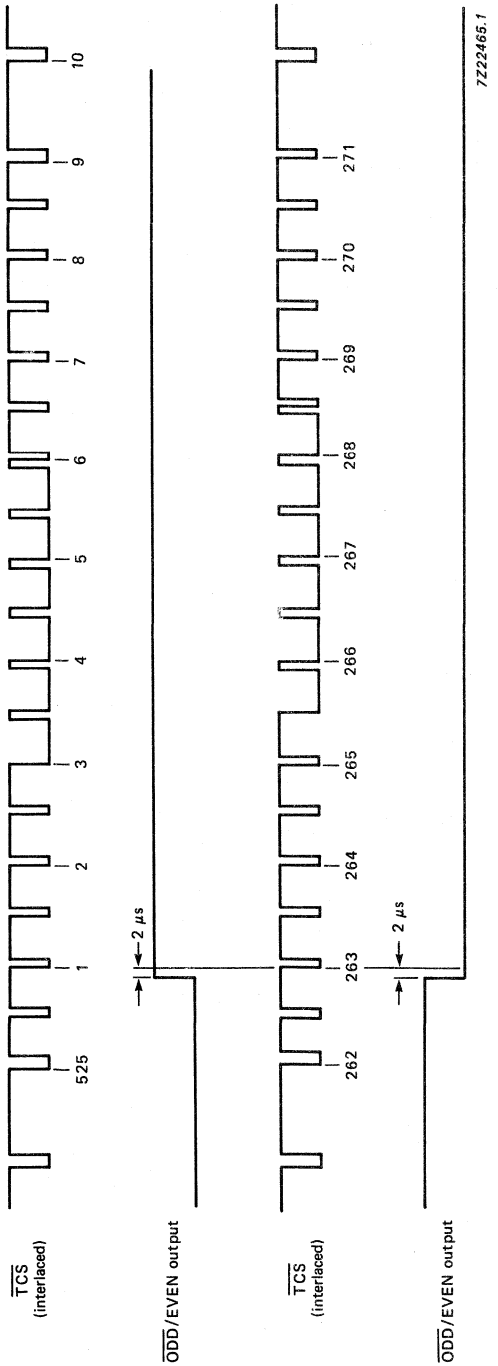


Fig. 10 $\overline{\text{ODD}}$/EVEN timing diagram.

APPLICATION INFORMATION

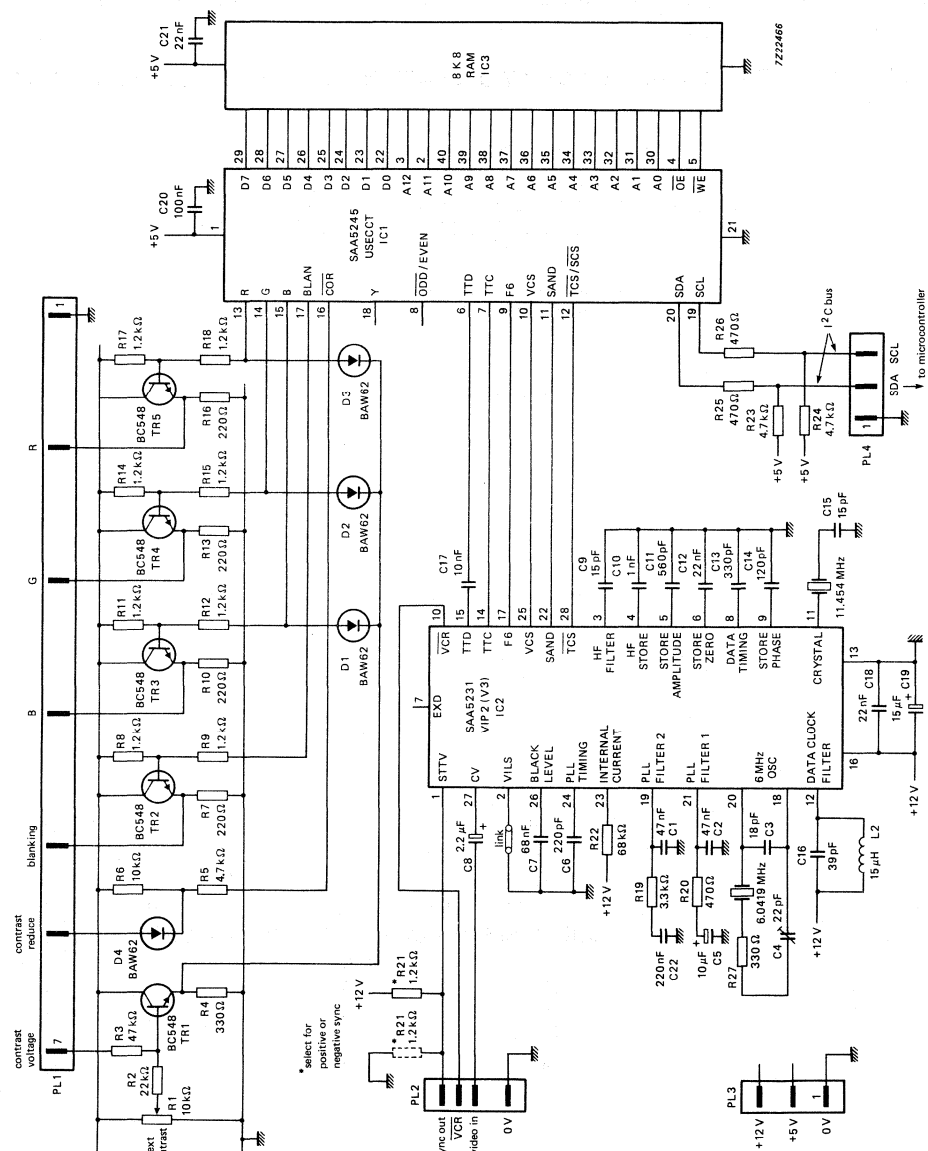


Fig. 11 USECCT based multi-page decoder circuit diagram.

USECCT page memory organization

The organization of a page memory is shown in Fig. 12. The USECCT provides an additional row compared with first generation decoders bringing the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page as broadcast and row 24 is the extra row available for user-generated status messages.

A MORE DETAILED DESCRIPTION OF USECCT OPERATION AND APPLICATION IS AVAILABLE ON REQUEST.

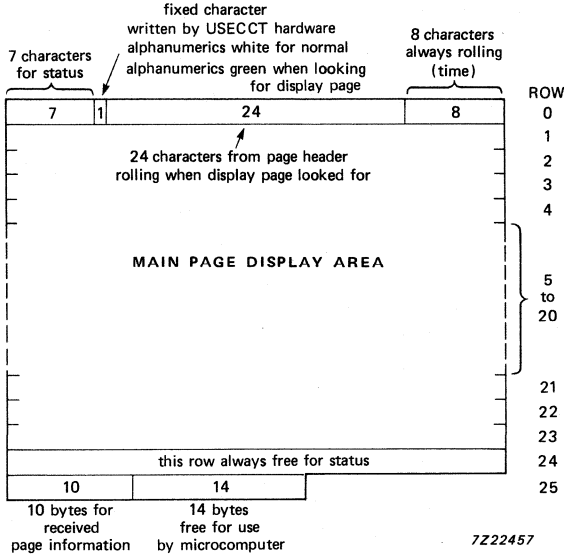


Fig. 12 Page memory organization.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	0	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

MAG	magazine	page number	MU	minutes units	page sub-code
PU	page units		MT	minutes tens	
PT	page tens		HU	hours units	
PBLF	page being looked for		HT	hours tens	
$\overline{\text{FOUND}}$	LOW for page has been found		C4-C14	transmitted control bits	
HAM.ER	Hamming error in corresponding byte				

APPLICATION INFORMATION (continued)

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by USECCT to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of row 25 contain control data relating to the received page. Seven digits are used to identify a page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

Register maps

USECCT mode registers R1 to R11 are shown in Table 2. R1 to R10 are WRITE only; R11 is READ/WRITE.
Register map (R3), for page requests, is shown in detail in Table 3.

Table 2 USECCT register map

		D7	D6	D5	D4	D3	D2	D1	D0
Operating mode	R1	TA	$\overline{7+P}$/ 8 BIT	ACQ. $\overline{ON}$/OFF	EXTENSION PACKET ENABLE	$\overline{DEW}$/ FULL FIELD	TCS ON	T1	T0
Page request address	R2	–	BANK SELECT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request data	R3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
Display chapter	R4	–	–	–	–	–	A2	A1	A0
Display control (normal)	R5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash/subtitle)	R6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	R7	STATUS ROW $\overline{BTM}$/TOP	CURSOR ON	$\overline{CONCEAL}$/ REVEAL	$\overline{TOP}$/ BOTTOM	$\overline{SINGLE}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0
Active chapter	R8	–	–	–	–	CLEAR MEM.	A2	A1	A0
Active row	R9	–	–	–	R4	R3	R2	R1	R0
Active column	R10	–	–	C5	C4	C3	C2	C1	C0
Active data	R11	D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)

–bit does not exist

DEVELOPMENT DATA

Notes to Table 2

The arrows shown on the right of the register map indicate that the register auto-increments to the next one on the following I^2C transmission byte. TA and TB must be logic 0 for normal operation.
All bits in registers R1 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R5 and R6 which are set to logic 1.
All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha white' (00000111) as the acquisition circuit is enabled but all pages are on hold.

Where:

R1 Mode	
T0, T1	interlace/non-interlace 262/263 line control
TCS ON	text composite sync or direct sync select
$\overline{\text{DEW}}$/FULL FIELD	field-flyback or full channel mode
$\overline{7+P}$/8 BIT	7 bits with parity checking or 8-bit mode
TA, TB	test bits; 0 for normal operation
R2 Page request address	
START COLUMN	start column for page request data
ACQ CCT	selects one of four acquisition circuits
BANK SELECT	selects bank of four pages being addressed for acquisition
R3 Page request data	see Table 3
R4 Display chapter	determines which of the 8 pages is displayed
R5, R6 Display control	for normal and newsflash/subtitle
PON	picture on
TEXT	text on
COR	contrast reduction on
BKGND	background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 Display mode	
BOX ON 0 (1-23, 24)	boxing function allowed on row 0 (row 1-23, 24)
STATUS ROW $\overline{\text{BTM}}$/TOP	row 25 displayed above or below the main text
R8 to R11	active chapter, row, column and data information written to or read from page memory via the I^2C-bus

APPLICATION INFORMATION (continued)

Table 3 Register map for page requests (R3)

Start Column	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	X	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

Abbreviations are as for Table 1 except for D0 CARE bits.
When the D0 CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the D0 CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
There are four groups of data shown in Table 3, one for each acquisition circuit (four simultaneous page requests).
Columns auto-increment on successive I^2C transmission bytes.

CHARACTER SETS

The US teletext specification allows the selection of national character sets via the page header transmission bits, C12 to C14 as shown in Table 4.
USECCT automatically decodes transmission bits C12 to C14. Other combinations of C12 to C14 are defaulted to English in SAA5245P/A. With 8-bit decoding the character matrices are shown in Table 5.

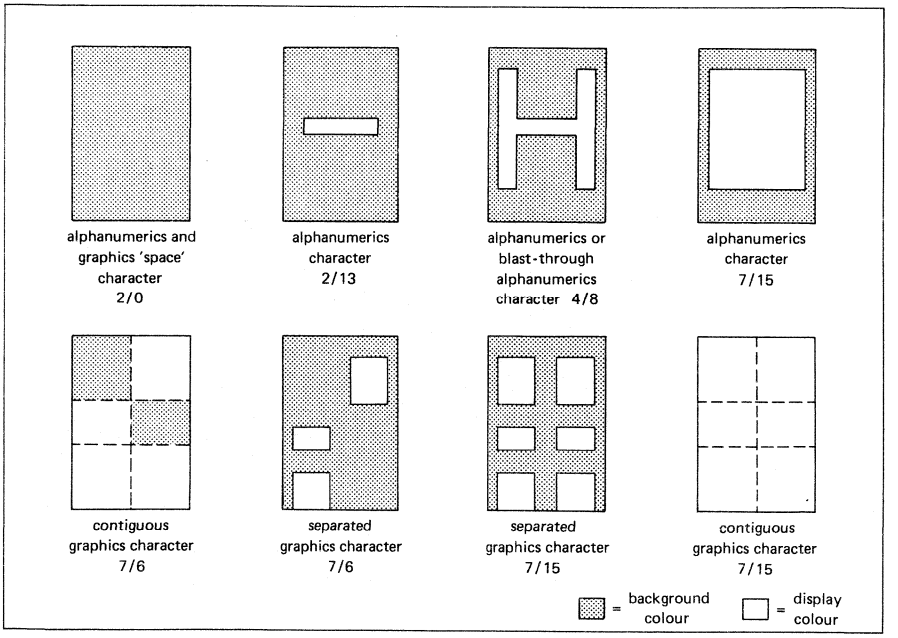
Table 4 Selection of national character sets (SAA5245P/A)

PHCB	ENGLISH	GERMAN	SWEDISH	ITALIAN	FRENCH	SPANISH
C12	0	0	0	0	1	1
C13	0	0	1	1	0	0
C14	0	1	0	1	0	1

Where:

PHCB page header control bits.

DEVELOPMENT DATA



Character bytes are listed as transmitted from b_1 to b_7.

Fig. 13 Character format.

APPLICATION INFORMATION (continued)

Table 5 Character data input decoding (SAA5245A).

BITS b8	0	0	0 or 1	0 or 1	0	0	0	0	1	1	1	1	1	1
b7	0	0	0	1	1	1	1	1	0	0	1	1	1	1
b6	0	0	1	0	0	1	1	1	0	0	0	1	1	1
b5	0	1	0	1	0	1	0	1	0	1	0	1	0	1
b4 b3 b2 b1 \ column / row	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha–numerics black	graphics black															
0 0 0 1	1	alpha–numerics red	graphics red															
0 0 1 0	2	alpha–numerics green	graphics green															
0 0 1 1	3	alpha–numerics yellow	graphics yellow															
0 1 0 0	4	alpha–numerics blue	graphics blue															
0 1 0 1	5	alpha–numerics magenta	graphics magenta															
0 1 1 0	6	alpha numerics cyan	graphics cyan															
0 1 1 1	7	alpha–numerics white **	graphics white															
1 0 0 0	8	flash	conceal display															
1 0 0 1	9	steady **	contiguous graphics **															
1 0 1 0	10	end box **	separated graphics															
1 0 1 1	11	start box	ESC *															
1 1 0 0	12	normal height **	black back–ground **															
1 1 0 1	13	double height	new back–ground															
1 1 1 0	14	SO *	hold graphics															
1 1 1 1	15	SI *	release graphics **															

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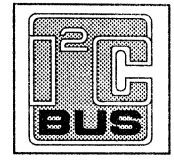
Notes to Table 5

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Codes may be referred to by column and row. For example 2/5 refers to %.
3. Black represents displayed colour. White represents background.
4. Character rectangle shown as follows: □
5. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters to combine with character 8/5.
6. With bit 8 = 0 national option characters will be decoded according to the setting of control bits C12 to C14 (see Table 4).

* These control characters are reserved for compatibility with other data codes.
** These control characters are presumed before each row begins.

Integrated VIP and Teletext (IVT1.0)

SAA5246A



QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	64	128	mA
V_{syn}	sync amplitude	0.1	0.3	0.6	V
V_{vid}	video amplitude	0.7	1.0	1.4	V
f_{XTAL}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature range	–20	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5246AP/E	48	DIL	plastic	SOT240
SAA5246AZP/E	52	SDIL	plastic	SOT247
SAA5246AGP/E	64	QFP	plastic	SOT208

FEATURES

- Complete Teletext and VPS decoder in a 48-pin DIL, 52-pin shrink DIL, or 64-pin QFP, integrated circuit
- Single +5 V power supply
- Both video and scan related synchronization modes are supported
- RGB interface to standard colour decoder ICs, push-pull output drive
- Digital data slicer and display clock phase-locked loop reduce peripheral components to a minimum
- Data capture performance similar to SAA5231 (VIP2)
- Option for up to seven national languages
- Optional storage of packet 24 in the display memory
- Separate text and video signal quality detectors, 625/525 video status and language version all readable via I²C-bus
- Automatic $\overline{\text{ODD}}$/EVEN output control with override
- Control of display PLL free-run and rolling header via I²C-bus
- VCS to SCS mode for stable 525 line status display

DESCRIPTION

The SAA5246A is a single-chip teletext decoder IC for decoding 625 line base World System Teletext transmissions. The teletext decoder hardware is based on the Enhanced Computer Controlled ECCT device (SAA5243) with some additional features.
The Video Input Processor section of the device uses mixed analog and digital designs in the data slicer and clock phase-locked-loop functions. As a result the number of external components are greatly reduced and no critical or adjustable components are required.

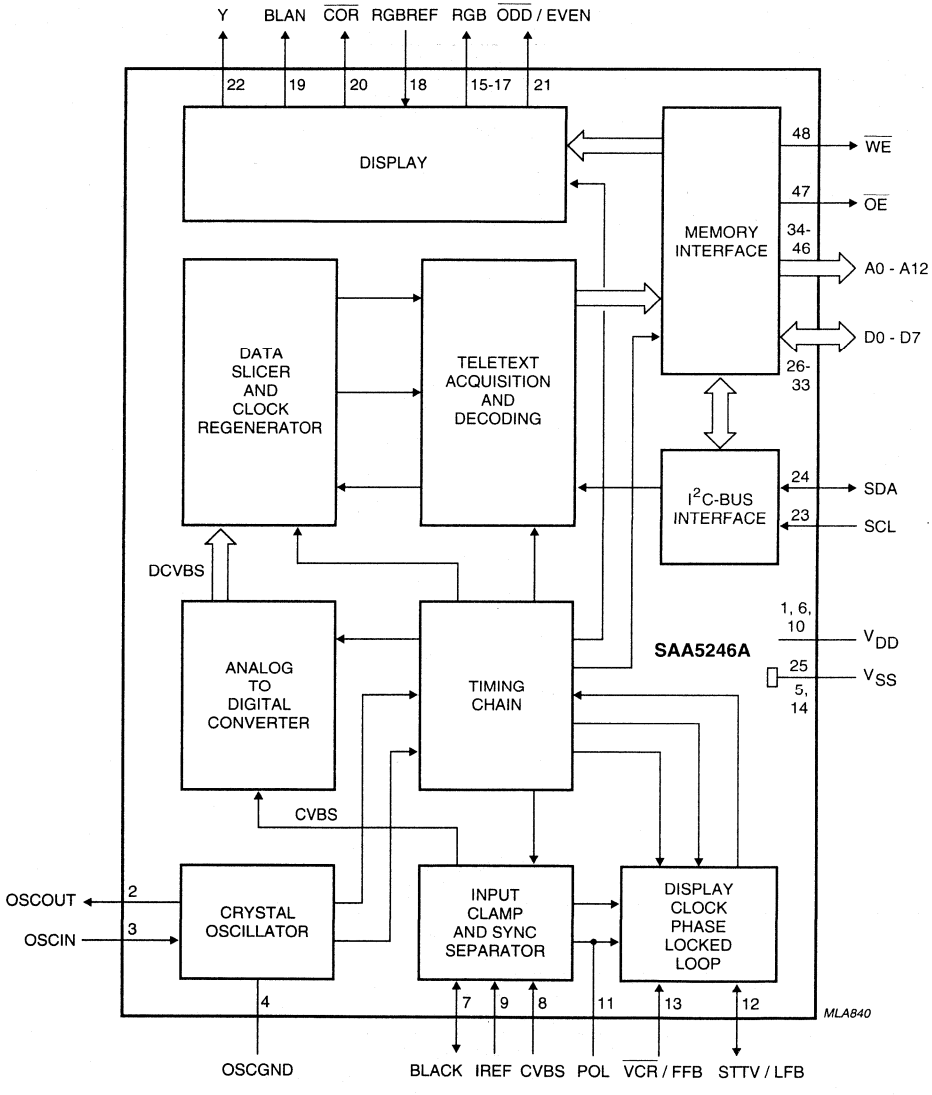


Fig.1 Block diagram for SOT240 (DIL48) package.

PINNING

SYMBOL	PIN			DESCRIPTION
	SOT240	SOT247	SOT208	
OSCOUT	2	1	27	27 MHz crystal oscillator output
OSCIN	3	2	28	27 MHz crystal oscillator input
OSCGND	4	3	29	0 V crystal oscillator ground
V_{SS}	5, 14, 25	4, 5, 15, 26	26, 30, 31, 43, 58	0 V ground
n.c.	-	7	-	not connected
BLACK	7	8	35	video black level storage pin, connected to ground via a 100 nF capacitor
CVBS	8	9	36	composite video input pin. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor
IREF	9	10	37	reference current input pin, connected to ground via a 27 kΩ resistor
V_{DD}	1, 6, 10	6, 11, 52	25, 32, 38	+5 V positive supply
POL	11	12	39	STTV/LFB/FFB polarity selection pin
STTV/LFB	12	13	40	sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode)
$\overline{VCR}$/FFB	13	14	42	PLL time constant switch/field input pin. Function controlled by an internal register bit (scan sync mode)
R	15	16	44	dot rate character output of the RED colour information
G	16	17	45	dot rate character output of the GREEN colour information
B	17	18	47	dot rate character output of the BLUE colour information
RGBREF	18	19	48	input DC voltage to define the output high level on the RGB pins
BLAN	19	20	52	dot rate fast blanking output
$\overline{COR}$	20	21	53	programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages. Open-drain output
$\overline{ODD}$/EVEN	21	22	54	In $\overline{ODD}$/EVEN mode a 25 MHz output synchronized to the input CVBS field sync pulses to make a non-interlaced display by adjustment of the vertical deflection currents.
Y	22	23	55	dot rate character output of teletext foreground colour information. Open-drain output
SCL	23	24	56	serial clock input for I²C-bus. It can still be driven HIGH during power-down of the device
SDA	24	25	57	serial data port for the I²C-bus. Open drain output. It can still be driven HIGH during power-down of the device
D0-D5	26-31	27-32	60 - 64, 3	data ports for the page RAM

SYMBOL	PIN			DESCRIPTION
	SOT240	SOT247	SOT208	
n.c.	-	33, 34	1, 2, 10, 11, 15, 18, 33, 34, 41, 46, 49 - 51, 59	not connected
D6-D7	32, 33	35, 36	4, 5	data ports for the page RAM
A0-A12	34-46	37-49	6-9, 12-14, 16, 17, 19-22	address output for the page SRAM
$\overline{OE}$	47	50	23	output enable for the page SRAM
$\overline{WE}$	48	51	24	write enable for the page SRAM

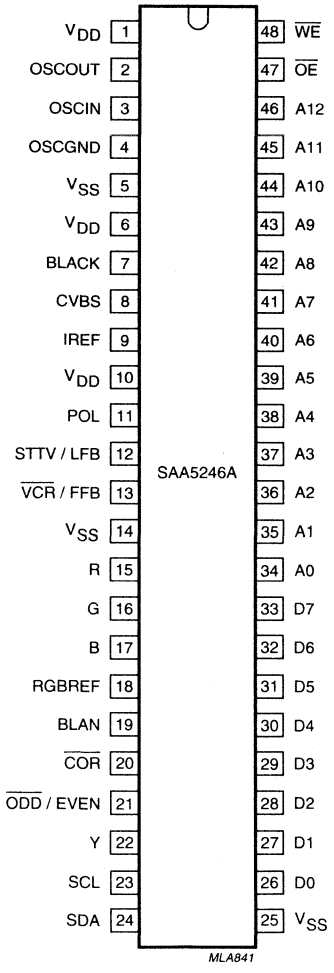


Fig.2 Pin configuration; SOT240 (DIL48).

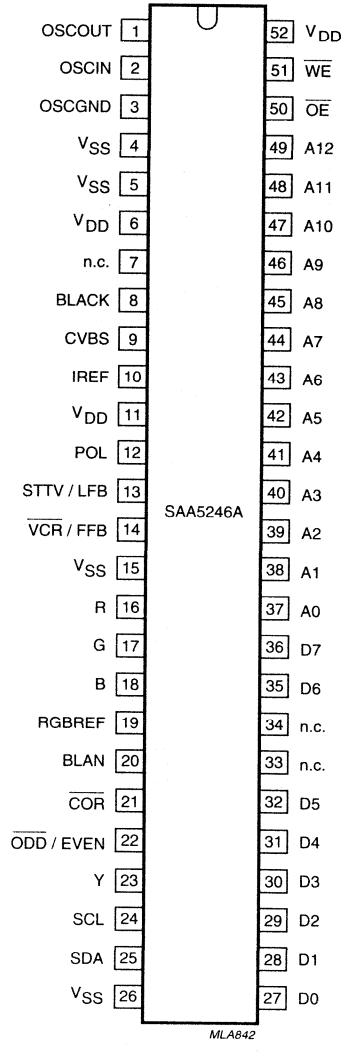


Fig.3 Pin configuration; SOT247 (SDIL52).

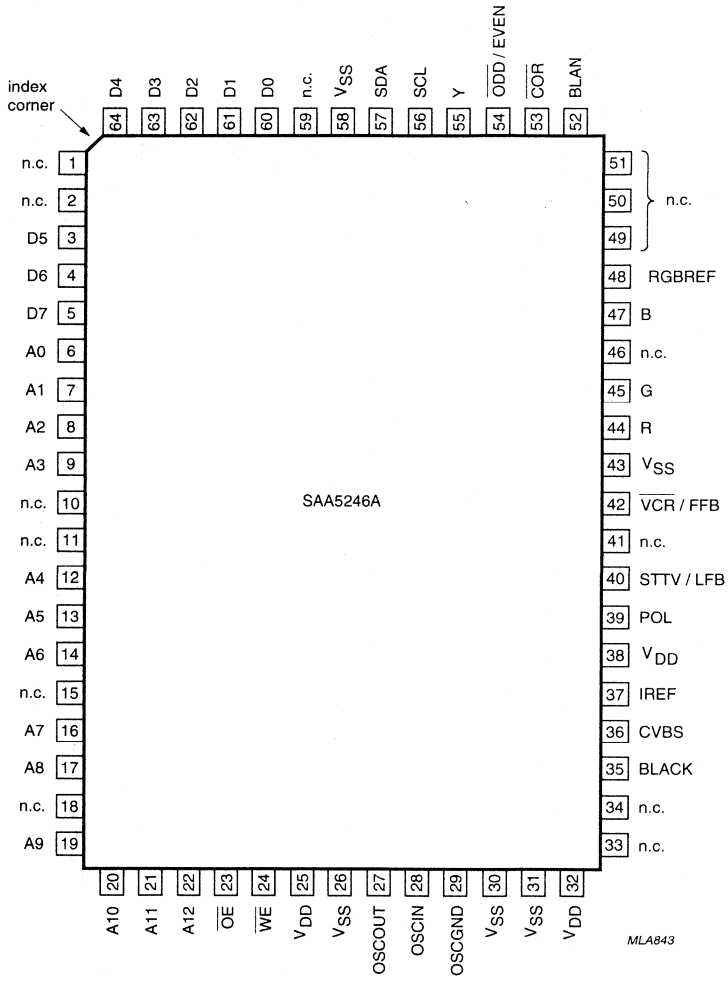


Fig.4 Pin configuration; SOT208 (QFP64).

LIMITING VALUES

In accordance with Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	−0.3	6.5	V
V_I	input voltage (any input)	−0.3	V_{DD} +0.5	V
V_O	output voltage (any output)	−0.3	V_{DD} +0.5	V
I_O	output current (each output)	−	±10	mA
I_{IOK}	DC input or output diode current	−	±20	mA
T_{amb}	operating ambient temperature range	−20	+70	°C
T_{stg}	storage temperature range	−55	+125	°C
V_{stat}	electrostatic handling (see note)	−2000	+2000	V

Note

Electrostatic handling is equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor with a 15 ns rise time.

Failure Rate

The failure rate at T_{amb} = 55 °C will be a maximum of 1000 FITS (1 FIT = 1 x 10^{-9} failures per hour).

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = −20 to +70 °C, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage range		4.5	5.0	5.5	V
I_{DD}	total supply current		–	64	120	mA
Inputs						
CVBS						
V_{syn}	sync amplitude		0.1	0.3	0.6	V
t_{syn}	delay from CVBS to TCS output from STTV buffer (nominal video, average of leading/trailing edge)		−150	0	+150	ns
t_{syd}	change in sync delay between all black and all white video input at nominal levels		0	–	25	ns
$V_{vid(p-p)}$	video input amplitude (peak-to-peak)		0.7	1.0	1.4	V
	display PLL catching range		±7	–	–	%
Z_{src}	source impedance		–	–	250	Ω
C_I	input capacitance		–	–	10	pF
IREF						
R_g	resistor to ground		–	27	–	kΩ
POL						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
LFB						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
I_I	input current	note 1	−1	–	+1	mA
t_{LFB}	delay between LFB front edge and input video line sync		–	250	–	ns
$\overline{VCR}$/FFB						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
I_I	input current	note 1	−1	–	+1	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGBREF						
V_{IL}	LOW level input voltage		−0.3	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
I_{DC}	DC current		–	–	10	mA
SCL						
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
f_{SCL}	clock frequency		0	–	100	kHz
t_r	input rise time	10% to 90%	–	–	2	µs
t_f	input fall time	90% to 10%	–	–	2	µs
C_I	input capacitance		–	–	10	pF
Inputs/outputs						
CRYSTAL OSCILLATOR (OSCIN; OSCOUT)						
f_{XTAL}	crystal frequency		–	27	–	MHz
V_{OSC}	oscillation amplitude (peak-to-peak value)		–	1.5	–	V
G_v	small signal voltage gain		–	1	–	V/V
G_m	mutual conductance		5	–	–	mA/V
C_I	input capacitance		–	–	10	pF
C_{FB}	feedback capacitance		–	1	–	pF
BLACK						
C_{blk}	storage capacitor to ground		–	100	–	nF
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
SDA						
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
t_r	input rise time	10% to 90%	–	–	2	µs
t_f	input fall time	90% to 10%	–	–	2	µs
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.5	V
t_f	output fall time	3 V to 1 V	–	–	200	ns
C_L	load capacitance		–	–	400	pF
D0 TO D7						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current		−10	–	+10	µA
C_I	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA	2.4	–	V_{DD}	V
t_r	output rise time	0.6 V to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 V to 0.6 V	–	–	50	ns
C_L	load capacitance		–	–	120	pF
Outputs						
STTV						
G_{stt}	gain of STTV relative to video input		0.9	1.0	1.1	
V_{tcs}	TCS amplitude		0.2	0.3	0.45	V
V_{DCs}	DC shift between TCS output and nominal video output		–	–	0.15	V
I_O	output drive current		–	–	3.0	mA
C_L	load capacitance		–	–	100	pF
A0 TO A12 ADDRESS OUTPUT TO MEMORY						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 V to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 V to 0.6 V	–	–	50	ns
$\overline{OE}$, $\overline{WE}$						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 V to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 V to 0.6 V	–	–	50	ns
R, G AND B						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.2	V
V_{OH}	HIGH level output voltage	I_{OH} = –1.6 mA; RGBREF ≤ V_{DD}–2 V	RGBREF –0.25 V	RGBREF	RGBREF +0.25 V	V
I_{DC}	DC current		–	–	–3.3	mA
$\lvert Z_o \rvert$	output impedance		–	–	200	Ω
C_L	load capacitance		–	–	50	pF
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
BLAN						
V_{OL}	LOW level output voltage	I_{OL} = 0.2 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA; V_{DD} = 4.5 V	1.1	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OH}	HIGH level output voltage	I_{OH} = 0 mA; V_{DD} = 5.5 V	–	–	2.8	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
$\overline{ODD}$/EVEN						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −1.6 mA	V_{DD}−0.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
$\overline{COR}$ AND Y (OPEN DRAIN)						
V_{OH}	pull-up voltage at pin		–	–	V_{DD}	V
V_{OL}	LOW level output voltage	I_{OL} = +2 mA	0	–	0.4	V
V_{OL}	LOW level output voltage	I_{OL} = +5 mA	0	–	1.0	V
C_L	load capacitance		–	–	25	pF
t_f	output fall time	load resistor of 1.2 kΩ to V_{DD}; measured between V_{DD} −0.5 and 1.5 V	–	–	50	ns
I_{LO}	output leakage current	V_I = 0 to V_{DD}	−10	–	+10	μA
T_{SK}	skew delay between display outputs R, G, B, $\overline{COR}$, Y and BLAN		–	–	20	ns
Timing						
MEMORY INTERFACE						
t_{CY}	cycle time		–	500	–	ns
t_{OE}	address change to $\overline{OE}$ LOW		55	–	–	ns
t_{ADDR}	address active time		450	500	–	ns
t_{rOEW}	$\overline{OE}$ pulse width read		295	–	–	ns
t_{wOEW}	$\overline{OE}$ pulse width write		100	–	–	ns
t_{ACC}	access time from address data valid		–	–	150	ns
t_{DH}	data hold time from $\overline{OE}$ HIGH or address change		0	–	150	ns
t_{WEW}	$\overline{WE}$ pulse width		100	–	–	ns
t_{DS}	data set-up time to $\overline{WE}$ HIGH		60	–	–	ns
t_{DHWE}	data hold time from $\overline{WE}$ HIGH		20	–	–	ns
t_{WR}	write recovery time		20	–	–	ns
t_{DE}	data enable from $\overline{WE}$ LOW		60	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-BUS						
t_{LOW}	clock LOW period		4	–	–	µs
t_{HIGH}	clock HIGH period		4	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		170	–	–	ns
$t_{SU;STO}$	set-up time from clock HIGH to STOP		4	–	–	µs
t_{BUF}	START set-up time following a STOP		4	–	–	µs
$t_{HD;STA}$	START hold time		4	–	–	µs
$t_{SU;STA}$	START set-up time following clock LOW-to-HIGH transition		4	–	–	µs

Notes to the characteristics

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. Series current limiting resistors must be used to limit the input currents to ± 1 mA.
2. Can be pulled higher by external pull-up resistor, (maximum leakage current ≈200 µA).

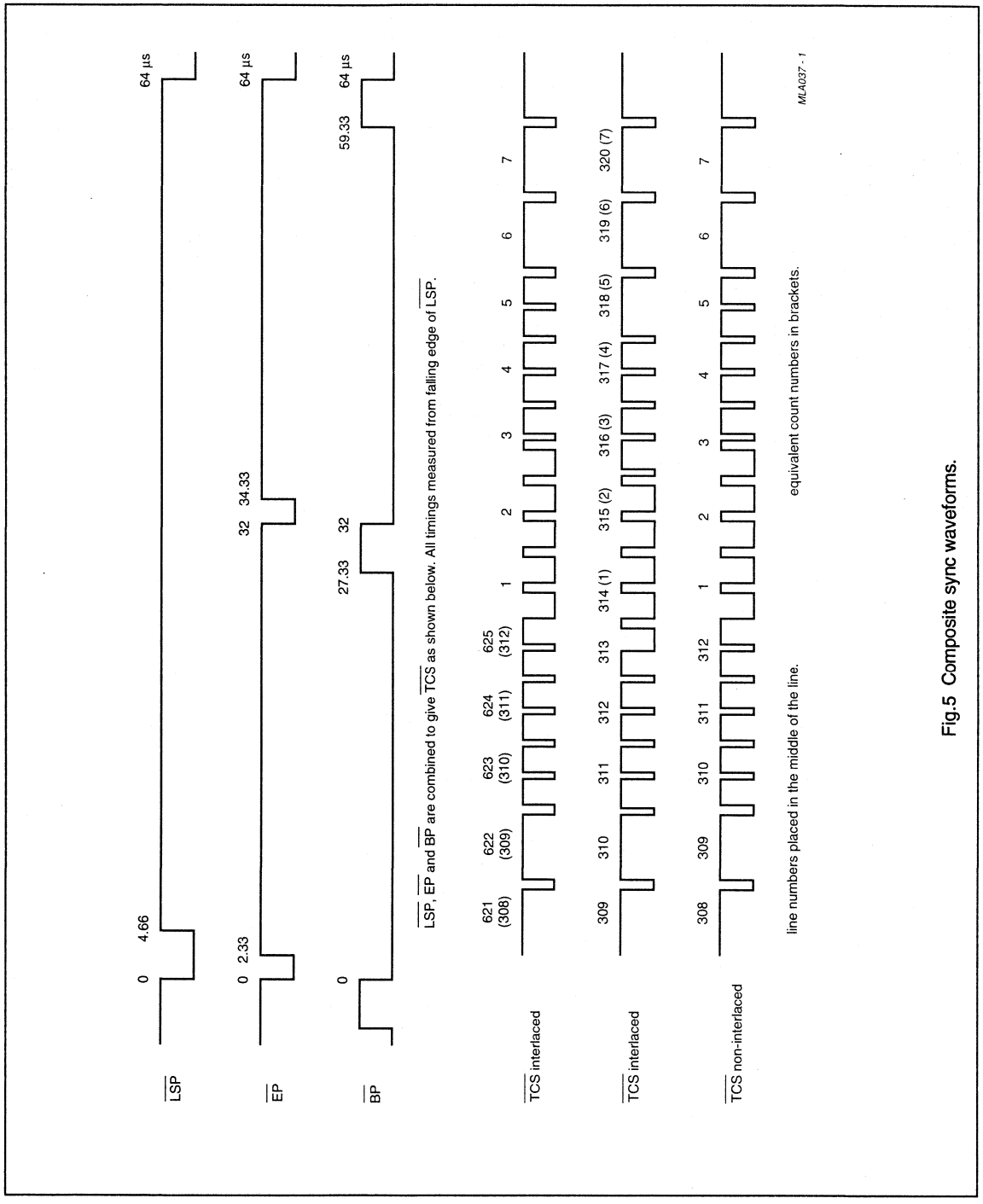


Fig.5 Composite sync waveforms.

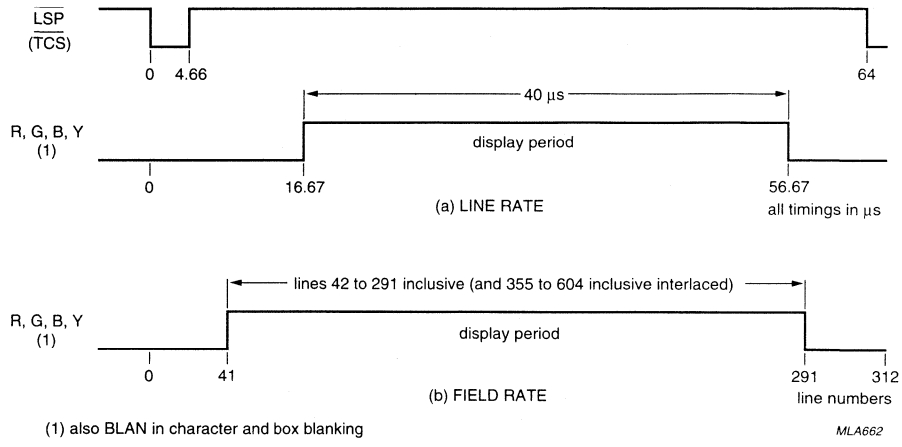


Fig.6 Display output timing (a) line rate (b) field rate.

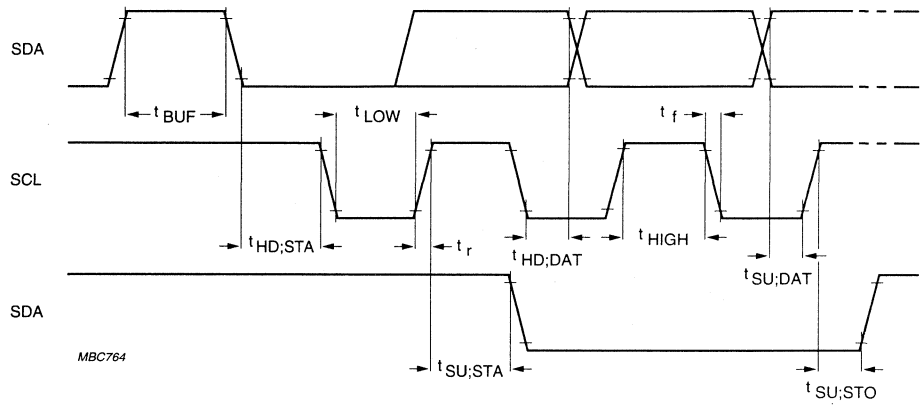


Fig.7 I²C-bus timing.

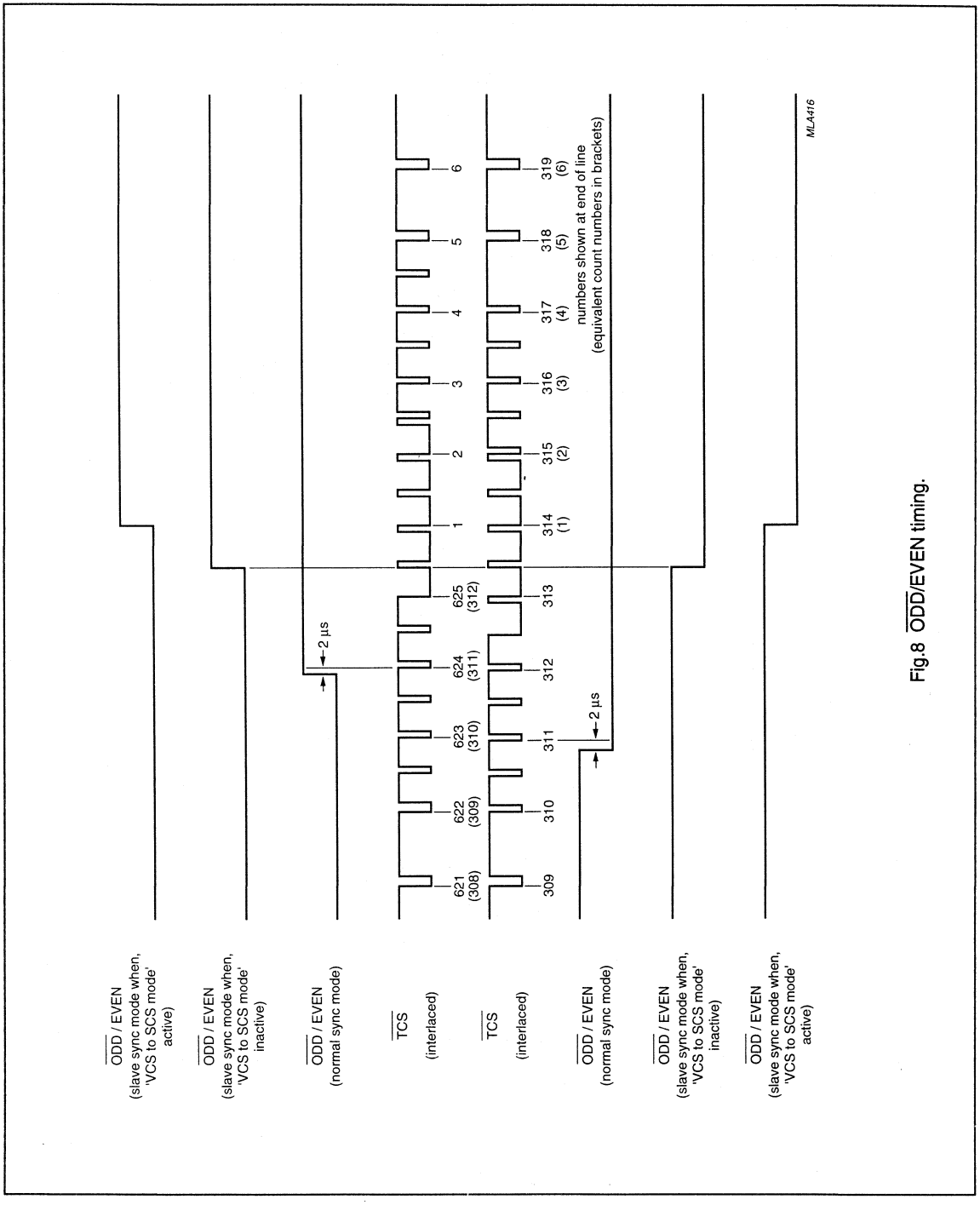
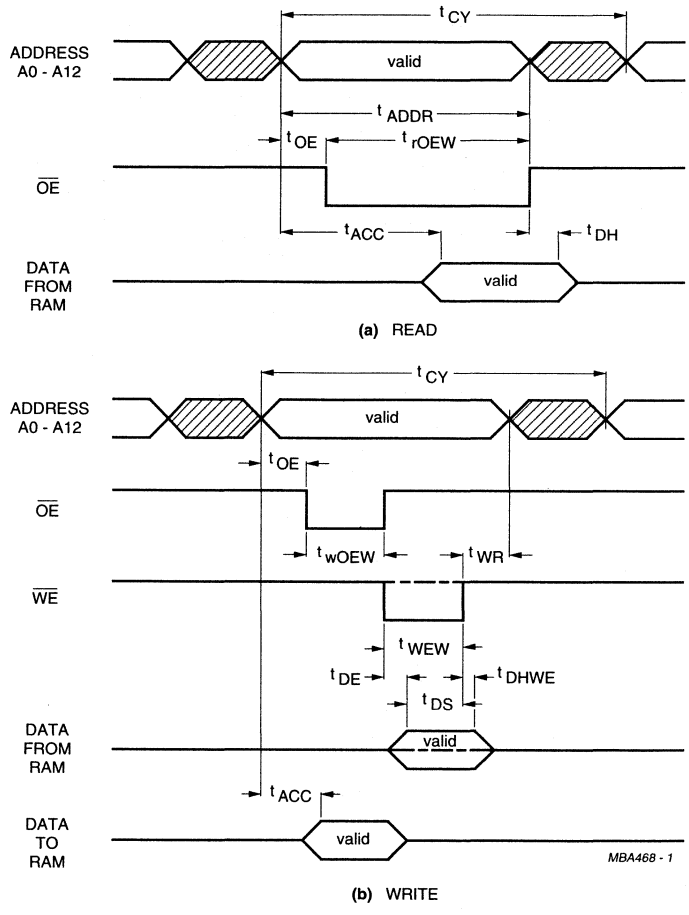


Fig.8 $\overline{\text{ODD}}$/EVEN timing.



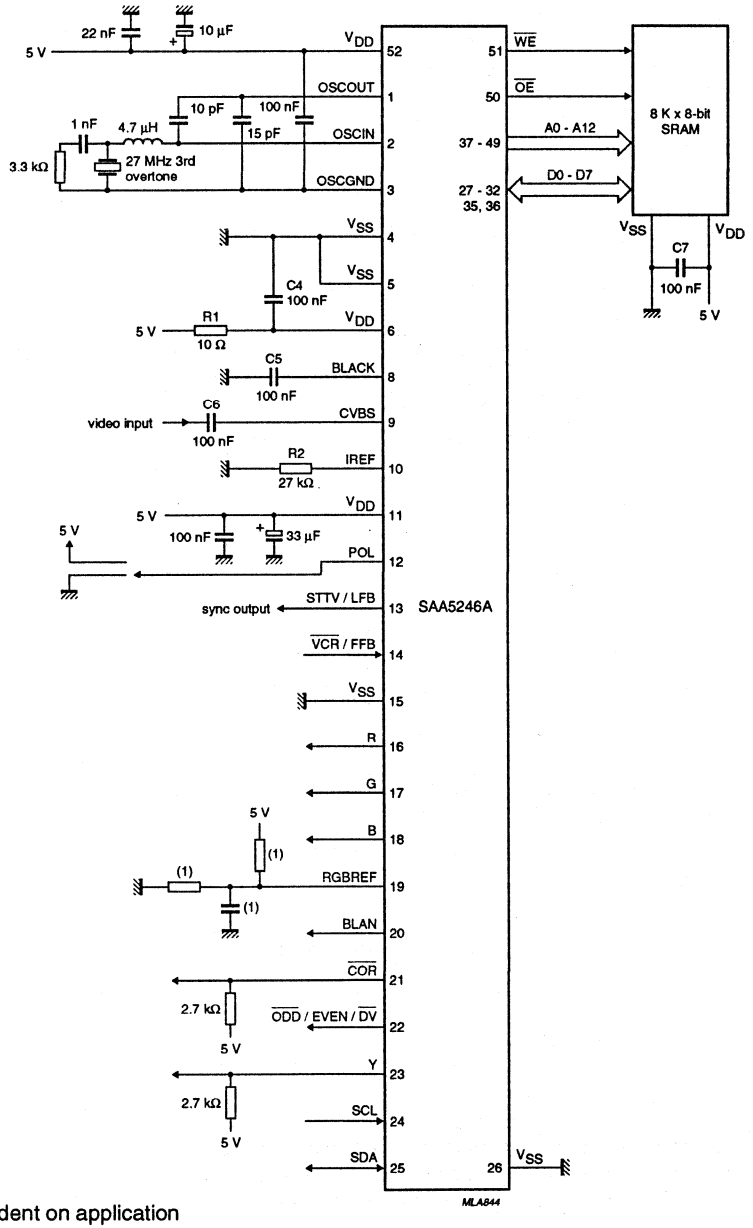
_.._.._ Level during flicker stopped cycle.

Fig.9 Memory interface timing (a) read (b) write.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

APPLICATION INFORMATION



(1) Value dependent on application

Fig.10 Application diagram.

SAA5246A page memory organization

The organization of the page memory is illustrated by Fig.11. The SAA5246A provides an additional row as compared with first generation decoders; this brings the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page; Rrow 24 is the extra row available for software generated status messages and FLOF/FASTEXT prompt information.

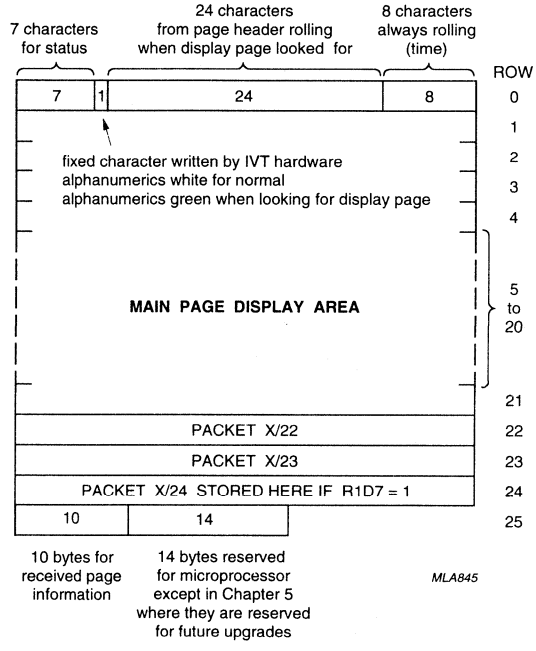


Fig.11 Basic page memory organization.

Note to Fig.11

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by SAA5246A to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of Row 25 contain control data relating to the received page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer, except in Chapter 5 where they are reserved for future upgrades.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

Page number

MAG magazine
PU page units
PT page tens

PBLF page being looked for
$\overline{\text{FOUND}}$ LOW for page has been found
HAM.ER Hamming error in corresponding byte

Page sub-code

MU minutes units
MT minutes tens
HU hours units
HT hours tens

C4-C14 transmitted control bits.

When in extension packet enabled mode the rows of information are organized as illustrated by Fig.12.

Row 23 of the extension page, as shown in Fig.12, contains packet 8/30. Packet 8/30 is mapped into the SAA5246A memory as follows:

8/30/0 and 8/30/1 to Chapter 4 Row 23
8/30/2 and 8/30/3 to Chapter 5 Row 23
8/30/4 to 8/30/15 to Chapter 6 Row 23

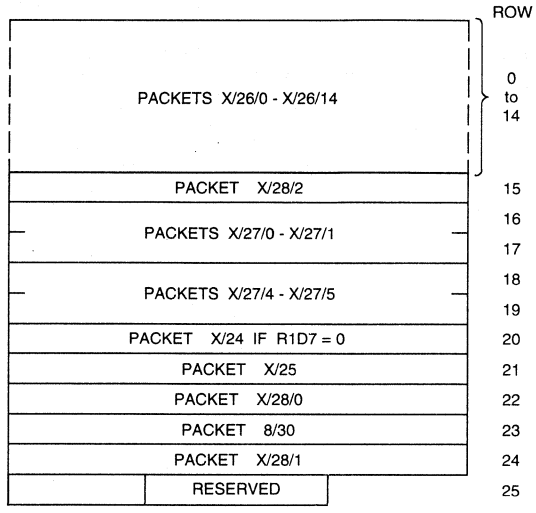


Fig.12 Organization of the extension memory.

Register maps

SAA5246A mode registers R0 to R11 are shown in Table 2. R0 to R10 are WRITE only; R11 is READ/WRITE. Register map (R3), for page requests, is shown in detail in Table 4.

Table 2 Register map

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
Adv. control	0	X24 POS	FREE RUN PLL	AUTO $\overline{\text{ODD}}$/EVEN	DISABLE HDR ROLL	–	DISABLE $\overline{\text{ODD}}$/EVEN	VCR MODE	$\overline{\text{R11}}$/R11B SELECT
Mode	1	VCS TO SCS	$\overline{7+P}$/ 8-BIT	ACQ $\overline{\text{ON}}$/OFF	EXT. PACKET ENABLE	$\overline{\text{DEW}}$/ FULL FIELD	TCS ON	T1	T0
Page request address	2	HAM. CHECK 27, 28, 8/30	BANK SELECT A2	ACQ CIRCUIT A1	ACQ CIRCUIT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request data	3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
Display chapter	4	–	–	–	–	–	A2	A1	A0
Display control (normal)	5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash /subtitle)	6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	7	STATUS TOP	CURSOR ON	REVEAL ON	BOTTOM HALF	DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0
Active chapter	8	–	–	–	–	CLEAR MEM.	A2	A1	A0
Cursor row	9	–	–	–	R4	R3	R2	R1	R0
Cursor column	10	–	–	C5	C4	C3	C2	C1	C0
Cursor data	11	D7	D6	D5	D4	D3	D2	D1	D0
Device status	11B	$\overline{625}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	DATA QUALITY	VCS SIGNAL QUALITY

Notes to Table 2

1. All bits in registers R0 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R1, R5 and R6 which are set to logic 1.
2. All memory is cleared to 'space' (00100000) on power-up, except Row 0 Column 7 Chapter 0, which is 'alpha' white (00000111) as the acquisition circuit is enabled but the page is on hold.
3. TB must be set to logic 0 for normal operation.
4. The I²C-bus slave address is 0010001.

Where:

'–' Indicates a bit which does not exist and must be written to logic 0 for future compatibility.

Register description

R0 ADVANCED CONTROL - auto increments to Register 1

$\overline{R11}$/R11B SELECT	Selects reading of R11 or R11B
VCR MODE	Selects short time constant of PLL when logic 1
DISABLE $\overline{ODD}$/EVEN	Forces $\overline{ODD}$/EVEN output LOW when logic 1 (see Table 3)
DISABLE HDR ROLL	Disables green rolling header and time
AUTO $\overline{ODD}$/EVEN	When set forces $\overline{ODD}$/EVEN low if any TV picture displayed, if DISABLE $\overline{ODD}$/EVEN = 0 (see Table 3)
FREE RUN PLL	Will force the PLL to free run in all conditions
X24 POS	Automatic display of FASTEXT prompt row when logic 1

R1 MODE - auto increments to Register 2

T0, T1	Interlace/non-interlace 312/313 line control (see Table 5)
TCS ON	Text composite sync or direct sync select
$\overline{DEW}$/FULL FIELD	Field-flyback or full channel mode
EXT. PACKET ENABLE	Allocates 2.8 k memory per chapter
ACQ $\overline{ON}$/OFF	Aquisition circuits turned off when logic 1
$\overline{7 + P}$/8-BIT	7 bits with parity checking or 8-bit mode
VCS TO SCS	When logic 1 enables display of messages with 60 Hz input signal

R2 PAGE REQUEST ADDRESS - auto increments to Register 3

HAM. CHECK 27 28 8/30	When logic 1 enables hamming checking of extension packet 27, 28, 8/30
COL SC0 - SC2	Point to start column for page request data (see Table 4)
TB	Must be logic 0 for normal operation
ACQ CIRCUIT	Selects one of four acquisition circuits
BANK SELECT	Selects which bank of four pages is being accessed

R3 PAGE REQUEST DATA - does not auto increment (see Table 4)

R4 DISPLAY CHAPTER - auto increments to Register 5

determines which of the 8 pages is displayed

R5 NORMAL DISPLAY CONTROL - auto increments to Register 6

PON	Picture on
TEXT	Text on
COR	Contrast reduction on
BKGND	Background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R6 NEWSFLASH DISPLAY - auto increments to Register 7

PON	Picture on
TEXT	Text on
COR	Contrast reduction on
BKGND	Background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 DISPLAY MODE - does not auto increment

BOX ON 0	Boxing function allowed on Row 0
BOX ON 1-23	Boxing function allowed on Row 1-23
BOX ON 24	Boxing function allowed on Row 24
DOUBLE HEIGHT	To display double height text
BOTTOM HALF	To select bottom half of page when DOUBLE HEIGHT = 1
REVEAL ON	To reveal concealed text
CURSOR ON	To display cursor
STATUS TOP	Row 25 displayed above or below the main text

R8 ACTIVE CHAPTER - auto increments to Register 9

A0 to A2	Active chapter
CLEAR MEMORY	When set to 1, clears the display memory. This bit is automatically reset

R9 CURSOR ROW - auto increments to Register 10

R0 to R4	Active row for data written to or read from memory via the I²C-bus

R10 CURSOR COLUMN - auto increments to Register 11 or 11B

C0 to C5	Active column for data written to or read from memory via the I²C-bus

R11 CURSOR DATA - does not auto increment

D0 to D7	Data read from/written to memory via I²C, at location pointed to by R8, R9 and R10. This location automatically increments each time R11 is accessed

R11B DEVICE STATUS - does not auto increment

VCS SIGNAL QUALITY	Indicates that the video signal quality is good and PLL is phase locked to input video when = 1
DATA QUALITY	If good data (either Teletext or VPS) is detected then = 1
ROM VER R0 to R4	Indicated language/ROM variant. See Table 7
$\overline{625}$/525 SYNC	If the input video is a 525 line signal when = 1

Table 3 Register map for page requests (R3)

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

1. Abbreviations are as for Table 1 except for DO CARE bits.
2. When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
3. If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
4. Columns auto-increment on successive I²C-bus transmission bytes.
5. 'X' = Don't care.

Table 4 Interlace/non-interlace 312/313 line control (T0 and T1)

T1	T0	RESULT
0	0	interlaced 312.5/312.5 lines
0	1	non-interlaced 312/313 lines (note 1)
1	0	non-interlaced 312/312 lines (note 1)
1	1	SCS mode (scan composite sync)

Note to Table 4

1 Reverts to interlaced mode if a newsflash or subtitle is being displayed.

CLOCK SYSTEMS

Crystal oscillator

The crystal is a conventional 2-pin design operating at 27 MHz. It is capable of oscillating with both fundamental and third overtone mode crystals. External components should be used to suppress the fundamental output of the third overtone as illustrated in Fig.13.

Table 5 Crystal characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Crystal (27 MHz, 3rd overtone)					
C1	series capacitance	–	1.7	–	pF
C0	parallel capacitance	–	5.2	–	pF
C_L	load capacitance	–	20	–	pF
Rr	resonant resistance	–	–	50	Ω
R1	series resistance	–	20	–	Ω
Xa	ageing	–	–	±5	10^{-6}/yr
Xj	adjustment tolerance	–	–	±25	10^{-6}
Xd	drift	–	–	±25	10^{-6}

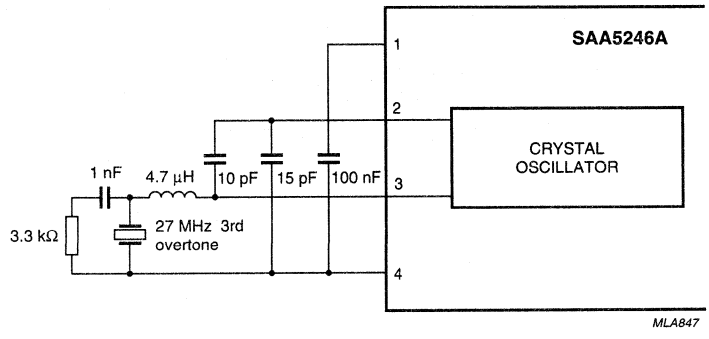


Fig.13 Crystal oscillator application diagram; pins indicated are for SOT240.

Character sets

The WST specification allows the selection of national character sets via the page header transmission bits, C12 to C14. The basic 96 character sets differ only in 13 national option characters as indicated in Table 8 with reference to their table position in the basic character matrix illustrated in Table 7. The SAA5246A automatically decodes transmission bits C12 to C14. Table 6 illustrates the character matrixs.

Character bytes are listed as transmitted from b1 to b7.

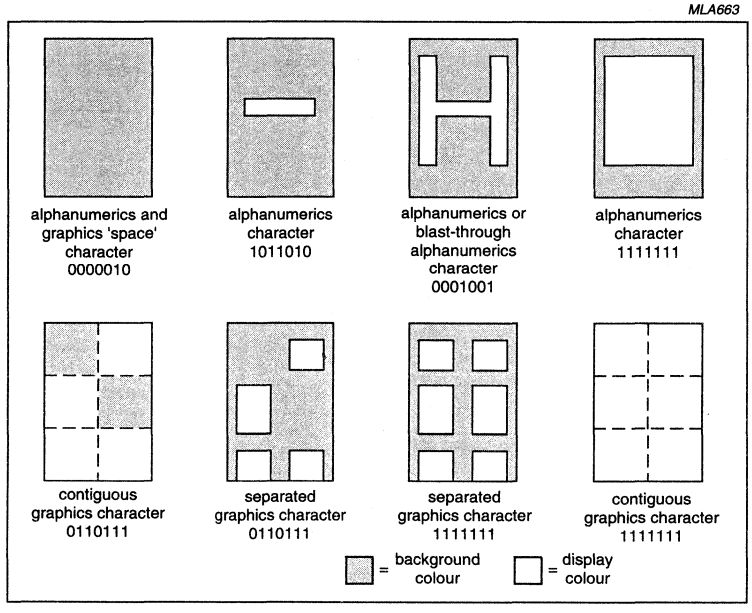
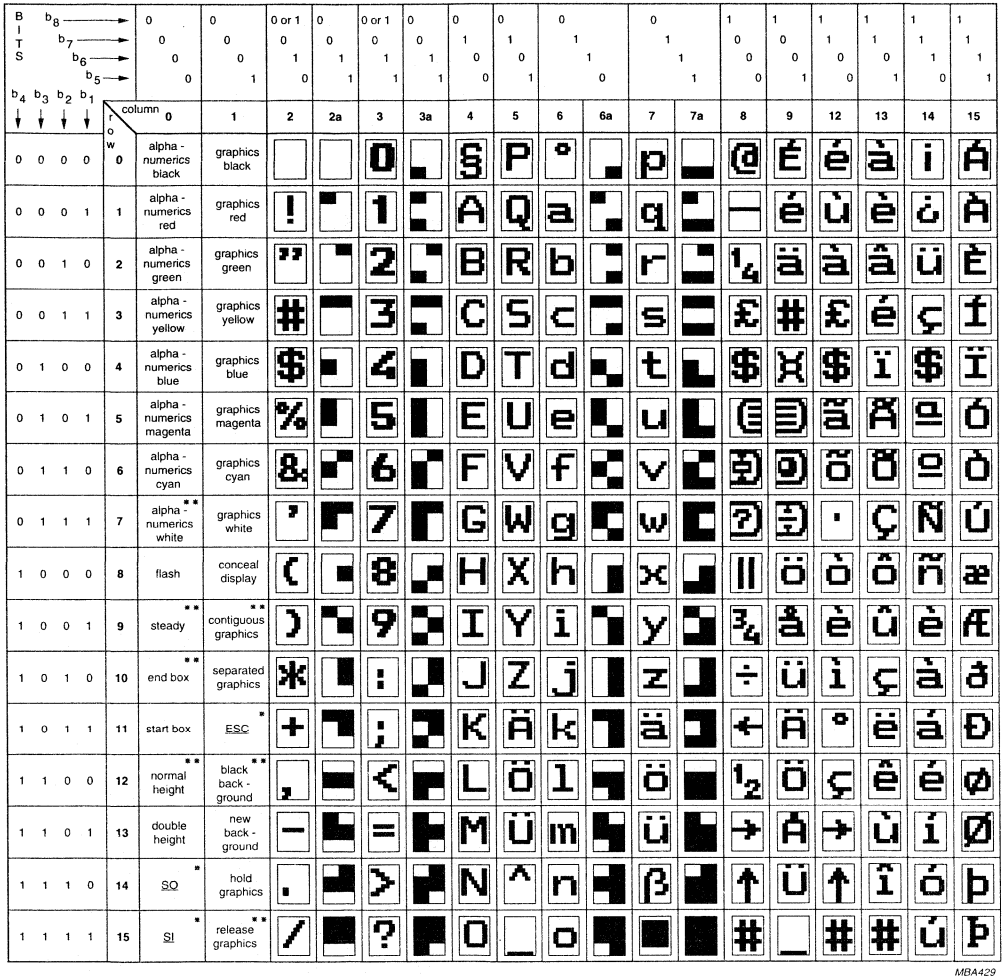


Fig.14 Character format.

Table 6a SAA5246AP/E character data input decoding



For character version number (00000) see Register 11B.

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Table 6b SAA5246AP/H character data input decoding, East European languages

BITS b_8	0	0	0 or 1	0	0 or 1	0	0	0	0	0	0	1	1	1	1	1	1
b_7	0	0	0	1	1	1	1	0	1	1	1	0	0	1	1	1	1
b_6	0	0	1	0	1	0	1	0	0	1	1	0	0	0	1	1	1
b_5	0	1	0	0	0	1	1	0	1	0	1	0	1	0	0	1	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓ column / row	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha-numerics black	graphics black															
0 0 0 1	1	alpha-numerics red	graphics red															
0 0 1 0	2	alpha-numerics green	graphics green															
0 0 1 1	3	alpha-numerics yellow	graphics yellow															
0 1 0 0	4	alpha-numerics blue	graphics blue															
0 1 0 1	5	alpha-numerics magenta	graphics magenta															
0 1 1 0	6	alpha-numerics cyan	graphics cyan															
0 1 1 1	7	alpha-** numerics white	graphics white															
1 0 0 0	8	flash	conceal display															
1 0 0 1	9	** steady	** contiguous graphics															
1 0 1 0	10	** end box	separated graphics															
1 0 1 1	11	start box	* ESC															
1 1 0 0	12	** normal height	** black background															
1 1 0 1	13	double height	new background															
1 1 1 0	14	* SO	hold graphics															
1 1 1 1	15	* SI	** release graphics															

7Z22497.5

For character version number (00001) see Register 11B.

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Table 6c SAA5246AP/T character data input decoding, West European and Turkish languages

BITS b_4 b_3 b_2 b_1	row	column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
		b_8 →	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
		b_7 →	0	0	0	0	0	1	1	1		1		0	0	1	1	1	1
		b_6 →	0	0	1	1	1	0	0	1		1		0	0	0	0	1	1
		b_5 →	0	1	0	1	1	0	1	0		1		0	1	0	1	0	1
0 0 0 0	0	alpha - numerics black	graphics black																
0 0 0 1	1	alpha - numerics red	graphics red																
0 0 1 0	2	alpha - numerics green	graphics green																
0 0 1 1	3	alpha - numerics yellow	graphics yellow																
0 1 0 0	4	alpha - numerics blue	graphics blue																
0 1 0 1	5	alpha - numerics magenta	graphics magenta																
0 1 1 0	6	alpha - numerics cyan	graphics cyan																
0 1 1 1	7	alpha - numerics ** white	graphics white																
1 0 0 0	8	flash	conceal display																
1 0 0 1	9	steady **	contiguous graphics **																
1 0 1 0	10	end box **	separated graphics																
1 0 1 1	11	start box	ESC *																
1 1 0 0	12	normal height **	black back - ground **																
1 1 0 1	13	double height	new back - ground																
1 1 1 0	14	SO *	hold graphics																
1 1 1 1	15	SI *	release graphics **																

MBA431

For character version number (00010) see Register 11B.

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Table 6d SAA5246AP/L character data input decoding, Arabic and Hebrew languages

BITS b_8	0	0	0 or 1	0	0 or 1	0	0	0	0	0 or 1	0	0 or 1	1	1	1	1	1	1
b_7	0	0	0	1	1	1	1	0	0	0	1	1	0	0	0	0	1	1
b_6	0	0	1	0	0	1	1	0	1	1	0	0	0	0	1	1	0	0
b_5	0	1	0	0	1	0	1	0	0	1	0	1	0	1	0	1	0	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓ / row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha-numerics black	graphics black															
0 0 0 1	1	alpha-numerics red	graphics red															
0 0 1 0	2	alpha-numerics green	graphics green															
0 0 1 1	3	alpha-numerics yellow	graphics yellow															
0 1 0 0	4	alpha-numerics blue	graphics blue															
0 1 0 1	5	alpha-numerics magenta	graphics magenta															
0 1 1 0	6	alpha-numerics cyan	graphics cyan															
0 1 1 1	7	alpha-** numerics white	graphics white															
1 0 0 0	8	flash	conceal display															
1 0 0 1	9	** steady	** contiguous graphics															
1 0 1 0	10	** end box	separated graphics															
1 0 1 1	11	start box	TWIST															
1 1 0 0	12	** normal height	black ** background															
1 1 0 1	13	double height	new background															
1 1 1 0	14	* SO	hold graphics															
1 1 1 1	15	* SI	** release graphics															

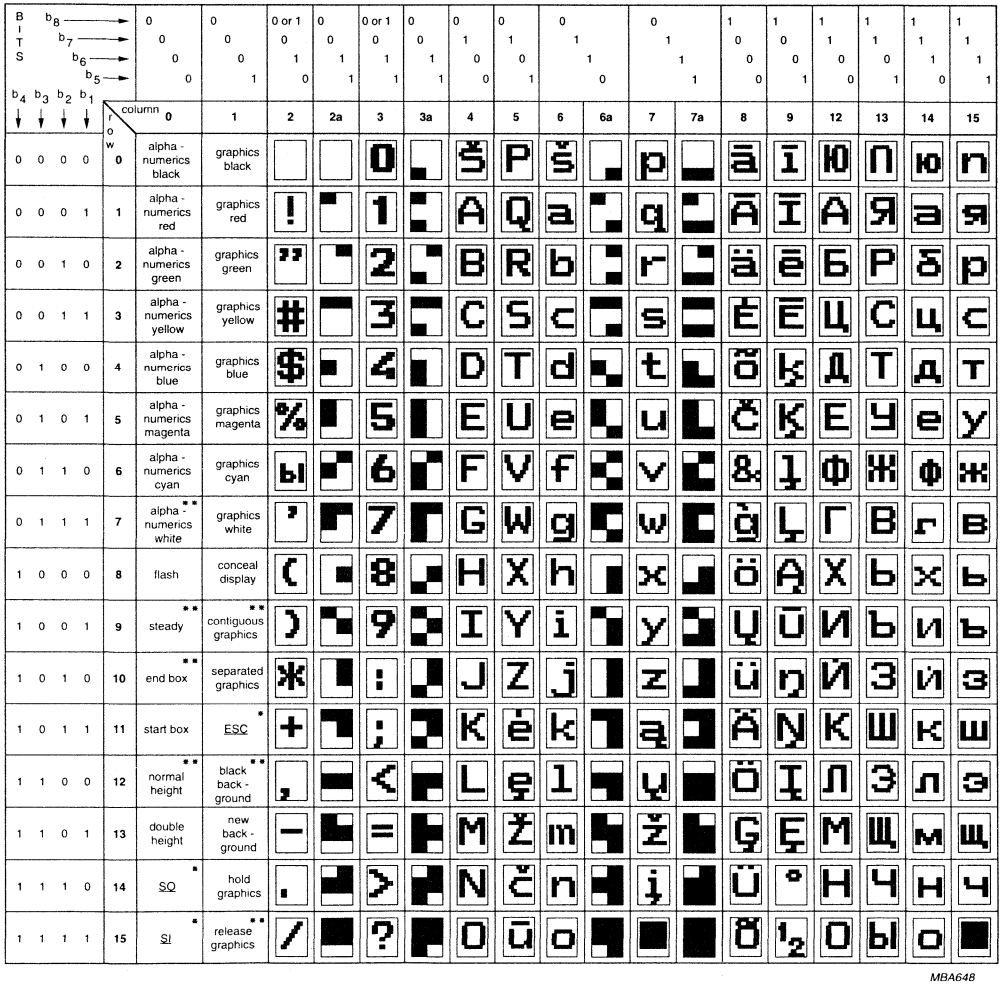
7Z22679.4

For character version number (00100) see Register 11B.

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Table 6e SAA5246AP/R character data input decoding, Baltic and Cyrillic languages



For character version number (00101) see Register 11B.

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Notes to Table 6

1. Control characters shown in Columns 0 and 1 are normally displayed as spaces.
2. Characters may be referred to by column and row, For example 2/5 refers to %.
3. Black represents displayed colour. White represents backgound.
4. Character rectangle shown as follows: 
5. The SAA5246A national option characters are illustrated in Table 8.
6. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters for combining with character 8/5.
7. National option characters will be developed according to the setting of control bits C12 to C14. These will be mapped into the basic code table into positions shown in Table 8.
8. Columns 2a, 3a, 6a and 7a are displayed in graphics mode.

Table 7 SAA5246A basic character matrix

Table 8a SAA5246AP/E national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MEA559

(1) PHCB are the Page Header Control Bits. Other combinations default to English.

Table 8b SAA5246AP/H national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN/ROW)													
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
POLISH	0	0	0	#	ń	ą	Ż	Ś	Ł	ć	ó	ę	ż	ś	ł	ź
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
SERBO-CROAT	1	0	1	#	½	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
CZECHOSLOVAK	1	1	0	#	ů	č	ť	ž	ý	í	ř	é	á	ě	ú	š
RUMANIAN	1	1	1	#	¤	Ţ	Â	Ş	Ă	Î	ı	ţ	â	ş	ă	î

7Z22658.1

(1) PHCB are the Page Header Control Bits. Other combinations default to German. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 7.

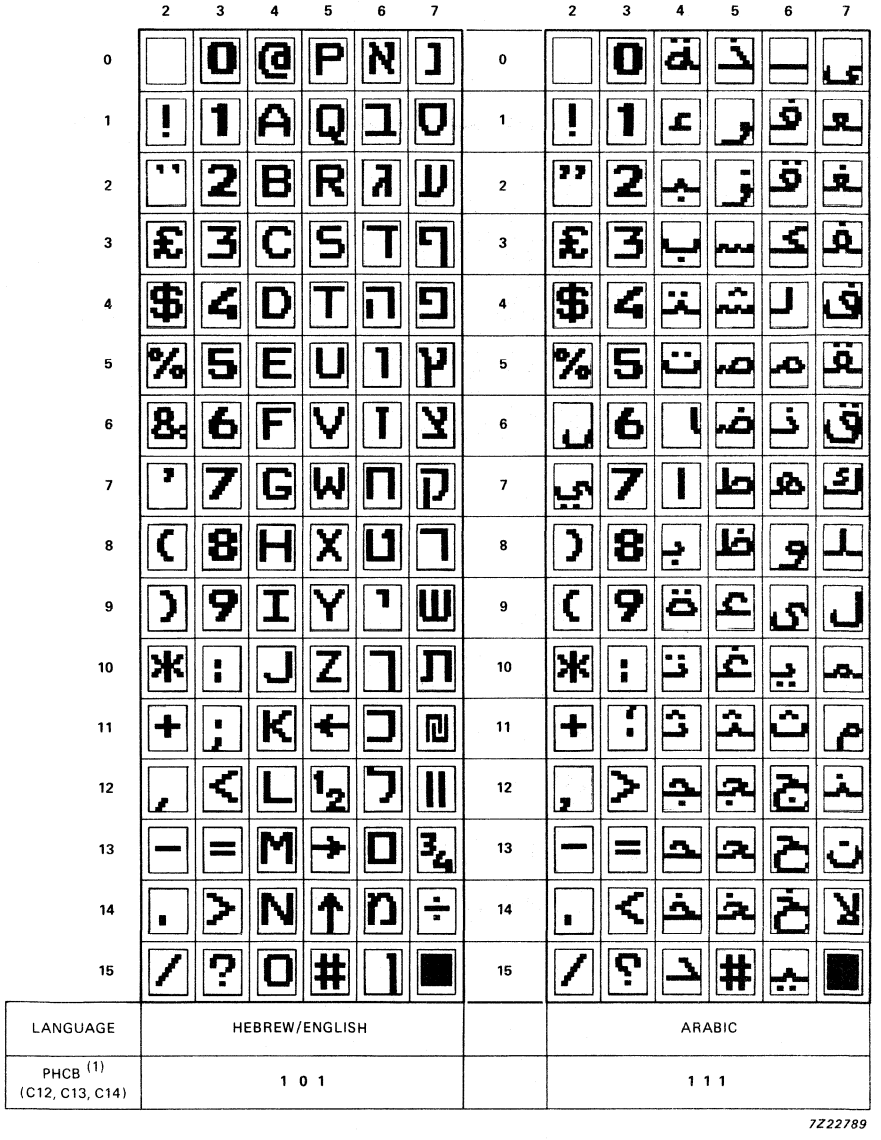
Table 8c SAA5246AP/T national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)													
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
TURKISH	1	1	0	Ł	ğ	İ	Ş	Ö	Ç	Ü	Ğ	ı	ş	ö	ç	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MBA430

(1) PHCB are the Page Header Control Bits. Other combinations default to English. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 7.

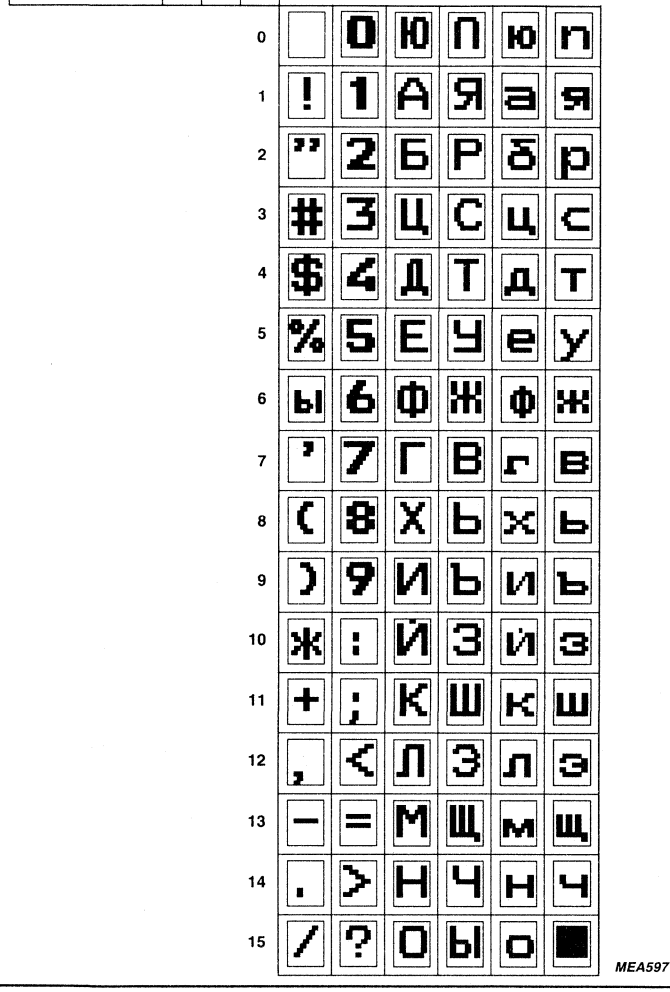
Table 8d SAA5246AP/L national option character set



(1) PHCB are the Page Header Control Bits. Other combinations default to English.

Table 8e SAA5246AP/R national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ESTONIAN	0	1	0	#	Õ	Š	Ä	Ö	Ž	Ü	Õ	š	ä	ö	ž	ü
LETTISH / LITHUANIAN	0	1	1	#	$	Š	ė	ę	Ž	č	ū	š	ą	ų	ž	į
RUSSIAN	1	0	0													



(1) PHCB are the Page Header Control Bits. Other combinations default to Estonian.

Integrated VIP and Teletext with Background Memory Controller (IVT1.1BMC)

SAA5247

FEATURES

- Complete background memory controller enabling storage of up to 512 teletext pages in external RAM
- Interfaces to either one 256 K x 4 DRAM, two 256 K x 4 DRAMs or 1 M x 4 DRAM, pin programmable
- Fast background memory scan. Maximum access time to any one of 512 pages = 0.2 s
- Single +5 V power supply
- Digital data slicer and display clock phase-locked loop reduce peripheral components to a minimum
- Both video and scan related synchronization modes are supported
- On board single page memory including extension packets for FASTEXT
- Single page acquisition system
- RGB interface to standard colour decoder ICs, push-pull output drive
- Data capture performance similar to SAA5231 (VIP2)
- Simple software control via I²C-bus and software compatible with SAA5244 (IVT1.1)
- Options for five national languages
- 32 supplementary characters for on-screen displays
- Optional storage of packet 24 in the display memory
- Page links in packets 27 and 8/30 are Hamming decoded
- Separate text and video signal quality detectors, 625/525 video status and language version all readable via I²C-bus
- Automatic ODD/$\overline{\text{EVEN}}$ output control with manual override
- Control of display PLL free-run and rolling header via I²C-bus
- VCS to SCS mode for stable 525 line status display

DESCRIPTION

The Integrated VIP and Teletext (IVT1.1BMC) is a teletext decoder (contained within a single chip package) for decoding 625-line based World System Teletext transmissions, with in-built background memory controller for direct storage of all incoming teletext transmissions. The BMC can store up to 512 teletext pages in external DRAMs; this is rapidly scanned on each page request, thereby giving near instant page access. The teletext decoder is based on the IVT1.1 device (SAA5244) and is designed to be software compatible. The pins are arranged so that one PCB can take either an IVT1.1 or IVT1.1BMC. The Video Input Processor (VIP) section of the device uses mixed analog and digital designs for the data slicer and the display clock phase-locked loop functions. As a result the number of external components is greatly reduced and no critical or adjustable components are required. A single page static RAM is incorporated in the device thereby giving a genuine single-chip teletext decoder device.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5247P/B	48	DIL	plastic	SOT240
SAA5247GP/B	64	QFP	plastic	SOT208

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	90	180	mA
V_{syn}	sync amplitude	0.1	0.3	0.6	V
V_{vid}	video amplitude	0.7	1.0	1.4	V
f_{XTAL}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature range	–20	–	+70	°C

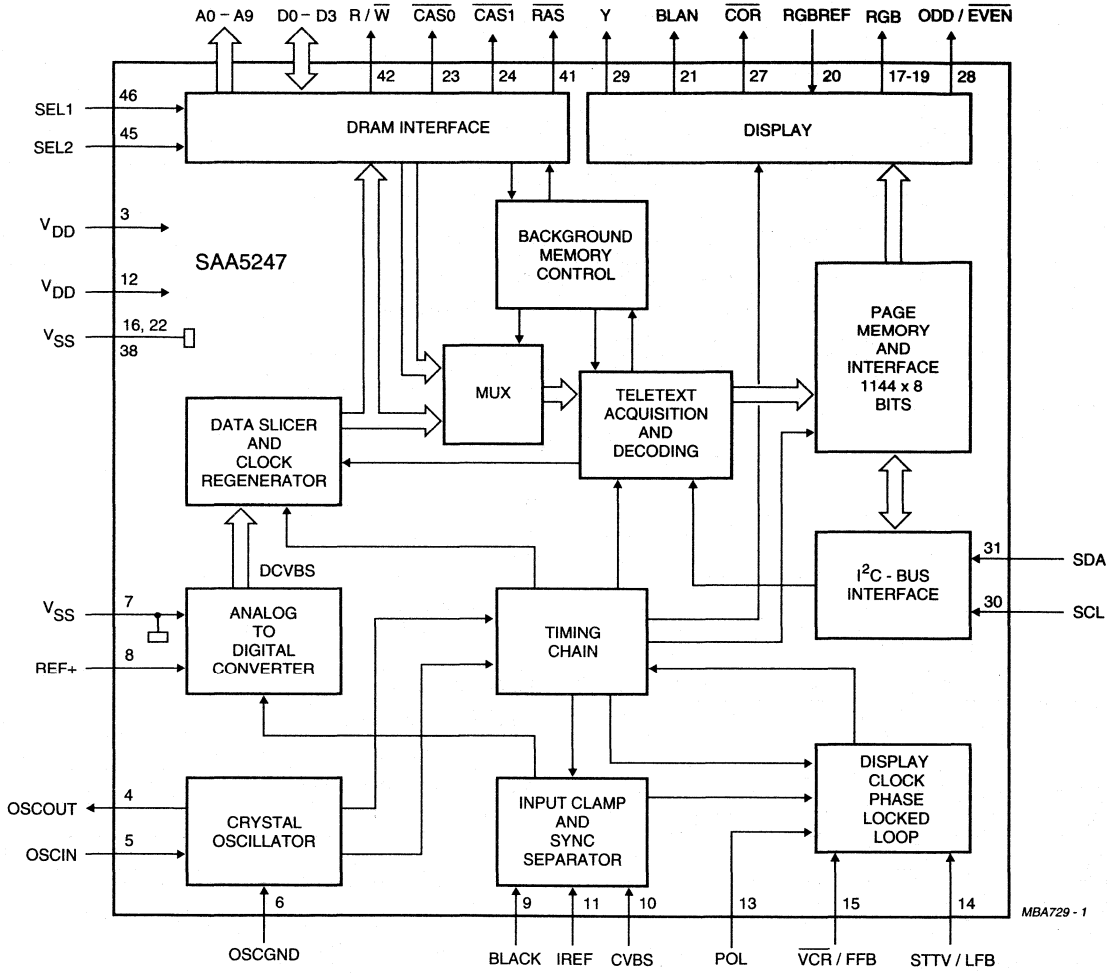


Fig.1 Block diagram for SOT240 (DIL48) package.

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT240	SOT208	
n.c.	1	1	not connected
n.c.	2	2	not connected
V_{DD}	3	25	+5 V supply
OSCOUT	4	27	27 MHz crystal oscillator output
OSCIN	5	28	27 MHz crystal oscillator input
OSCGND	6	29	0 V crystal oscillator ground
V_{SS}	7	12	0 V ground
REF+	8	32	positive reference voltage. The pin should be connected to +5 V supply
BLACK	9	35	video black level storage pin, connected to ground via a 100 nF capacitor
CVBS	10	36	composite video input pin. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor
IREF	11	37	reference current input pin, connected to ground via a 27 kΩ resistor
V_{DD}	12	38	+5 V supply
POL	13	39	STTV/LFB/FFB polarity selection pin
STTV/LFB	14	40	sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode)
$\overline{VCR}$/FFB	15	42	PLL time constant switch/field input pin. Function controlled by an internal register bit (scan sync mode)
V_{SS}	16	30	0 V ground
REF–	–	31	negative reference voltage; this pin should be connected to REF+ via a 100 nF capacitor
R	17	49	dot rate character output of the RED colour information
G	18	50	dot rate character output of the GREEN colour information
B	19	51	dot rate character output of the BLUE colour information
RGBREF	20	52	input DC voltage to define the output high level on the RGB pins
BLAN	21	53	dot rate fast blanking output
V_{SS}	22	54, 55	0 V ground
$\overline{CAS0}$	23	56	column address select to external DRAM for BMC function
$\overline{CAS1}$	24	57	column address select to external DRAM for BMC function for second DRAM where two 256 k x 4 devices are used
A4	25	58	address output to external DRAM for BMC function
A3	26	59	address output to external DRAM for BMC function
$\overline{COR}$	27	60	programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages. Open drain output
ODD/$\overline{EVEN}$	28	61	25 Hz output synchronized with the CVBS input's field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents
Y	29	62	dot rate character output of teletext foreground colour information. Open drain output

SYMBOL	PIN		DESCRIPTION
	SOT240	SOT208	
SCL	30	63	serial clock input for I²C-bus. It can still be driven HIGH during power-down of the device
SDA	31	64	serial data port for the I²C-bus. Open drain output. It can still be driven HIGH during power-down of the device
A5	32	4	address output to external DRAM for BMC function
A2	33	5	address output to external DRAM for BMC function
A6	34	6	address output to external DRAM for BMC function
A1	35	8	address output to external DRAM for BMC function
A7	36	9	address output to external DRAM for BMC function
A0	37	11	address output to external DRAM for BMC function
V_{SS}	38	43	0 V ground
A8	39	13	address output to external DRAM for BMC function
A9	40	14	address output to external DRAM for BMC function
$\overline{RAS}$	41	15	row address select to external DRAM
R/$\overline{W}$	42	18	read/$\overline{write}$ for external DRAM
D2	43	19	data input/output for external DRAM
D0	44	20	data input/output for external DRAM
SEL2	45	21	RAM select input to choose external DRAM size
SEL1	46	22	RAM select input to choose external DRAM size
D3	47	23	data input/output for external DRAM
D1	48	24	data input/output for external DRAM

The remaining pins for SOT208 are not connected.

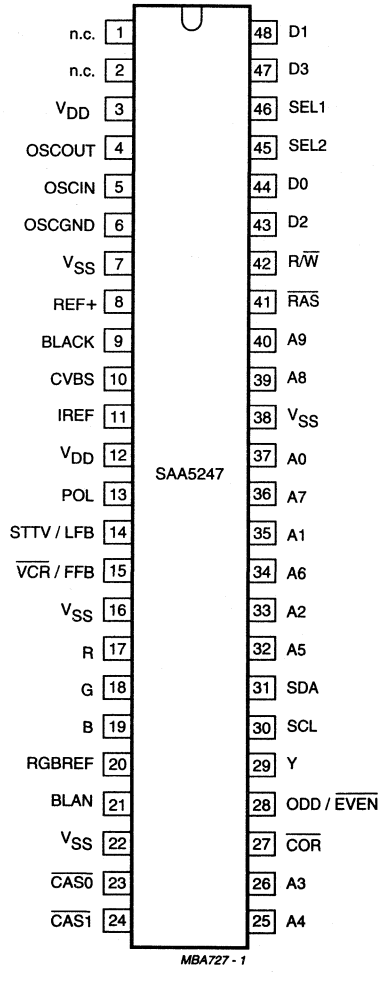


Fig.2 Pin configuration; SOT240 (DIL48).

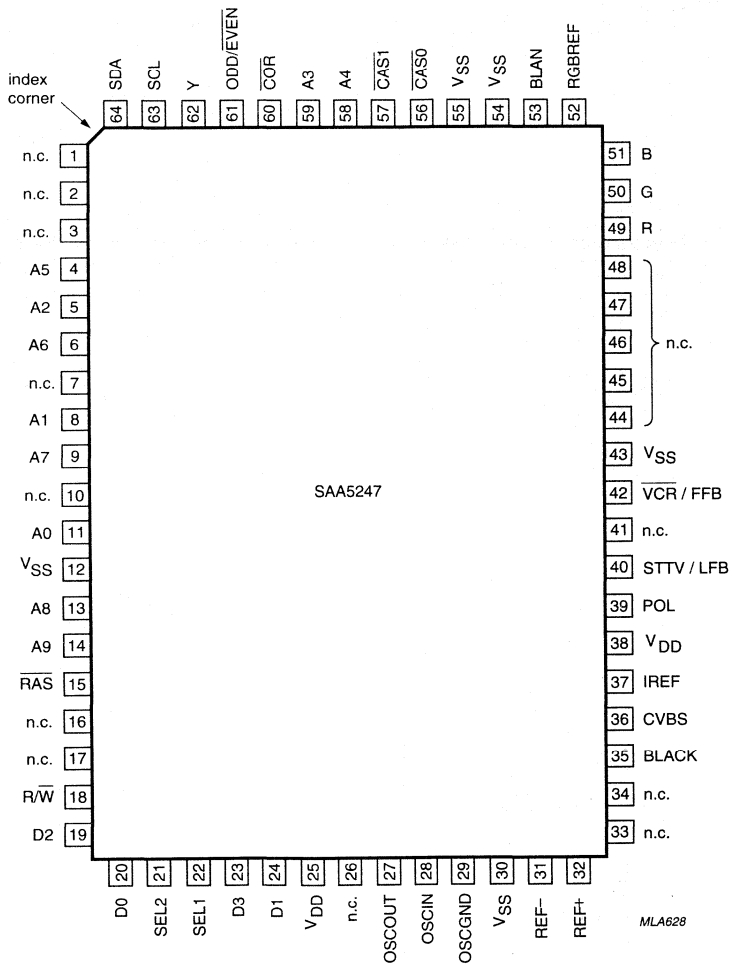


Fig.3 Pin configuration; SOT208 (QFP64).

LIMITING VALUES

In accordance with Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	−0.3	+6.5	V
V_I	input voltage (any input)	−0.3	V_{DD}+0.5	V
V_O	output voltage (any output)	−0.3	V_{DD}+0.5	V
V_{Sdiff}	difference between V_{SS} and OSCGND	−0.25	+0.25	V
V_{Ddiff}	difference between V_{DD} and REF+	−0.25	+0.25	V
I_O	output current (each output)	−	±10	mA
I_{IOK}	DC input or output diode current	−	±20	mA
T_{amb}	operating ambient temperature range	−20	+70	°C
T_{stg}	storage temperature range	−55	+125	°C
V_{stat}	electrostatic handling (see note)	−2000	+2000	V

Note

Electrostatic handling is equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor with a 15 ns rise time.

Failure Rate

The failure rate at T_{amb} = 55 °C will be a maximum of 1000 FITS (1 FIT = 1 x 10^{-9} failures per hour).

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = −20 to +70 °C, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage range		4.5	5	5.5	V
I_{DD}	total supply current		–	90	125	mA
Inputs						
CVBS						
V_{syn}	sync amplitude		0.1	0.3	0.6	V
t_{syn}	delay from CVBS to TCS output from STTV buffer (nominal video, average of leading/trailing edge)		−150	0	150	ns
t_{syd}	change in sync delay between all black and all white video input at nominal levels		0	–	25	ns
$V_{vid(p-p)}$	video input amplitude (peak-to-peak)		0.7	1.0	1.4	V
	display PLL catching range		±7	–	–	%
Z_{src}	source impedance		–	–	250	Ω
C_I	input capacitance		–	–	10	pF
IREF						
R_g	resistor to ground		–	27	–	kΩ
POL						
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
LFB						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
I_I	input current	note 1	−1	–	+1	mA
t_{LFB}	delay between LFB front edge and input video line sync		–	250	–	ns
$\overline{VCR}$/FFB						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
I_I	input current	note 1	−1	–	+1	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
RGBREF (NOTE 2)						
V_{IL}	LOW level input voltage		−0.3	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	μA
I_{DC}	DC current		–	–	10	mA
SEL1 AND SEL2						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	μA
SCL						
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	μA
f_{SCL}	clock frequency		0	–	100	kHz
t_r	input rise time	10% to 90%	–	–	2	μs
t_f	input fall time	90% to 10%	–	–	2	μs
C_I	input capacitance		–	–	10	pF
Inputs/outputs						
CRYSTAL OSCILLATOR (OSCIN; OSCOUT)						
f_{XTAL}	crystal frequency		–	27	–	MHz
G_v	small signal voltage gain		3.5	–	–	–
G_m	mutual conductance	f = 100 kHz	1.5	–	–	mA/V
C_I	input capacitance		–	–	10	pF
C_{FB}	feedback capacitance		–	–	5	pF
BLACK						
C_{blk}	storage capacitor to ground		–	100	–	nF
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	μA
SDA						
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	μA
C_I	input capacitance		–	–	10	pF
t_r	input rise time	10% to 90%	–	–	2	μs
t_f	input fall time	90% to 10%	–	–	2	μs
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.5	V
t_f	output fall time	3 V to 1 V	–	–	200	ns
C_L	load capacitance		–	–	400	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs/outputs						
D0 TO D3						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current		−10	–	+10	μA
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	2.4	–	V_{DD}	V
t_r	output rise time	0.6 V to 2.2 V	–	–	20	ns
t_f	output fall time	2.2 V to 0.6 V	–	–	20	ns
C_L	load capacitance		–	–	50	pF
Outputs						
STTV						
G_{stt}	gain of STTV relative to video input		0.9	1.0	1.1	
V_{tcs}	TCS amplitude		0.2	0.3	0.45	V
V_{DCs}	DC shift between TCS output and nominal video output		–	–	0.15	V
I_O	output drive current		–	–	3.0	mA
C_L	load capacitance		–	–	100	pF
A0 TO A9 ADDRESS OUTPUT TO MEMORY						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.6 V to 2.2 V	–	–	20	ns
t_f	output fall time	2.2 V to 0.6 V	–	–	20	ns
R/$\overline{W}$, $\overline{CAS0}$ AND $\overline{CAS1}$						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.6 V to 2.2 V	–	–	20	ns
t_f	output fall time	2.2 V to 0.6 V	–	–	20	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
R, G AND B						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.2	V
V_{OH}	HIGH level output voltage	I_{OH} = –1.6 mA; RGBREF ≤ V_{DD}–2 V	RGBREF –0.25 V	RGBREF	RGBREF +0.25 V	V
$\|Z_o\|$	output impedance		–	–	200	Ω
C_L	load capacitance		–	–	50	pF
I_{DC}	DC current		–	–	–3.3	mA
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
BLAN						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA; V_{DD} = 4.5 V	1.1	–	–	V
V_{OH}	HIGH level output voltage	I_{OH} = 0 mA; V_{DD} = 5.5 V	–	–	2.8	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
ODD/$\overline{\text{EVEN}}$						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
$\overline{\text{COR}}$ AND Y (OPEN DRAIN)						
V_{OH}	pull-up voltage at pin		–	–	V_{DD}	V
V_{OL}	output voltage LOW	I_{OL} = 5 mA	0	–	1.0	V
C_L	load capacitance		–	–	25	pF
t_f	output fall time	load resistor of 1.2 kΩ to V_{DD}; measured between V_{DD} –0.5 and 1.5 V	–	–	50	ns
I_{LO}	output leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
T_{SK}	skew delay between display outputs R, G, B, $\overline{\text{COR}}$, Y and BLAN		–	–	20	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing						
DRAM INTERFACE						
t_{RC}	read or write cycle time		344	380	415	ns
t_{RP}	$\overline{RAS}$ precharge time		125	140	155	ns
t_{RAS}	$\overline{RAS}$ pulse width		194	210	230	ns
t_{CAS}	$\overline{CAS}$ pulse width		113	133	153	ns
t_{ASR}	row address set-up time		30	60	80	ns
t_{RAH}	row address hold time		50	60	92	ns
t_{ASC}	column address set-up time		50	60	75	ns
t_{CAH}	column address hold time		50	60	70	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time		130	148	160	ns
t_{RAD}	$\overline{RAS}$ to column address delay time		60	74	105	ns
t_{RSH}	$\overline{RAS}$ hold time		15	60	70	ns
t_{CSH}	$\overline{CAS}$ hold time		260	286	300	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time		60	70	80	ns
t_{DZC}	$\overline{CAS}$ set-up time from data input		200	225	280	ns
t_T	rise and fall times		10	15	20	ns
t_{WCS}	write set-up time		193	212	235	ns
t_{WCH}	write command hold time		116	137	150	ns
t_{DS}	data input set-up time		193	212	235	ns
t_{DH}	data input hold time		42	62	80	ns
t_{RAC}	access time from $\overline{RAS}$		165	183	220	ns
t_{CAC}	access time from $\overline{CAS}$		0	35	40	ns
$\hat{t}_{AA}$	access time from address		95	108	120	ns
t_{RCS}	read command set-up time		193	212	235	ns
t_{RCH}	read command hold time to $\overline{CAS}$		0	10	20	ns
t_{RRH}	read command hold time to $\overline{RAS}$		55	65	100	ns
t_{RAL}	column address to $\overline{RAS}$ lead time		90	133	150	ns
t_{OFF1}	output buffer turn-off time		20	30	40	ns
t_{CDD}	$\overline{CAS}$ to data input delay time		25	35	45	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-BUS						
t_{LOW}	clock LOW period		4	–	–	µs
t_{HIGH}	clock HIGH period		4	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		170	–	–	ns
$t_{SU;STO}$	set-up time from clock HIGH to STOP		4	–	–	µs
t_{BUF}	START set-up time following a STOP		4	–	–	µs
$t_{HD;STA}$	START hold time		4	–	–	µs
$t_{SU;STA}$	START set-up time following clock LOW-to-HIGH transition		4	–	–	µs

Notes to the characteristics

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. Series current limiting resistors must be used to limit the input currents to ± 1 mA.
2. RGBREF is the positive supply for the RGB output pins and it must be able to source the I_{OH} current from the R, G and B pins. The leakage specification on RGBREF only applies when there is no current load on the RGB pins.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

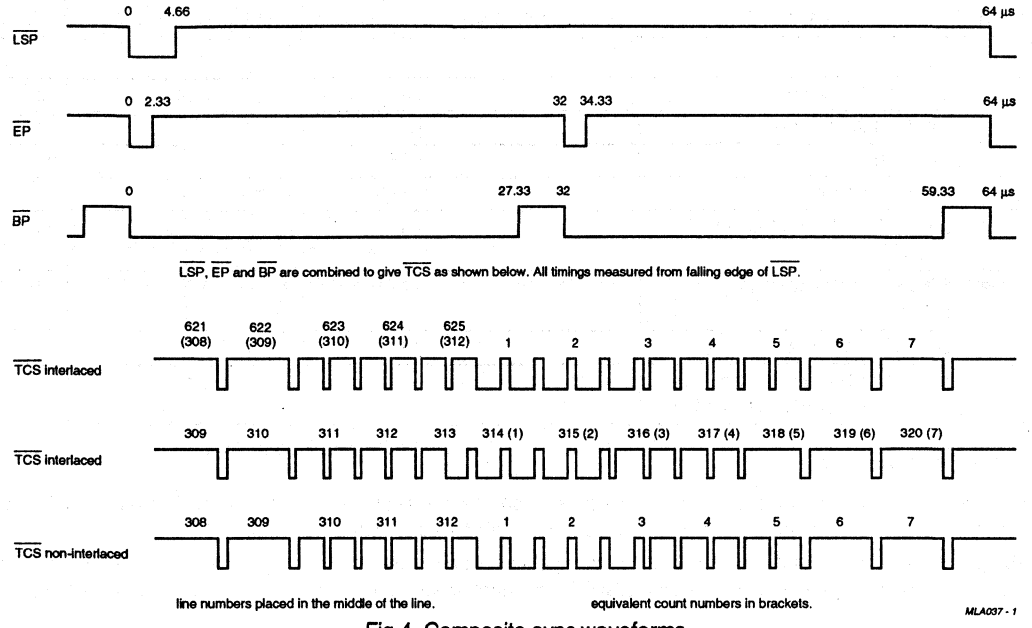


Fig.4 Composite sync waveforms.

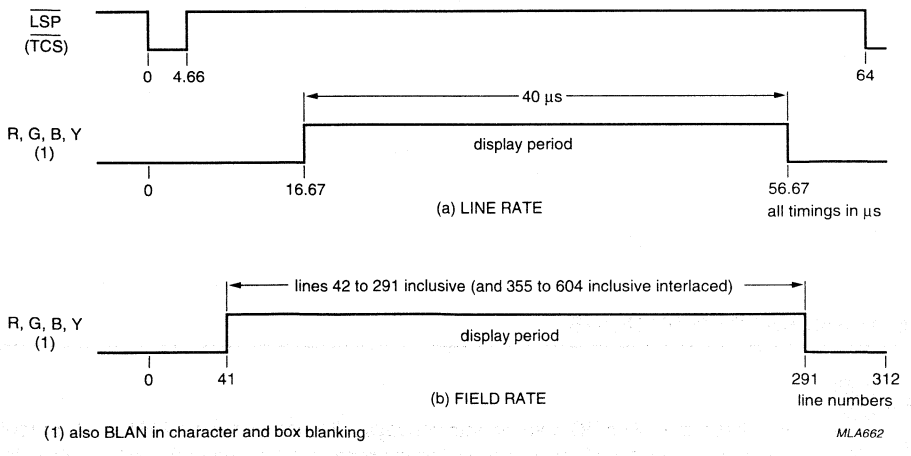


Fig.5 Display output timing (a) line rate (b) field rate.

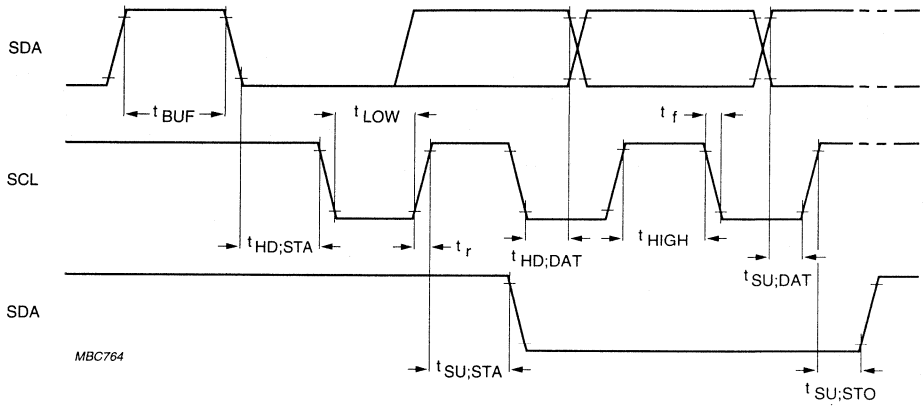


Fig.6 I²C-bus timing.

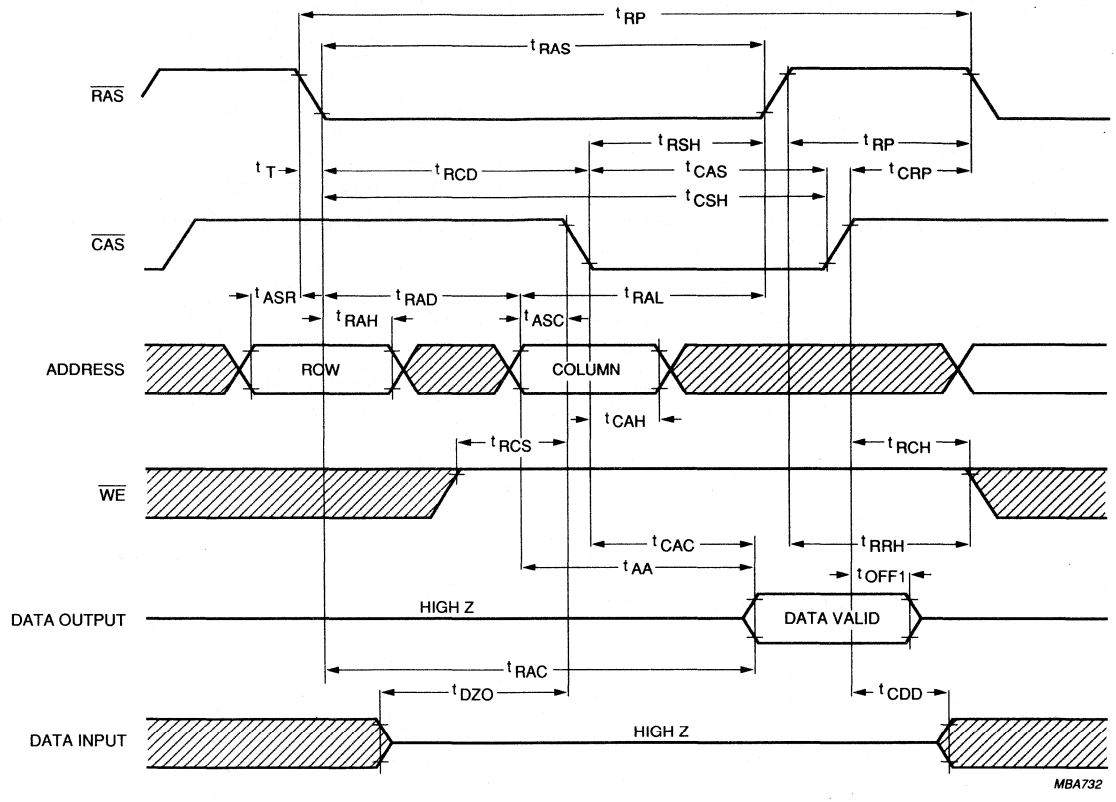


Fig.7 DRAM interface timing; read cycle.

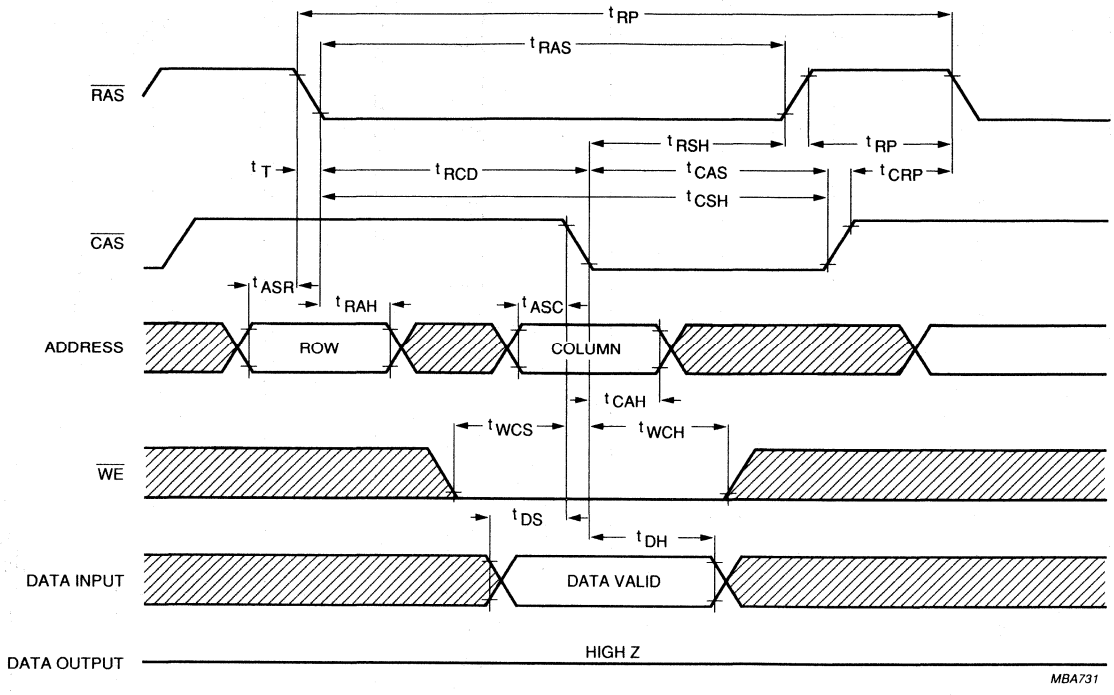


Fig.8 DRAM interface timing; write cycle.

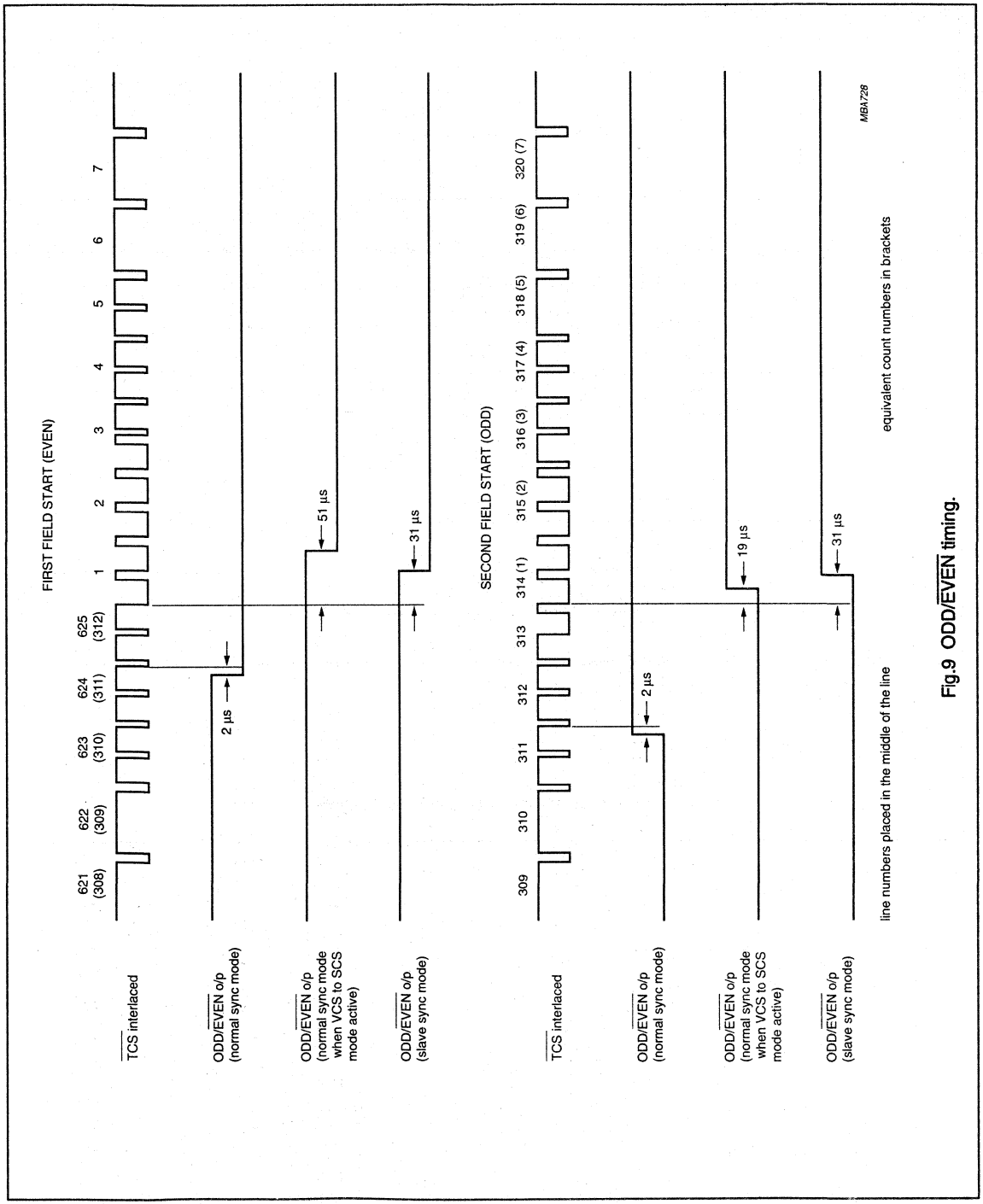


Fig.9 ODD/$\overline{\text{EVEN}}$ timing.

APPLICATION INFORMATION

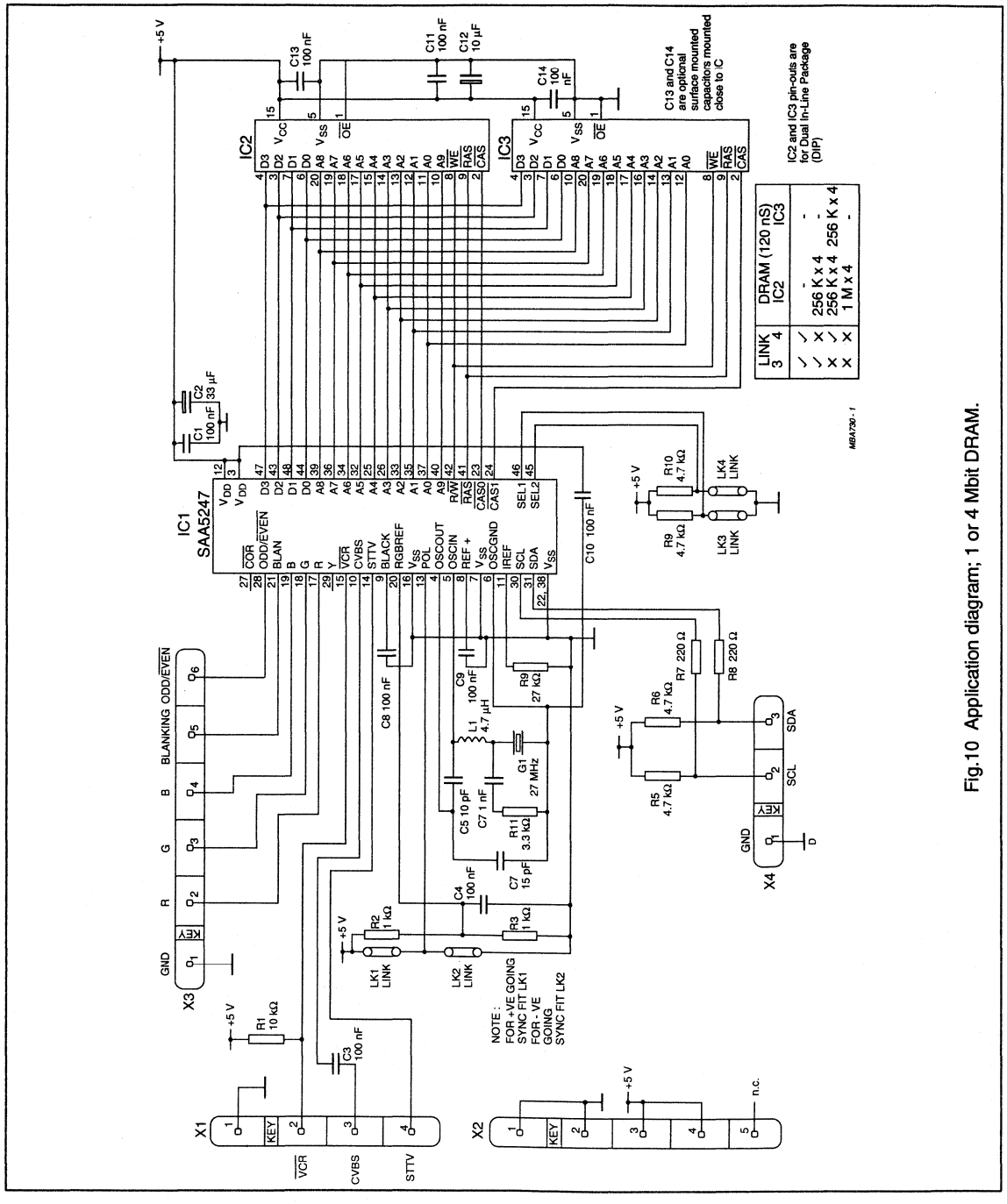


Fig.10 Application diagram; 1 or 4 Mbit DRAM.

IVT1.1BMC page memory organization

The organization of the page memory is illustrated by Fig.11. The IVT1.IBMC provides an additional row as compared with first generation decoders; this brings the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page; Row 24 is the extra row available for software generated status messages and FLOF/FASTEXT prompt information.

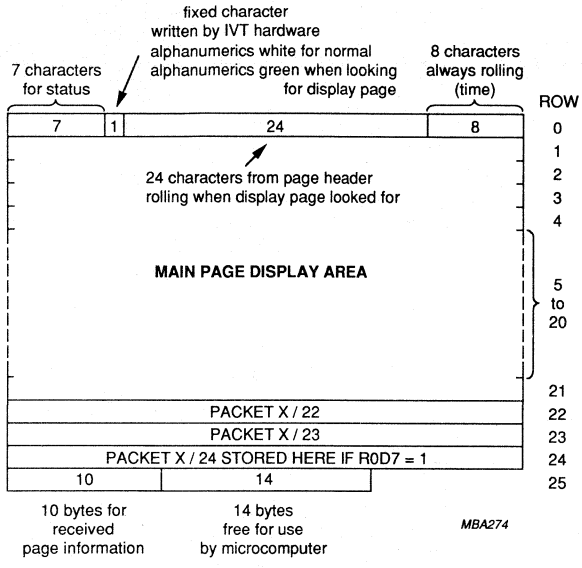


Fig.11 Basic page memory organization.

Note to Fig.11

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by IVT1.1BMC to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of Row 25 contain control data relating to the received page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

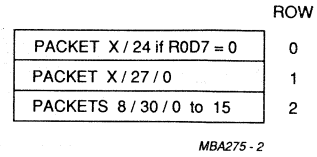


Fig.12 Organization of the extension memory.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

Page number

MAG magazine
PU page units
PT page tens

PBLF page being looked for
$\overline{\text{FOUND}}$ LOW for page has been found
HAM.ER Hamming error in corresponding byte

Page sub-code

MU minutes units
MT minutes tens
HU hours units
HT hours tens

C4-C14 transmitted control bits.

Register maps

IVT1.1BMC mode registers R0 to R11 are shown in Table 2. R0 to R10 are WRITE only; R11 is READ/WRITE. Register map (R3), for page requests, is shown in detail in Table 3.

Table 2 Register map

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
Adv. control	0	X24 POS	FREE RUN PLL	AUTO ODD/$\overline{\text{EVEN}}$	DISABLE HDR ROLL	DISPLAY STATUS ROW ONLY	DISABLE ODD/$\overline{\text{EVEN}}$	–	$\overline{\text{R11}}$/R11B SELECT
Mode	1	VCS TO SCS	$\overline{7+P}$/ 8-BIT	ACQ $\overline{\text{ON}}$/OFF	–	$\overline{\text{DEW}}$/ FULL FIELD	TCS ON	T1	T0
Page request address	2	–	–	–	–	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request data	3	–	–	CLEAR B.M.	PRD4	PRD3	PRD2	PRD1	PRD0
		–	–	–	–	–	–	–	–
Display control (normal)	5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash /subtitle)	6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	7	STATUS $\overline{\text{BTM}}$ TOP	CURSOR ON	$\overline{\text{CONCEAL}}$ REVEAL ON	$\overline{\text{TOP}}$/BTM HALF	$\overline{\text{SINGLE}}$ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0
		–	–	–	–	–	–	–	–
Cursor row	9	SUPPL. BLAST	CLEAR MEM.	A0	R4	R3	R2	R1	R0
Cursor column	10	SUPPL. ROW 24	SUPPL. ROW 0	C5	C4	C3	C2	C1	C0
Cursor data	11	D7	D6	D5	D4	D3	D2	D1	D0
Device status	11B	$\overline{\text{625}}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	TEXT SIGNAL QUALITY	VCS SIGNAL QUALITY

Notes to Table 2

1. – indicates these bits are inactive and must be written to logic 0 for future compatibility.
2. All bits in registers R0 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of Registers R1, R5 and R6 which are set to logic 1.
3. All memory is cleared to 'space' (00100000) on power-up, except Row 0 Column 7 Chapter 0, which is 'alpha' white (00000111) as the acquisition circuit is enabled but the page is on hold.
4. TB must be set to logic 0 for normal operation.
5. The I²C slave address is 0010001

Register description

R0 ADVANCED CONTROL - auto increments to Register 1

$\overline{R11}$/R11B SELECT	Selects reading of R11 or R11B
DISABLE ODD/$\overline{EVEN}$	Forces ODD/$\overline{EVEN}$ output LOW when logic 1
DISPLAY STATUS ROW	When SET = 1 and R1D6 = 1 open (8-bit mode) then all the text display is blanked out apart from the status row, this allows the page memory to be used for non-textural data, such as in the German top system.
DISABLE HDR ROLL	Disables green rolling header and time
AUTO ODD/$\overline{EVEN}$	When set forces ODD/$\overline{EVEN}$ low if any TV picture displayed, if DISABLE ODD/$\overline{EVEN}$ = 0
FREE RUN PLL	Will force the PLL to free run in all conditions
X24 POS	Automatic display of FASTEXT prompt row when logic 1

R1 MODE - auto increments to Register 2

T0, T1	Interlace/non-interlace 312/313 line control (see Table 4)
TCS ON	Text composite sync or direct sync select
$\overline{DEW}$/FULL FIELD	Field-flyback or full channel mode
ACQ $\overline{ON}$/OFF	Aquisition circuits turned off when logic 1
$\overline{7+P}$/8-BIT	7 bits with parity checking or 8-bit mode.
VCS TO SCS	When logic 1 enables display of messages with 60 Hz input signal

R2 PAGE REQUEST ADDRESS - auto increments to Register 3

COL SC0 - SC2	Point to start column for page request data (see Table 3)
TB	Must be logic 0 for normal operation

R3 PAGE REQUEST DATA - does not auto increment (see Table 3)

CLEAR B.M.	When set to logic 1. Useful when transmission increase channel changes.

R5 NORMAL DISPLAY CONTROL - auto increments to Register 6

R6 NEWSFLASH/SUBTITLE DISPLAY CONTROL - auto increments to Register 7

PON	Picture on
TEXT	Text on
COR	Contrast reduction on
BKGND	Background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 DISPLAY MODE - does not auto increment

BOX ON 0	Boxing function allowed on Row 0
BOX ON 1-23	Boxing function allowed on Row 1-23
BOX ON 24	Boxing function allowed on Row 24
DOUBLE HEIGHT	To display double height text
BOTTOM HALF	To select bottom half of page when DOUBLE HEIGHT = 1
REVEAL ON	To reveal concealed text
CURSOR ON	To display cursor
STATUS TOP	Row 25 displayed above or below the main text

R9 CURSOR ROW - auto increments to Register 10

R0 to R4	Active row for data written to or read from memory via the I²C-bus
A0	Selects display memory page (when = 0) or extension packet memory (when = 1)
CLEAR MEM.	When set to 1, clears the display memory. This bit is automatically reset
SUPPL. BLAST	When set to 1, Column S4 and S5 (of Table 5) are mapped into 4 and 5 respectively, replacing blast-through alphanumerics in graphics mode

R10 CURSOR COLUMN - auto increments to Register 11 or 11B

C0 to C5	Active column for data written to or read from memory via the I²C-bus
SUPPL. ROW 0	When set to 1, Column S4 and S5 (of Table 5) are mapped into Columns 6 and 7 respectively, just for Row 0 Columns 0 to 7
SUPPL. ROW 24	When set to 1, Column S4 and S5 (of Table 5) are mapped into Columns 6 and 7 respectively just for Row 24

R11 CURSOR DATA - does not auto increment

D0 to D6	Data read from/written to memory via I²C, at location pointed to by R9 and R10. This location automatically increments each time R11 is accessed

R11B DEVICE STATUS - does not auto increment

VCS SIGNAL QUALITY	Indicates that the video signal quality is good and PLL is phase locked to input video when = 1
TEXT SIGNAL QUALITY	If a good teletext signal is being received when = 1
ROM VER R0 to R4	Indicated language/ROM variant. For Western European = 01001
$\overline{625}$/525 SYNC	If the input video is a 525 line signal when = 1

Table 3 Register map for page requests (R3)

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

1. Abbreviations are as for Table 1 except for DO CARE bits.
2. When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
3. If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
4. Columns auto-increment on successive I²C-bus transmission bytes.

Table 4 Interlace/non-interlace 312/313 line control (T0 and T1)

T1	T0	RESULT
0	0	interlaced 312.5/312.5 lines
0	1	non-interlaced 312/313 lines (note 1)
1	0	non-interlaced 312/312 lines (note 1)
1	1	SCS mode (scan composite sync)

Note to Table 4

1 Reverts to interlaced mode if a newsflash or subtitle is being displayed.

CLOCK SYSTEMS

Crystal oscillator

The crystal is a conventional 2-pin design operating at 27 MHz. It is capable of oscillating with both fundamental and third overtone mode crystals. External components should be used to suppress the fundamental output of the third overtone as illustrated in Fig.13.

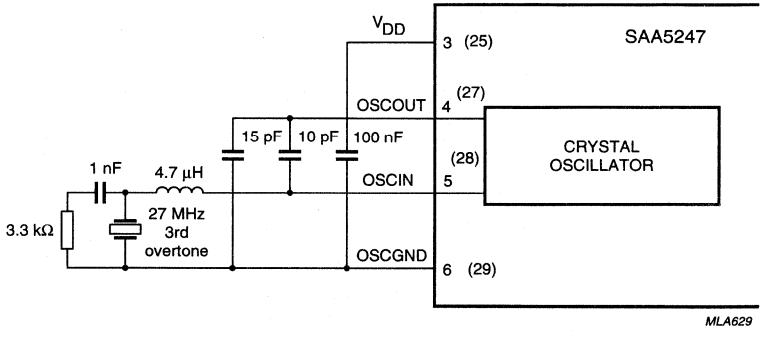


Fig.13 Crystal oscillator application diagram for SOT240; pins in parenthesis are for SOT208.

Table 5 Crystal characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Crystal (27 MHz, 3rd overtone)					
C1	series capacitance	–	1.7	–	pF
C0	parallel capacitance	–	5.2	–	pF
C_L	load capacitance	–	20	–	pF
Rr	resonant resistance	–	–	50	Ω
R1	series resistance	–	20	–	Ω
Xa	ageing	–	–	±5	10^{-6}/yr
Xj	adjustment tolerance	–	–	±25	10^{-6}
Xd	drift	–	–	±25	10^{-6}

Character sets

The WST specification allows the selection of national character sets via the page header transmission bits, C12 to C14. The basic 96 character sets differ only in 13 national option characters as indicated in Table 7 with reference to their table position in the basic character matrix illustrated in Table 6. The IVT1.1BMC automatically decodes transmission bits C12 to C14. Table 5 illustrates the character matrixs.

Character bytes are listed as transmitted from b1 to b7.

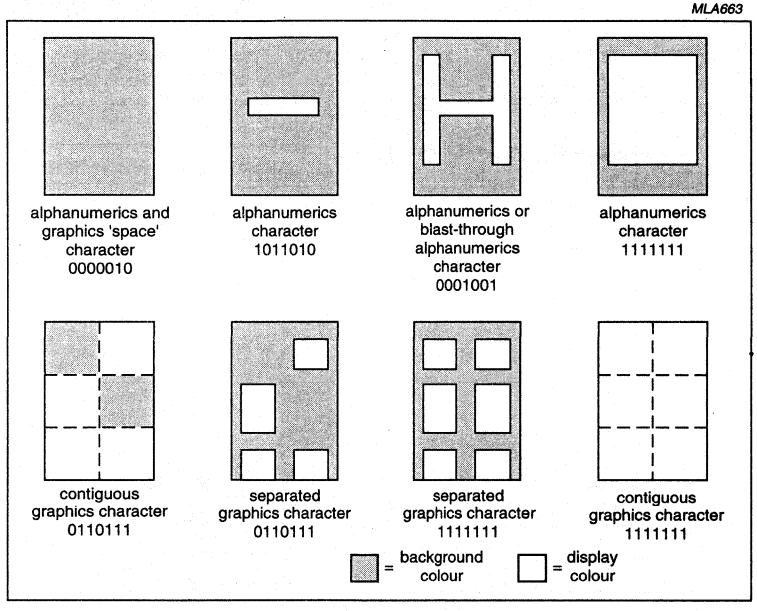
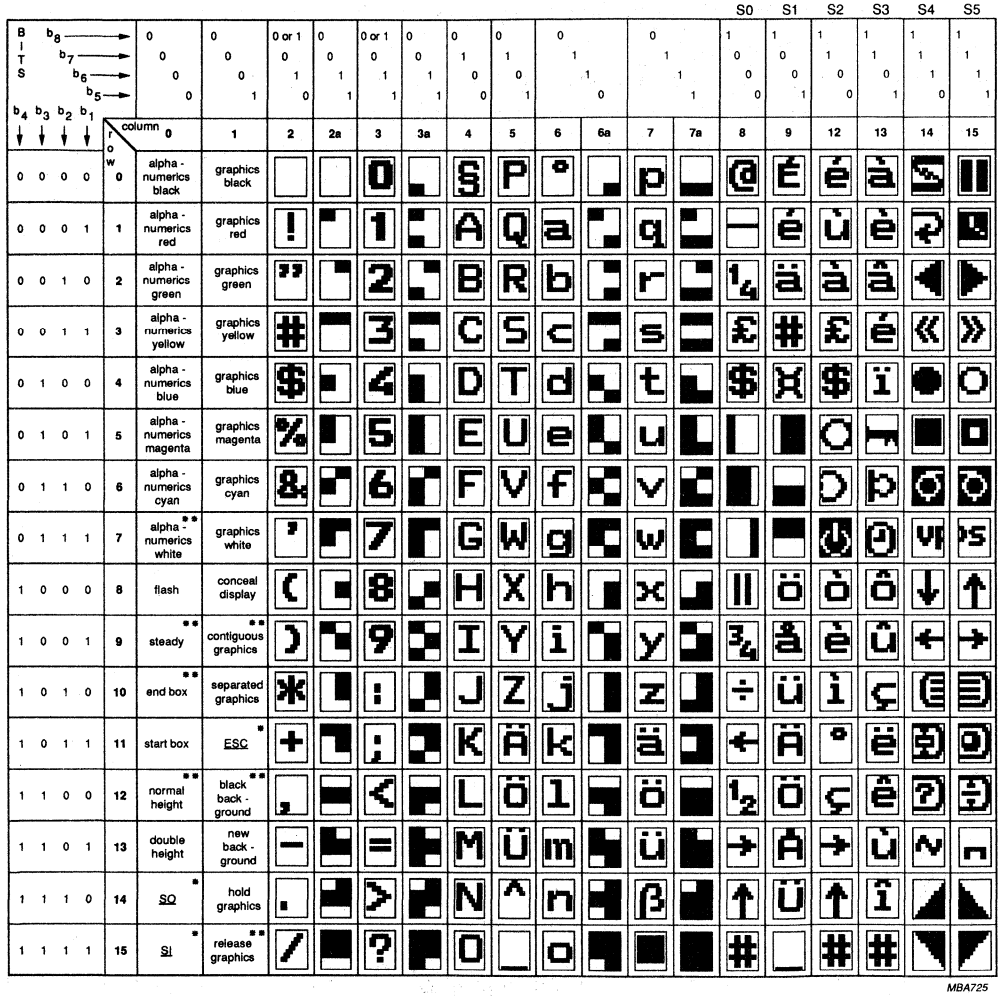


Fig.14 Character format.

Table 5 SAA5247P/B character data input decoding



For character version number (01001) see Register 11B.

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Notes to Table 5

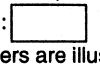
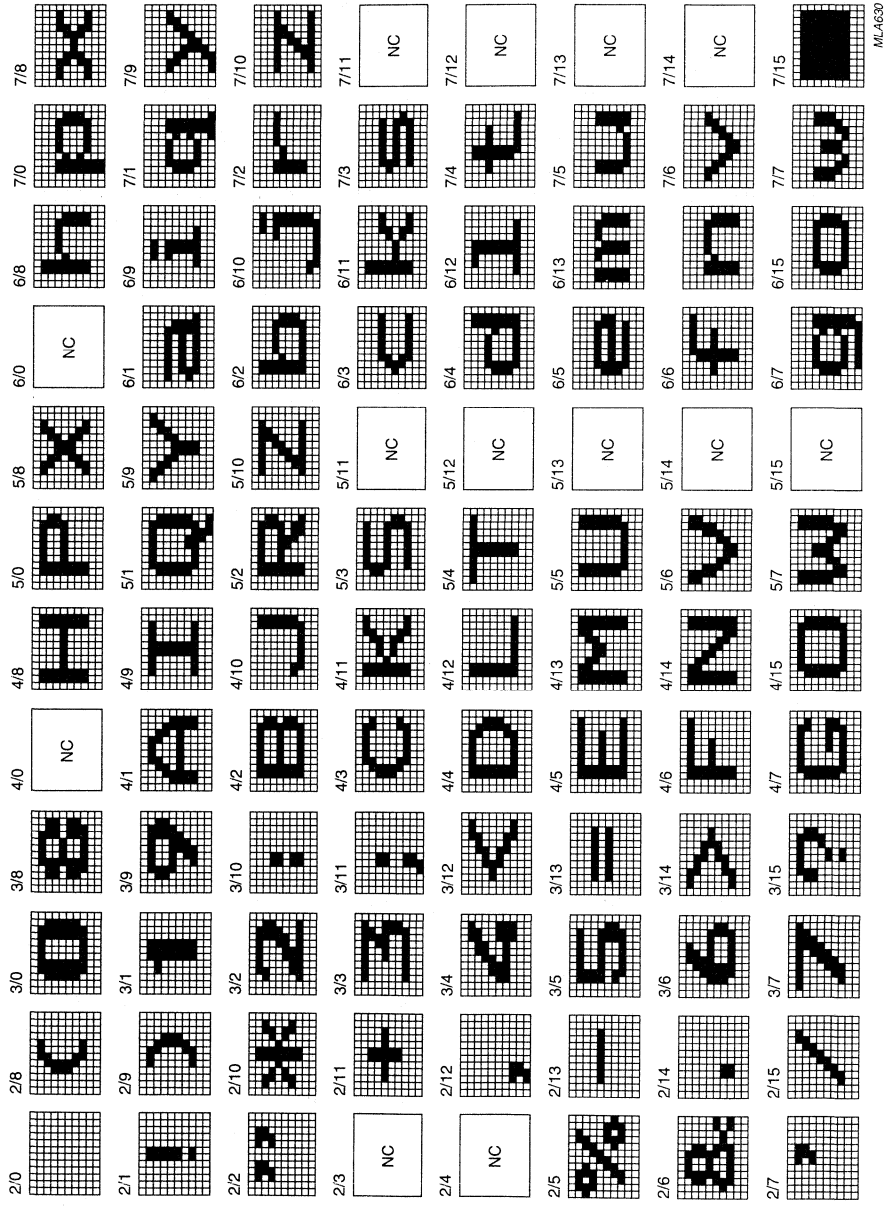
1. Control characters shown in Columns 0 and 1 are normally displayed as spaces.
2. Characters may be referred to by column and row, For example 2/5 refers to %.
3. Black represents displayed colour. White represents backgound.
4. Character rectangle shown as follows: 
5. The SAA5247 national option characters are illustrated in Table 7.
6. Characters S4/11, S4/12, S5/10, S5/11 and S5/12 are special characters for combining with character S4/10.
7. National option characters will be developed according to the setting of control bits C12 to C14. These will be mapped into the basic code table into positions shown in Table 7. Therefore columns S0, S1, S2 and S3 are mapped into the basic code table as national options for English, Swedish, Italian and French respectively.
8. Columns S4 and S5 are mapped into Columns 6 and 7 respectively when enabled by R10 bit D6 (Row 0 Columns 0 to 7) and R10 bit D7 (row 24) set to 1.
9. Columns 2a, 3a, 6a and 7a are displayed in graphics mode.
8. Columns S4 and S5 replace columns 4 and 5 respectively when enabled by R9 bit D7 set to 1.
9. Columns S4 and S5 are directly accessible with column address 1110 and 1111 respectively.

Table 6 SAA5247 basic character matrix



Where: NC = national option character position.

Table 7 SAA5247 national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç

MLA664

(1) PHCB are the Page Header Control Bits. Other combinations default to English.

Single-chip Teletext and VPS decoder (IVT1.0VPS)

SAA5248

FEATURES

- Complete Teletext and VPS decoder in a 52-pin shrink DIL, or 64-pin QFP, integrated circuit
- Separate storage of VPS data (PDC System A) and packet 8/30/2 data (PDC System B) allowing dual standard VPT decoders
- Data valid output available to indicate reception of error-free VPS or packet 8/30/2 data.
- Packet 8/30/2 stored separately from other packets 8/30
- Software compatible with SAA5246 (apart from new VPS features).
- Hardware compatible with the SAA5246 teletext decoder.
- Single +5 V power supply
- Both video and scan related synchronization modes are supported
- RGB interface to standard colour decoder ICs, push-pull output drive
- Digital data slicer and display clock phase-locked loop reduce peripheral components to a minimum
- Data capture performance similar to SAA5231 (VIP2)
- Option for up to seven national languages
- Optional storage of packet 24 in the display memory
- Separate text and video signal quality detectors, 625/525 video status and language version all readable via I²C-bus
- Automatic $\overline{\text{ODD}}$/EVEN output control with override
- Control of display PLL free-run and rolling header via I²C-bus
- VCS to SCS mode for stable 525 line status display

DESCRIPTION

The SAA5248 is a single-chip teletext decoder IC for decoding 625 line base World System Teletext transmissions. The device is based on IVT1.0 (SAA5246) with the addition of reception facilities for the 2.5 MHz biphase VPS signal. It is intended for use in video recorders, in particular to implement the VPT facility (VCR Programming via Teletext). With suitable software, both VPT standards (EBU PDC System A and System B) can be accommodated to allow operation from any European VPT transmission.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5248ZP/E	52	SDIL	plastic	SOT247
SAA5248GP/E	64	QFP	plastic	SOT208

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	65	130	mA
V_{syn}	sync amplitude	0.1	0.3	0.6	V
V_{vid}	video amplitude	0.7	1.0	1.4	V
f_{XTAL}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature range	–20	–	+70	°C

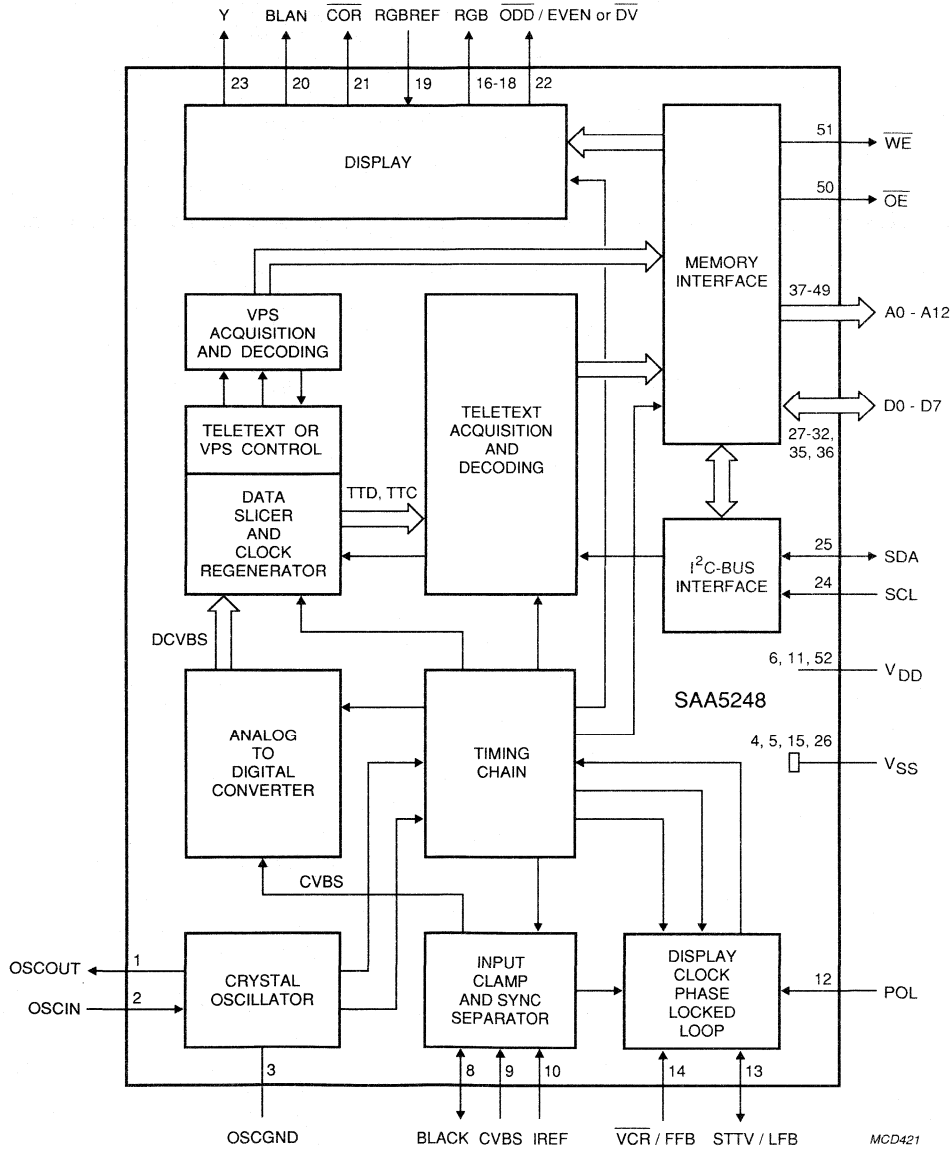


Fig.1 Block diagram for SOT247 (SDIL52) package.

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT 247	SOT208	
OSCOUT	1	27	27 MHz crystal oscillator output
OSCIN	2	28	27 MHz crystal oscillator input
OSCGND	3	29	0 V crystal oscillator ground
V_{SS}	4, 5, 15, 26	26, 30, 31, 43, 58	0 V ground
n.c.	7	-	not connected
BLACK	8	35	video black level storage pin, connected to ground via a 100 nF capacitor
CVBS	9	36	composite video input pin. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor
IREF	10	37	reference current input pin, connected to ground via a 27 kΩ resistor
V_{DD}	6, 11, 52	25, 32, 38	+5 V positive supply
POL	12	39	STTV/LFB/FFB polarity selection pin
STTV/LFB	13	40	sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode)
$\overline{VCR}$/FFB	14	42	PLL time constant switch/field input pin. Function controlled by an internal register bit (scan sync mode)
R	16	44	dot rate character output of the RED colour information
G	17	45	dot rate character output of the GREEN colour information
B	18	47	dot rate character output of the BLUE colour information
RGBREF	19	48	input DC voltage to define the output high level on the RGB pins
BLAN	20	52	dot rate fast blanking output
$\overline{COR}$	21	53	programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages. Open-drain output
$\overline{ODD}$/EVEN or $\overline{DV}$	22	54	In $\overline{ODD}$/EVEN mode a 25 MHz output synchronized to the input CVBS field sync pulses to make a non-interlaced display by adjustment of the vertical deflection currents. In $\overline{DV}$ mode a VPT data valid signal used to indicate reception of error-free VPS or 8/30/ format 2 data
Y	23	55	dot rate character output of teletext foreground colour information. Open-drain output
SCL	24	56	serial clock input for I²C-bus. It can still be driven HIGH during power-down of the device
SDA	25	57	serial data port for the I²C-bus. Open drain output. It can still be driven HIGH during power-down of the device

SYMBOL	PIN		DESCRIPTION
	SOT 247	SOT208	
D0-D5	27-32	60 - 64, 3	data ports for the page RAM
n.c.	33, 34	1, 2, 10, 11, 15, 18, 33, 34, 41, 46, 49 - 51, 59	not connected
D6-D7	35, 36	4, 5	data ports for the page RAM
A0-A12	37-49	6-9, 12-14, 16, 17, 19-22	address output for the page SRAM
$\overline{OE}$	50	23	output enable for the page SRAM
$\overline{WE}$	51	24	write enable for the page SRAM

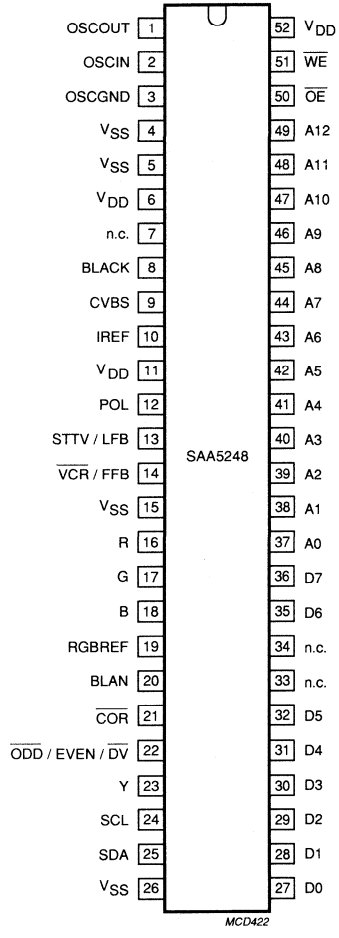


Fig.2 Pin configuration; SOT247 (SDIL52).

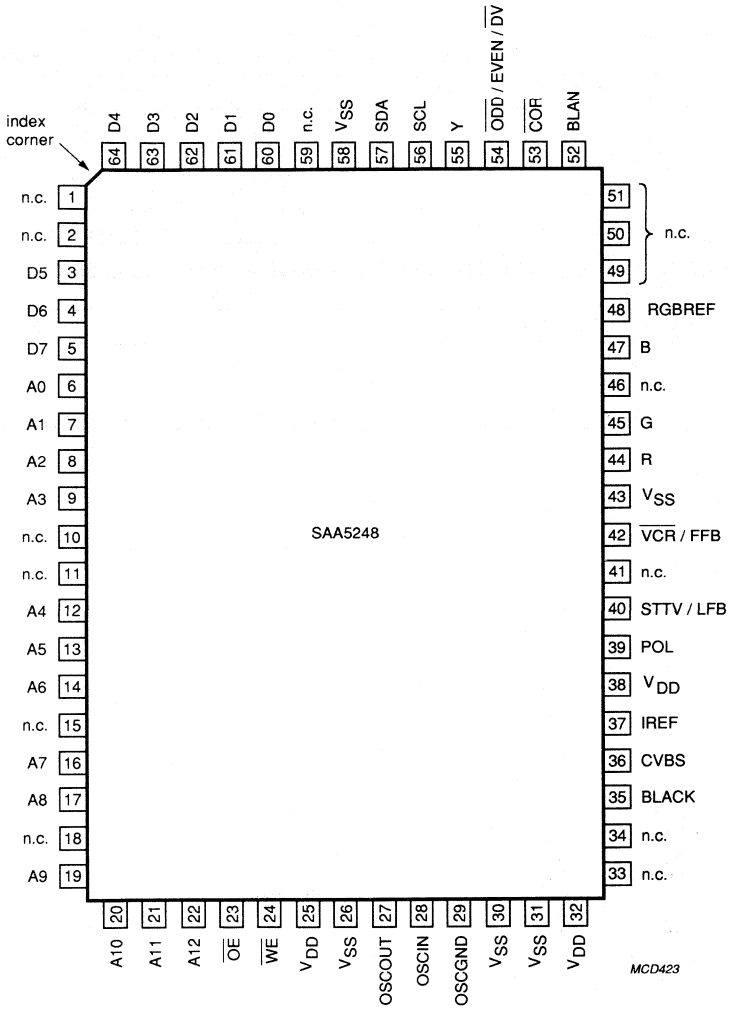


Fig.3 Pin configuration; SOT248 (QFP64).

LIMITING VALUES

In accordance with Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	−0.3	6.5	V
V_I	input voltage (any input)	−0.3	V_{DD} +0.5	V
V_O	output voltage (any output)	−0.3	V_{DD} +0.5	V
I_O	output current (each output)	−	±10	mA
I_{IOK}	DC input or output diode current	−	±20	mA
T_{amb}	operating ambient temperature range	−20	+70	°C
T_{stg}	storage temperature range	−55	+125	°C
V_{stat}	electrostatic handling (see note)	−2000	+2000	V

Note

Electrostatic handling is equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor with a 15 ns rise time.

Failure Rate

The failure rate at T_{amb} = 55 °C will be a maximum of 1000 FITS (1 FIT = 1 x 10^{-9} failures per hour).

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = −20 to +70 °C, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage range		4.5	5.0	5.5	V
I_{DD}	total supply current		–	65	130	mA
Inputs						
CVBS						
V_{syn}	sync amplitude		0.1	0.3	0.6	V
t_{syn}	delay from CVBS to TCS output from STTV buffer (nominal video, average of leading/trailing edge)		−150	0	+150	ns
t_{syd}	change in sync delay between all black and all white video input at nominal levels		0	–	25	ns
$V_{vid(p-p)}$	video input amplitude (peak-to-peak)		0.7	1.0	1.4	V
	display PLL catching range		±7	–	–	%
Z_{src}	source impedance		–	–	250	Ω
C_I	input capacitance		–	–	10	pF
IREF						
R_g	resistor to ground		–	27	–	kΩ
POL						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
LFB						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
I_I	input current	note 1	−1	–	+1	mA
t_{LFB}	delay between LFB front edge and input video line sync		–	250	–	ns
$\overline{VCR}$/FFB						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
I_I	input current	note 1	−1	–	+1	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
RGBREF						
V_{IL}	LOW level input voltage		−0.3	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
I_{DC}	DC current		–	–	10	mA
SCL						
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
f_{SCL}	clock frequency		0	–	100	kHz
t_r	input rise time	10% to 90%	–	–	2	µs
t_f	input fall time	90% to 10%	–	–	2	µs
C_I	input capacitance		–	–	10	pF
Inputs/outputs						
CRYSTAL OSCILLATOR (OSCIN; OSCOUT)						
f_{XTAL}	crystal frequency		–	27	–	MHz
V_{OSC}	oscillation amplitude (peak-to-peak value)		–	1.5	–	V
G_v	small signal voltage gain		–	1	–	V/V
G_m	mutual conductance		5	–	–	mA/V
C_I	input capacitance		–	–	10	pF
C_{FB}	feedback capacitance		–	1	–	pF
BLACK						
C_{blk}	storage capacitor to ground		–	100	–	nF
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
SDA						
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
t_r	input rise time	10% to 90%	–	–	2	µs
t_f	input fall time	90% to 10%	–	–	2	µs
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.5	V
t_f	output fall time	3 V to 1 V	–	–	200	ns
C_L	load capacitance		–	–	400	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs/outputs						
D0 TO D7						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current		−10	–	+10	μA
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	2.4	–	V_{DD}	V
t_r	output rise time	0.6 V to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 V to 0.6 V	–	–	50	ns
C_L	load capacitance		–	–	120	pF
Outputs						
STTV						
G_{stt}	gain of STTV relative to video input		0.9	1.0	1.1	
V_{tcs}	TCS amplitude		0.2	0.3	0.45	V
V_{DCs}	DC shift between TCS output and nominal video output		–	–	0.15	V
I_O	output drive current		–	–	3.0	mA
C_L	load capacitance		–	–	100	pF
A0 TO A12 ADDRESS OUTPUT TO MEMORY						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 V to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 V to 0.6 V	–	–	50	ns
$\overline{OE}$, $\overline{WE}$						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 V to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 V to 0.6 V	–	–	50	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
R, G AND B						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.2	V
V_{OH}	HIGH level output voltage	I_{OH} = –1.6 mA; RGBREF ≤ V_{DD}–2 V	RGBREF –0.25 V	RGBREF	RGBREF +0.25 V	V
I_{DC}	DC current		–	–	–3.3	mA
$\|Z_o\|$	output impedance		–	–	200	Ω
C_L	load capacitance		–	–	50	pF
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
BLAN						
V_{OL}	LOW level output voltage	I_{OL} = 0.2 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA; V_{DD} = 4.5 V	1.1	–	–	V
V_{OH}	HIGH level output voltage	I_{OH} = 0 mA; V_{DD} = 5.5 V	–	–	2.8	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
$\overline{ODD}$/EVEN OR $\overline{DV}$						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –1.6 mA	V_{DD}–0.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
$\overline{COR}$ AND Y (OPEN DRAIN)						
V_{OH}	pull-up voltage at pin		–	–	V_{DD}	V
V_{OL}	LOW level output voltage	I_{OL} = +2 mA	0	–	0.4	V
V_{OL}	LOW level output voltage	I_{OL} = +5 mA	0	–	1.0	V
C_L	load capacitance		–	–	25	pF
t_f	output fall time	load resistor of 1.2 kΩ to V_{DD}; measured between V_{DD} –0.5 and 1.5 V	–	–	50	ns
I_{LO}	output leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
T_{SK}	skew delay between display outputs R, G, B, $\overline{COR}$, Y and BLAN		–	–	20	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing						
MEMORY INTERFACE						
t_{CY}	cycle time		–	500	–	ns
t_{OE}	address change to $\overline{OE}$ LOW		55	–	–	ns
t_{ADDR}	address active time		450	500	–	ns
t_{rOEW}	$\overline{OE}$ pulse width read		295	–	–	ns
t_{wOEW}	$\overline{OE}$ pulse width write		100	–	–	ns
t_{ACC}	access time from address data valid		–	–	150	ns
t_{DH}	data hold time from $\overline{OE}$ HIGH or address change		0	–	150	ns
t_{WEW}	$\overline{WE}$ pulse width		100	–	–	ns
t_{DS}	data set-up time to $\overline{WE}$ HIGH		60	–	–	ns
t_{DHWE}	data hold time from $\overline{WE}$ HIGH		20	–	–	ns
t_{WR}	write recovery time		20	–	–	ns
t_{DE}	data enable from $\overline{WE}$ LOW		60	–	–	ns
I^2C-BUS						
t_{LOW}	clock LOW period		4	–	–	µs
t_{HIGH}	clock HIGH period		4	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		170	–	–	ns
$t_{SU;STO}$	set-up time from clock HIGH to STOP		4	–	–	µs
t_{BUF}	START set-up time following a STOP		4	–	–	µs
$t_{HD;STA}$	START hold time		4	–	–	µs
$t_{SU;STA}$	START set-up time following clock LOW-to-HIGH transition		4	–	–	µs

Notes to the characteristics

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. Series current limiting resistors must be used to limit the input currents to ± 1 mA.
2. Can be pulled higher by external pull-up resistor, (maximum leakage current ≈200 µA).

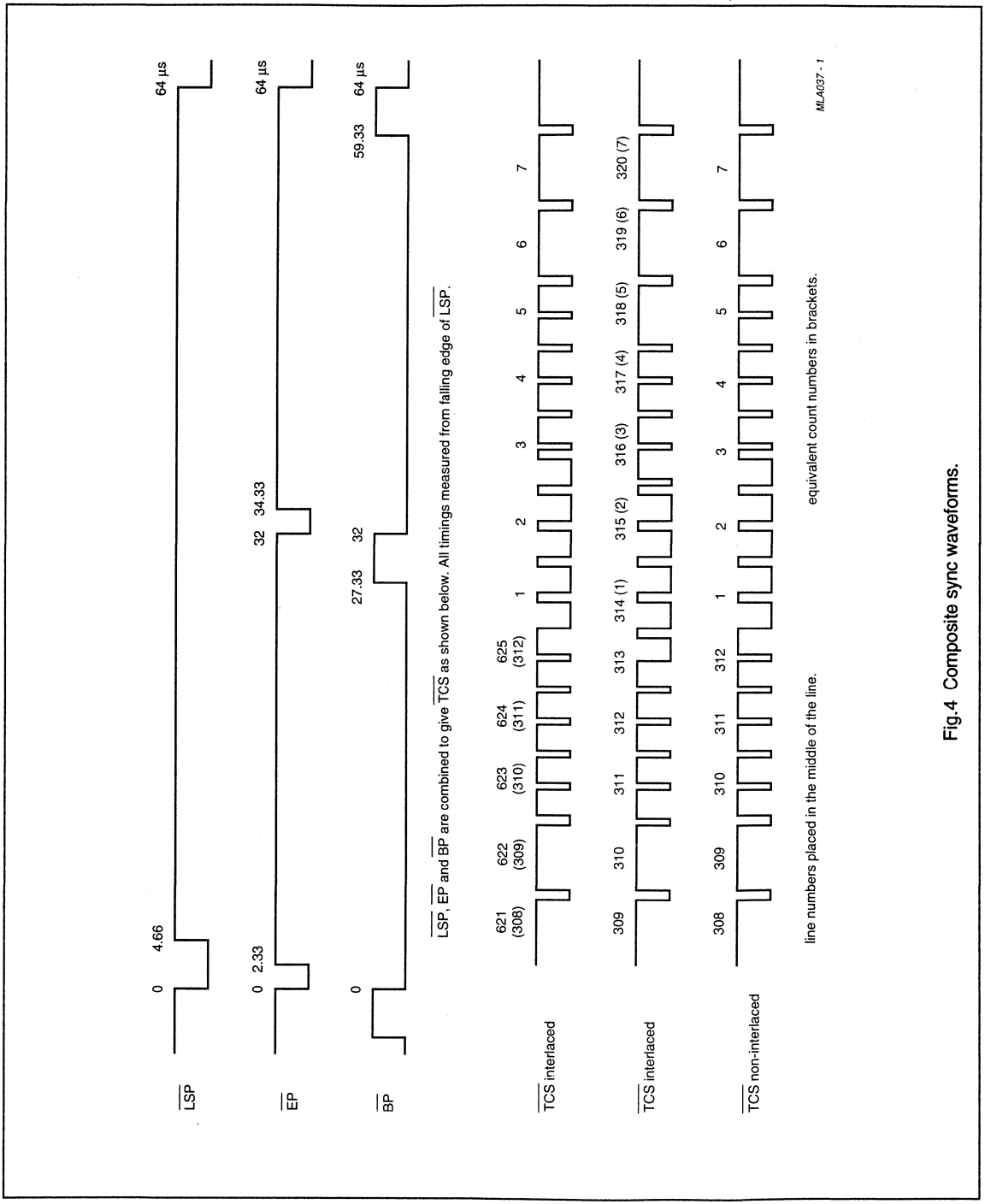


Fig.4 Composite sync waveforms.

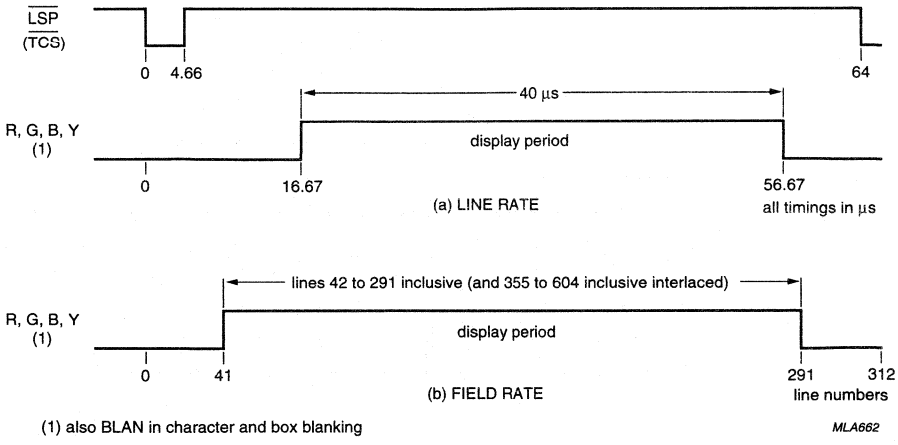


Fig.5 Display output timing (a) line rate (b) field rate.

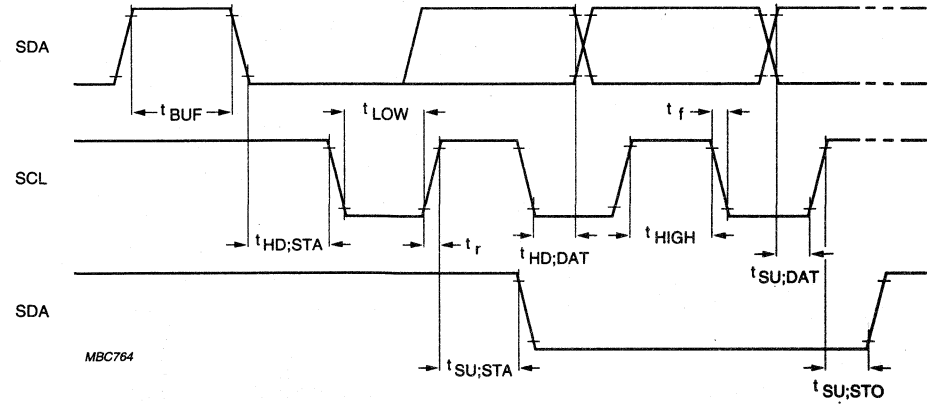


Fig.6 I²C-bus timing.

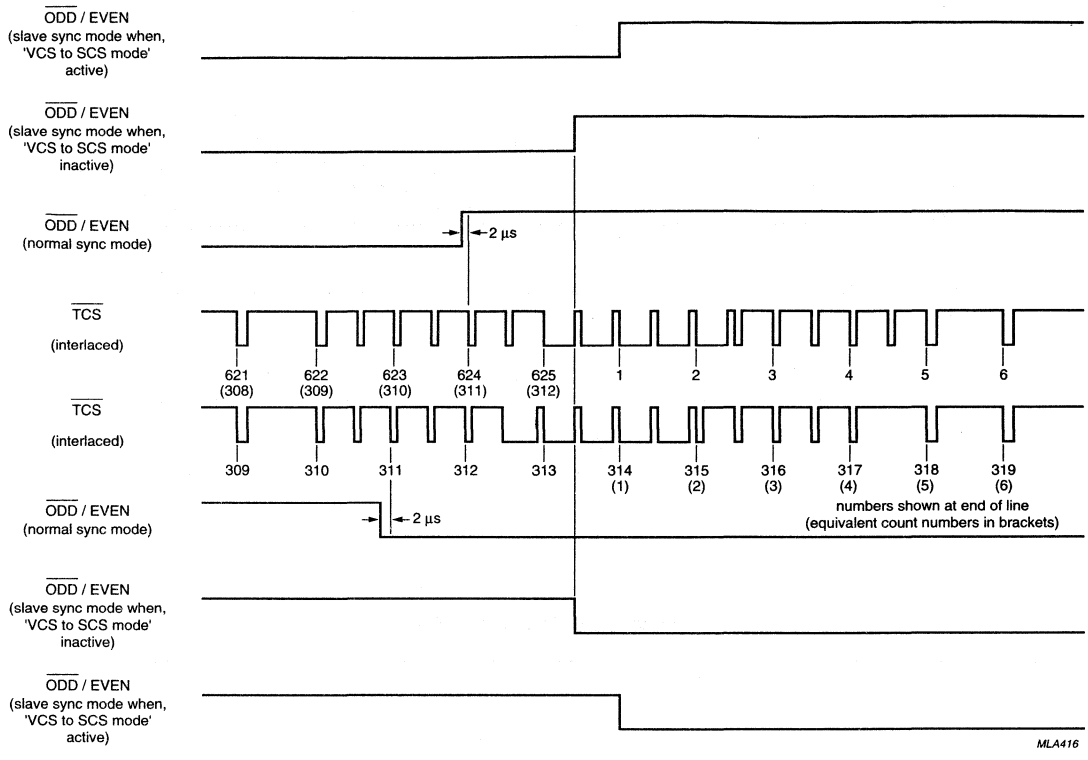


Fig.7 $\overline{\text{ODD}}$/EVEN timing.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

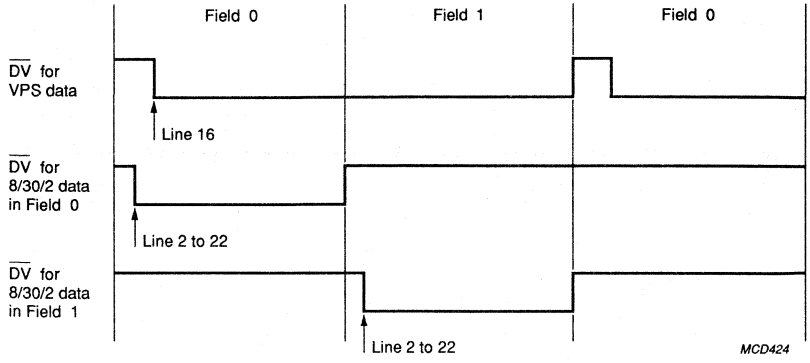
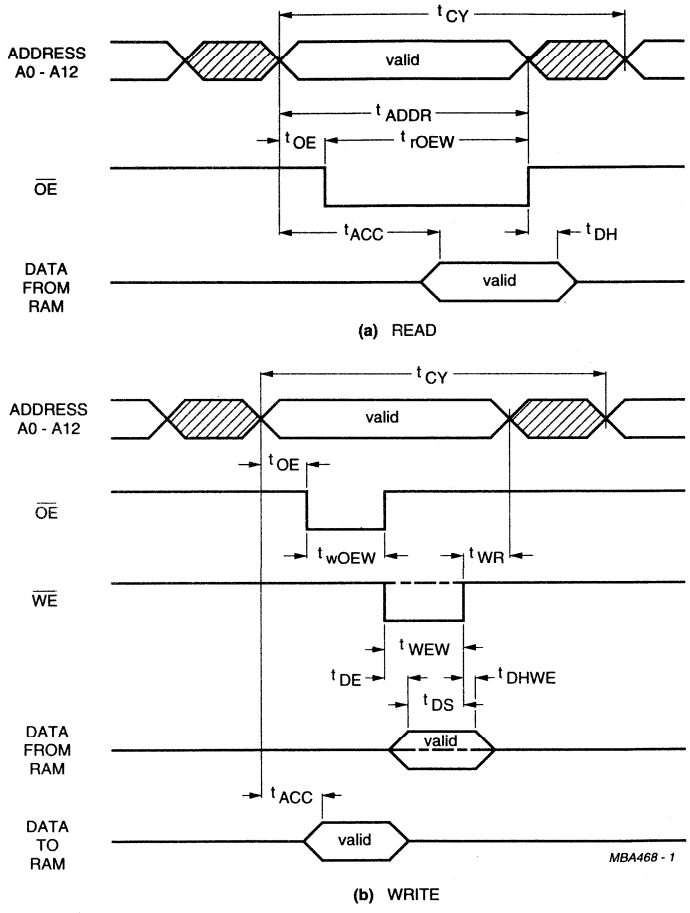


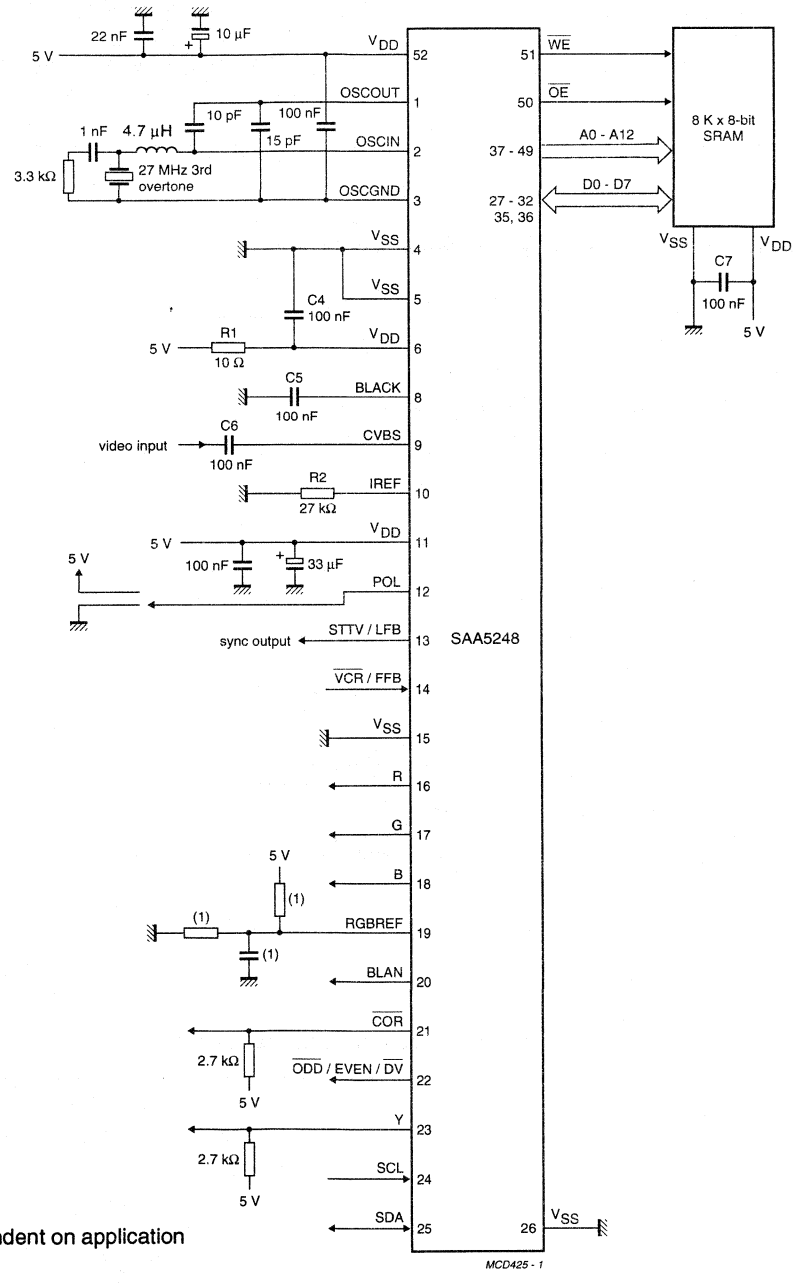
Fig.8 Data Valid timing ($\overline{DV}$).



_.._.._ Level during flicker stopped cycle.

Fig.9 Memory interface timing (a) read (b) write.

APPLICATION INFORMATION



(1) Value dependent on application

Fig.10 Application diagram.

SAA5248 page memory organization

The organization of the page memory is illustrated by Fig.11. The SAA5248 provides an additional row as compared with first generation decoders; this brings the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page; Rrow 24 is the extra row available for software generated status messages and FLOF/FASTEXT prompt information.

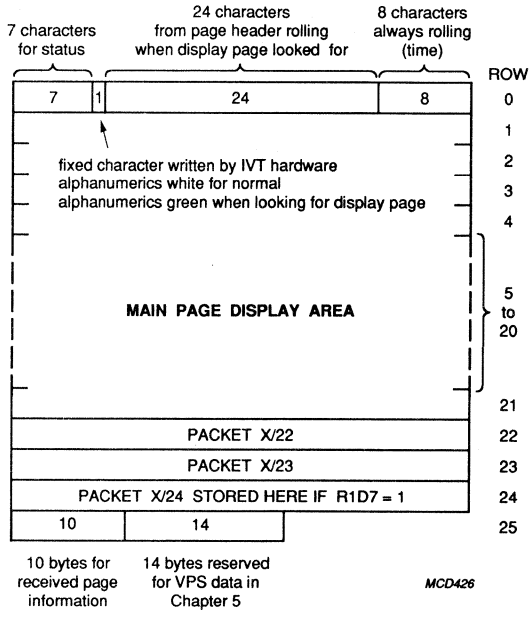


Fig.11 Basic page memory organization.

Note to Fig.11

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by SAA5248 to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of Row 25 contain control data relating to the received page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer, except in Chapter 5 (see Fig.13 where they are reserved for VPS data.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

Page number

MAG magazine
PU page units
PT page tens

PBLF page being looked for
$\overline{\text{FOUND}}$ LOW for page has been found
HAM.ER Hamming error in corresponding byte

When in extension packet enabled mode the rows of information are organized as illustrated by Fig.12.

Row 23 of the extension page, as shown in Fig.12, contains packet 8/30. Packet 8/30 is mapped into the SAA5248 memory as follows:

8/30/0 and 8/30/1 to Chapter 4 Row 23
8/30/2 and 8/30/3 to Chapter 5 Row 23
8/30/4 to 8/30/15 to Chapter 6 Row 23

Page sub-code

MU minutes units
MT minutes tens
HU hours units
HT hours tens

C4-C14 transmitted control bits.

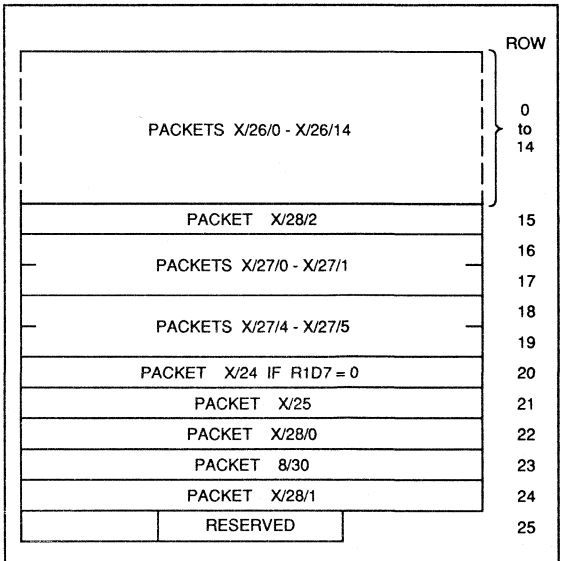


Fig.12 Organization of the extension memory.

VPT data memory organization

To simplify the software for dual-standard VPT decoders, the VPS data from line 16 is stored in Row 25 of Chapter 5 of the page memory, and is aligned to match the packet 8/30 format 2 data as far as possible.

Column	0	1	2	3	4	5	6	7	8	9	10	11
8/30/2 data Row 23 Chapter 5	D	INITIAL PAGE						b13	b14	b15	b16	b17
VPS data Row 25 Chapter 5	RECEIVED PAGE INFORMATION										B.11	

Column	12	13	14	15	16	17	18	19	20	21	22	23
8/30/2 data Row 23 Chapter 5	b18	b19	b20	b21	b22	b23	b24	b25	STATUS DISPLAY			
VPS data Row 25 Chapter 5	B.12		B.13		B.14		B.15		B.4		B.5	

Column	24 – 39
8/30/2 data Row 23 Chapter 5	STATUS DISPLAY CONTINUED

MCD428 - 1

Fig.13 Memory organization details.

Register maps

SAA5248 mode registers R0 to R11 are shown in Table 2. R0 to R10 are WRITE only; R11 is READ/WRITE. Register map (R3), for page requests, is shown in detail in Table 4.

Table 2 Register map

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
Adv. control	0	X24 POS	FREE RUN PLL	AUTO $\overline{ODD}$/ EVEN*	DISABLE HDR ROLL	–	DISABLE $\overline{ODD}$/ EVEN*	VCR MODE	$\overline{R11}$/R11B SELECT
Mode	1	VCS TO SCS	$\overline{7+P}$/ 8-BIT	ACQ $\overline{ON}$/OFF	EXT. PACKET ENABLE	$\overline{DEW}$/ FULL FIELD	TCS ON	T1	T0
Page request address	2	HAM. CHECK 27, 28, 8/30	BANK SELECT A2	ACQ CIRCUIT A1	ACQ CIRCUIT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request data	3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
Display chapter	4	–	–	–	–	–	A2	A1	A0
Display control (normal)	5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash /subtitle)	6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	7	STATUS TOP	CURSOR ON	REVEAL ON	BOTTOM HALF	DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0
Active chapter	8	–	–	–	VPS ENABLE	CLEAR MEM.	A2	A1	A0
Cursor row	9	–	–	–	R4	R3	R2	R1	R0
Cursor column	10	–	–	C5	C4	C3	C2	C1	C0
Cursor data	11	D7	D6	D5	D4	D3	D2	D1	D0
Device status	11B	$\overline{625}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	DATA QUALITY	VCS SIGNAL QUALITY

Where:

* Also used to enable Data Valid ($\overline{DV}$) output on $\overline{ODD}$/EVEN pin.

'–' Indicates a bit which does not exist and must be written to logic 0 for future compatibility.

Notes to Table 2

1. All bits in registers R0 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R1, R5 and R6 which are set to logic 1.
2. All memory is cleared to 'space' (00100000) on power-up, except Row 0 Column 7 Chapter 0, which is 'alpha' white (00000111) as the acquisition circuit is enabled but the page is on hold.
3. TB must be set to logic 0 for normal operation.
4. The I²C-bus slave address is 0010001

Register description

R0 ADVANCED CONTROL - auto increments to Register 1

$\overline{R11}$/R11B SELECT	Selects reading of R11 or R11B
VCR MODE	Selects short time constant of PLL when logic 1
DISABLE $\overline{ODD}$/EVEN	Forces $\overline{ODD}$/EVEN output LOW when logic 1 (see Table 3)
DISABLE HDR ROLL	Disables green rolling header and time
AUTO $\overline{ODD}$/EVEN	When set forces $\overline{ODD}$/EVEN low if any TV picture displayed, if DISABLE $\overline{ODD}$/EVEN = 0 (see Table 3)
FREE RUN PLL	Will force the PLL to free run in all conditions
X24 POS	Automatic display of FASTEXT prompt row when logic 1

R1 MODE - auto increments to Register 2

T0, T1	Interlace/non-interlace 312/313 line control (see Table 5)
TCS ON	Text composite sync or direct sync select
$\overline{DEW}$/FULL FIELD	Field-flyback or full channel mode
EXT. PACKET ENABLE	Allocates 2.8 k memory per chapter
ACQ $\overline{ON}$/OFF	Aquisition circuits turned off when logic 1
$\overline{7 + P}$/8-BIT	7 bits with parity checking or 8-bit mode
VCS TO SCS	When logic 1 enables display of messages with 60 Hz input signal

R2 PAGE REQUEST ADDRESS - auto increments to Register 3

HAM. CHECK 27 28 8/30	When logic 1 enables hamming checking of extension packet 27, 28, 8/30
COL SC0 - SC2	Point to start column for page request data (see Table 4)
TB	Must be logic 0 for normal operation
ACQ CIRCUIT	Selects one of four acquisition circuits
BANK SELECT	Selects which bank of four pages is being accessed

R3 PAGE REQUEST DATA - does not auto increment (see Table 4)

R4 DISPLAY CHAPTER - auto increments to Register 5

determines which of the 8 pages is displayed

R5 NORMAL DISPLAY CONTROL - auto increments to Register 6

PON	Picture on
TEXT	Text on
COR	Contrast reduction on
BKGND	Background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R6 NEWSFLASH DISPLAY - auto increments to Register 7

PON	Picture on
TEXT	Text on
COR	Contrast reduction on
BKGND	Background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 DISPLAY MODE - does not auto increment

BOX ON 0	Boxing function allowed on Row 0
BOX ON 1-23	Boxing function allowed on Row 1-23
BOX ON 24	Boxing function allowed on Row 24
DOUBLE HEIGHT	To display double height text
BOTTOM HALF	To select bottom half of page when DOUBLE HEIGHT = 1
REVEAL ON	To reveal concealed text
CURSOR ON	To display cursor
STATUS TOP	Row 25 displayed above or below the main text

R8 ACTIVE CHAPTER - auto increments to Register 9

A0 to A2	Active chapter
CLEAR MEMORY	When set to 1, clears the display memory. This bit is automatically reset
VPS ENABLE	Set to 1 to enable VPS decoding

R9 CURSOR ROW - auto increments to Register 10

R0 to R4	Active row for data written to or read from memory via the I²C-bus

R10 CURSOR COLUMN - auto increments to Register 11 or 11B

C0 to C5	Active column for data written to or read from memory via the I²C-bus

R11 CURSOR DATA - does not auto increment

D0 to D7	Data read from/written to memory via I²C, at location pointed to by R8, R9 and R10. This location automatically increments each time R11 is accessed

R11B DEVICE STATUS - does not auto increment

VCS SIGNAL QUALITY	Indicates that the video signal quality is good and PLL is phase locked to input video when = 1
DATA QUALITY	If good data (either Teletext or VPS) is detected then = 1
ROM VER R0 to R4	Indicated language/ROM variant. See Table 7
$\overline{625}$/525 SYNC	If the input video is a 525 line signal when = 1

Table 3 $\overline{ODD}$/EVEN/$\overline{DV}$ truth table

AUTO $\overline{ODD}$/EVEN	DISABLE $\overline{ODD}$/EVEN	$\overline{ODD}$/EVEN OUTPUT
0	0	$\overline{ODD}$/EVEN output continuously
0	1	$\overline{ODD}$/EVEN statically low
1	0	$\overline{ODD}$/EVEN active only when no TV picture displayed
1	1	Data Valid ($\overline{DV}$) output

Table 4 Register map for page requests (R3)

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{HOLD}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 4

1. Abbreviations are as for Table 1 except for DO CARE bits.
2. When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
3. If $\overline{HOLD}$ is set LOW, the page is held and not updated.
4. Columns auto-increment on successive I²C-bus transmission bytes.
5. 'X' = Don't care.

Table 5 Interlace/non-interlace 312/313 line control (T0 and T1)

T1	T0	RESULT
0	0	interlaced 312.5/312.5 lines
0	1	non-interlaced 312/313 lines (note 1)
1	0	non-interlaced 312/312 lines (note 1)
1	1	SCS mode (scan composite sync)

Note to Table 5

1 Reverts to interlaced mode if a newsflash or subtitle is being displayed.

CLOCK SYSTEMS

Crystal oscillator

The crystal is a conventional 2-pin design operating at 27 MHz. It is capable of oscillating with both fundamental and third overtone mode crystals. External components should be used to suppress the fundamental output of the third overtone as illustrated in Fig.14.

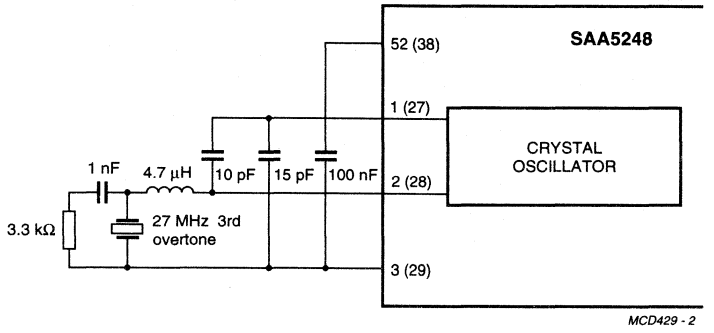


Fig.14 Crystal oscillator application diagram for SOT247; pins in parenthesis are for SOT208.

Table 6 Crystal characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Crystal (27 MHz, 3rd overtone)					
C1	series capacitance	–	1.7	–	pF
C0	parallel capacitance	–	5.2	–	pF
C_L	load capacitance	–	20	–	pF
Rr	resonant resistance	–	–	50	Ω
R1	series resistance	–	20	–	Ω
Xa	ageing	–	–	±5	10^{-6}/yr
Xj	adjustment tolerance	–	–	±25	10^{-6}
Xd	drift	–	–	±25	10^{-6}

Character sets

The WST specification allows the selection of national character sets via the page header transmission bits, C12 to C14. The basic 96 character sets differ only in 13 national option characters as indicated in Table 9 with reference to their table position in the basic character matrix illustrated in Table 8. The SAA5248 automatically decodes transmission bits C12 to C14. Table 7 illustrates the character matrixs.

Character bytes are listed as transmitted from b1 to b7.

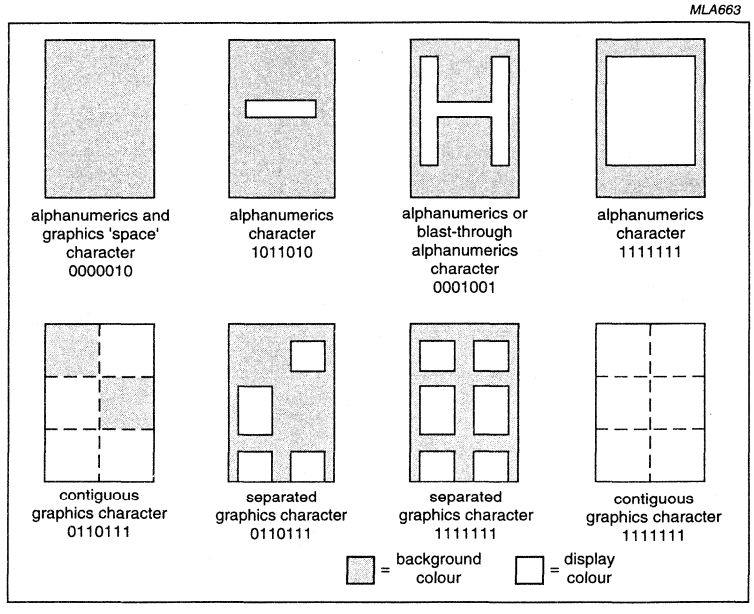


Fig.15 Character format.

Table 7 SAA5248P/E character data input decoding

BITS b_4 b_3 b_2 b_1	row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
	b_8	0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
	b_7	0	0	0	0	0	0	1	1	1		1		0	0	0	0	1	1
	b_6	0	0	1	1	1	1	0	0	1		1		0	0	0	1	0	1
	b_5	0	1	0	1	1	1	0	1	0		1		0	1	0	1	1	1
0 0 0 0	0	alpha - numerics black	graphics black																
0 0 0 1	1	alpha - numerics red	graphics red																
0 0 1 0	2	alpha - numerics green	graphics green																
0 0 1 1	3	alpha - numerics yellow	graphics yellow																
0 1 0 0	4	alpha - numerics blue	graphics blue																
0 1 0 1	5	alpha - numerics magenta	graphics magenta																
0 1 1 0	6	alpha - numerics cyan	graphics cyan																
0 1 1 1	7	alpha - numerics white **	graphics white																
1 0 0 0	8	flash	conceal display																
1 0 0 1	9	steady **	contiguous graphics **																
1 0 1 0	10	end box **	separated graphics																
1 0 1 1	11	start box	ESC *																
1 1 0 0	12	normal height **	black back - ground **																
1 1 0 1	13	double height	new back - ground																
1 1 1 0	14	SO *	hold graphics																
1 1 1 1	15	SI *	release graphics **																

MBA429

For character version number (00000) see Register 11B.

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Notes to Table 7

1. Control characters shown in Columns 0 and 1 are normally displayed as spaces.
2. Characters may be referred to by column and row, For example 2/5 refers to %.
3. Black represents displayed colour. White represents backgound.
4. Character rectangle shown as follows: 
5. The SAA5248 national option characters are illustrated in Table 9.
6. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters for combining with character 8/5.
7. National option characters will be developed according to the setting of control bits C12 to C14. These will be mapped into the basic code table into positions shown in Table 9.
8. Columns 2a, 3a, 6a and 7a are displayed in graphics mode.

Table 8 SAA5248 basic character matrix

Table 9 SAA5248 national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)													
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MEA559

(1) PHCB are the Page Header Control Bits. Other combinations default to English.

INTERFACE FOR DATA ACQUISITION AND CONTROL (for multi-standard teletext systems)

GENERAL DESCRIPTION

The SAA5250 is a CMOS Interface for Data Acquisition and Control (CIDAC) designed for use in conjunction with the Video Input Processor (SAA5230) in a multi-standard teletext decoder. The device retrieves data from a user selected channel (channel demultiplexer), as well as providing control signals and consecutive addressing space necessary to drive a 2 K bytes buffer memory.

The system operates in accordance with the following transmission standards:

- French Didon Antiope specification D2 A4-2 (DIDON)
- North American Broadcast Teletext specification (NABTS)
- U.K. teletext (CEEFAX)

Features

- 7,5 MHz maximum conversion rate
- Three prefixes; DIDON, NABTS and U.K. teletext (CEEFAX)
- Mode without prefix
- Internal calculation of the validation (VAL) and colour burst blanking (CBB) signals, if programmed
- Programmable framing code and channel numbers
- Error parity calculation or not (odd parity)
- Hamming processing of the prefix byte
- Full channel or VBI reception
- Slow/fast mode (detection of page flags or not)
- Maximum/default format up to 63 bytes
- Addressing space of 2 K bytes of the static memory
- Multiplexed address/data information is compatible with Motorola or Intel microcontrollers
- CIDAC is 'MOTEL' compatible

PACKAGE OUTLINES

SAA5250P: 40-lead DIL; plastic (SOT129).
SAA5250T: 40-lead mini-pack; plastic (VSO40; SOT158).

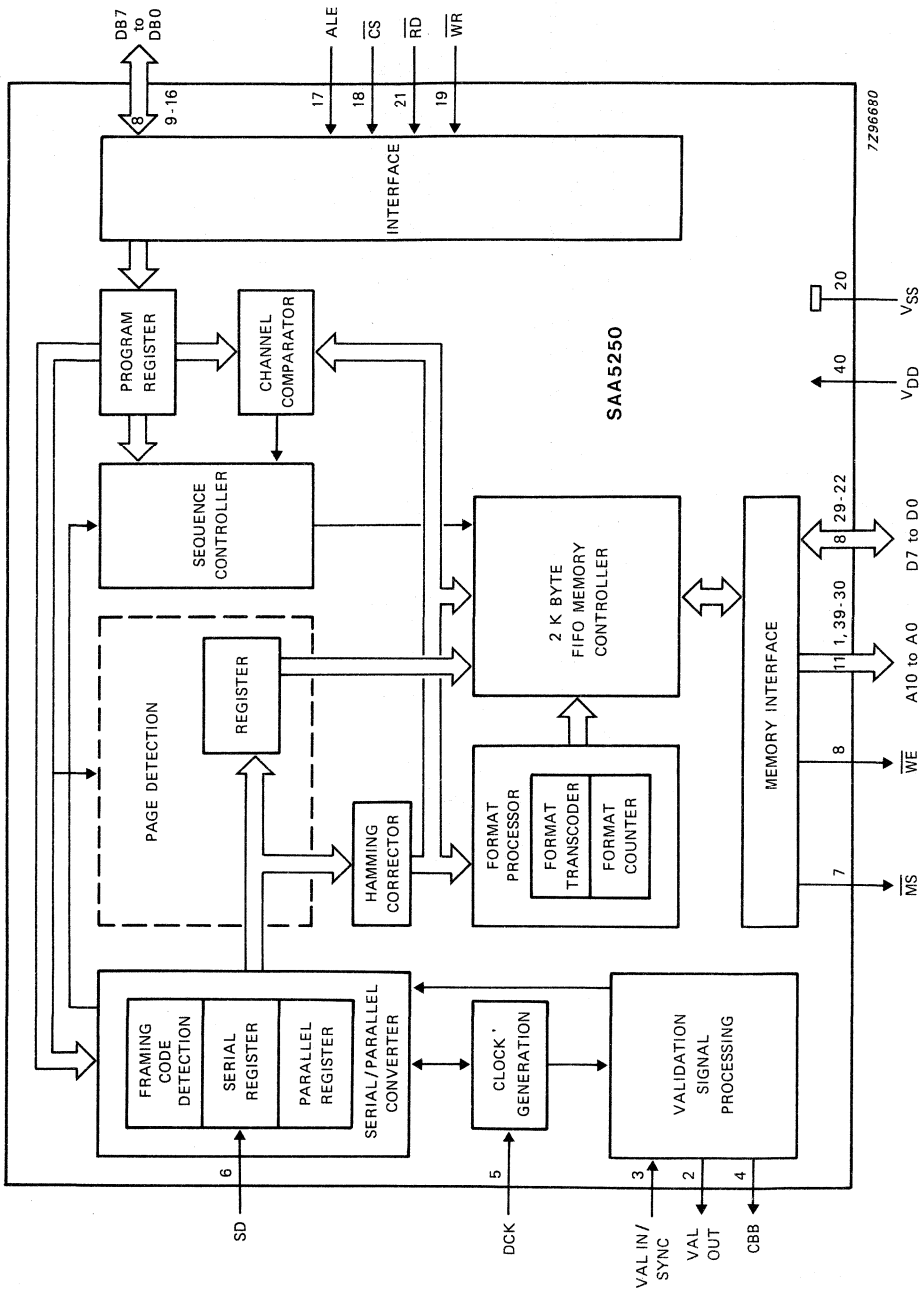


Fig. 1 Block diagram.

DEVELOPMENT DATA

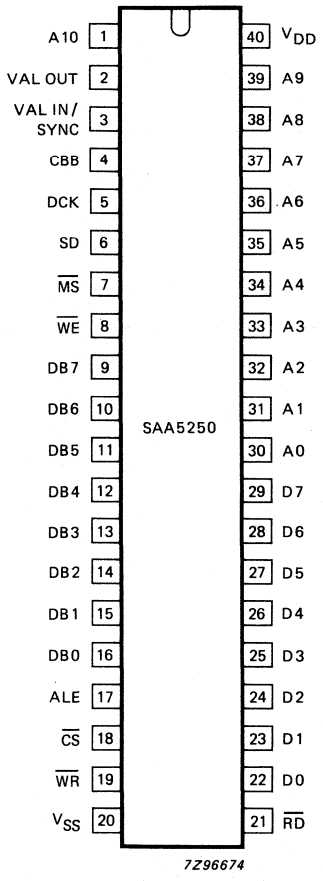


Fig. 2 Pinning diagram.

PINNING FUNCTION

mnemonic	pin no.	function
A10 and A0 to A9	1 and 30 to 39	Memory address outputs used by CIDAC to address a 2 K byte buffer memory
VAL OUT	2	Validation output signal used to control the location of the window for the framing code
VAL IN/SYNC	3	Validation input signal (line signal) used to give or calculate a window for the framing code detection
CBB	4	Colour burst blanking output signal used by the SAA5230 as a data slicer reset pulse
DCK	5	Data clock input, in synchronization with the serial data signal
SD	6	Serial data input, arriving from the demodulator
$\overline{MS}$	7	Chip enable output signal for buffer memory selection
$\overline{WE}$	8	Write command output for the buffer memory
DB7 to DB0	9 to 16	8-bit three state input/output data/address bus used to transfer commands, data and status between the CIDAC registers and the CPU
ALE	17	Demultiplexing input signal for the CPU data bus
$\overline{CE}$	18	Chip enable input for the SAA5250
$\overline{WR}$	19	Write command input (when LOW)
V_{SS}	20	ground
$\overline{RD}$	21	Read command input (when LOW)
D0 to D7	22 to 29	8-bit three state input/output data bus used to transfer data between CIDAC and the buffer memory
V_{DD}	40	+5 V power supply

FUNCTIONAL DESCRIPTION

Microcontroller interface

The microcontroller interface communicates with the CPU via the handshake signals DB7 – DB0, ALE, CS, $\overline{RD}$, $\overline{WR}$. The microcontroller interface produces control commands as well as programming the registers to write their contents or read incoming status/data information from the buffer memory. The details of the codes used to address the registers are given in Table 2.

The CIDAC is 'MOTEL' compatible (MOTEL compatible means it is compatible with standard **Mo**torola or In**tel** microcontrollers). It automatically recognizes the microcontroller type (such as the 6801 or 8501) by using the ALE signal to latch the state of the $\overline{RD}$ input. No external logic is required.

Table 1 Recognition signals

CIDAC	8049/8051 timing 1	6801/6805 timing 2
ALE $\overline{RD}$ $\overline{WR}$	ALE $\overline{RD}$ $\overline{WR}$	AS DS, E, $\Phi 2$ R/$\overline{W}$

Table 2 CIDAC register addressing

codes						
R	W	CS	DB2	DB1	DB0	function
1	0	0	0	0	0	write register R0
1	0	0	0	0	1	write register R1
1	0	0	0	1	0	write register R2
1	0	0	0	1	1	write register R3
1	0	0	1	0	0	write register R4
1	0	0	1	0	1	write register R5
1	0	0	1	1	0	write command register R6 (initialization command)
1	0	0	1	1	1	write register R7
0	1	0	0	0	0	read status
0	1	0	0	0	1	read data register
0	1	0	0	1	0	test (not used)
0	1	0	0	1	1	test (not used)

DEVELOPMENT DATA

Register organization

R0 register

Table 3 R0 Register contents

R04 slow/fast mode	R03 parity	R02 to R00 used prefixes
0 = slow mode 1 = fast mode	0 = no parity control 1 = odd parity	000 = DIDON long 001 = DIDON medium 010 = DIDON short 011 = not used 100 = U.K. teletext 101 = NABTS 110 } without prefix 111 }

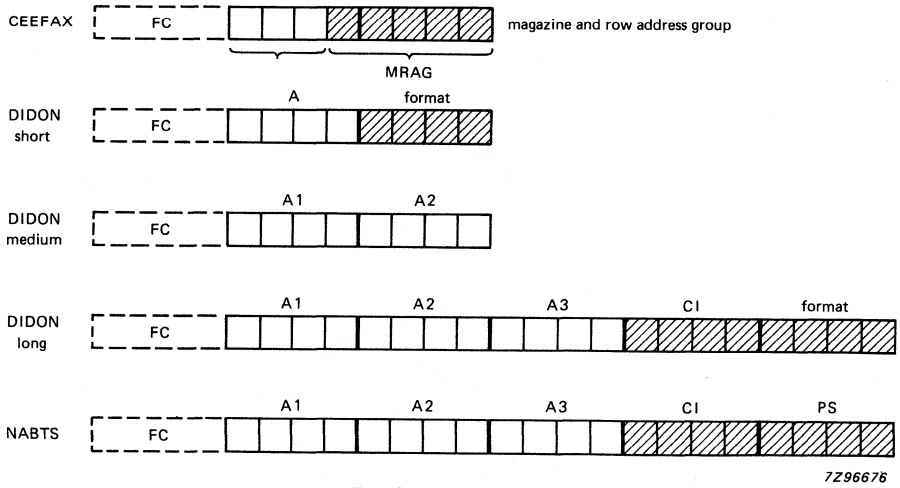


Fig. 3 Five prefixes.

All of the bytes (see Fig. 3) are Hamming protected. The hatched bytes are always stored in the memory in order to be processed by the CPU (see section 'Prefix processing'). In the mode without prefix all of the bytes which follow the framing code are stored in the memory until the end of the data packet, the format is then determined by the contents of the R3 register.

If R03 = 0; no parity control is carried out and the 8-bits of the incoming data bytes are stored in the fifo memory.

If R03 = 1; the 8th bit of the bytes following the prefix (data bytes) represents the result of the odd parity control.

If R04 = 0; the device operates in the slow mode. The CIDAC retrieves data from the user selected magazine (see section 'R1 and R2') and without searching for a start to a page stores the data into the FIFO memory.

If R04 = 1; the device operates in the fast mode. Prior to writing into the FIFO memory, the CIDAC searches for a start to a page which is variable due to the different prefixes:

- DIDON (long, medium and short): using the redundant bytes, SOH RS, X RS and SOH X (where X is a bit affected by a parity error)
- NABTS, the least significant bit of the PS byte is set to 1
- U.K. teletext, ROW = 0

R1 register

Table 4 R1 Register contents

R17 VAL IN/SYNC	R16 to R14 format table	R13 to R10 channel numbers (first digit)
1 = VAL 0 = SYNC	000 = list 1 001 = list 2 010 = list 3 011 = list 4 1XX = maximum/default value used (R3)	first digit hexadecimal value

Note

X = don't care

If VAL IN/SYNC = 1; the line signal immediately produces a validation signal for the framing code detection.

If VAL OUT = 0; the line signal is used as a starting signal for an internally processed validation signal (see Fig. 15). The framing code window width is fixed at 13 clock periods and the delay is determined by the contents of the R5 register (R56 to R50).

At any moment the user is able to ensure that the framing code window is correctly located. This is accomplished by the VAL OUT pin reflecting the internal validation signal. A CBB signal with programmable width (see section 'R7 register') can also be generated, this is used as a data slicer reset pulse by the SAA5230. The line signal is used as the starting point of the internal CBB signal width fixed by the contents of the R7 register.

If R16 = 0; then bits R15 and R14 provide the format table number using DIDON long and short prefixes (see Table 6).

If R16 = 1; then the format is determined by the contents of the R3 register.

The bits R13 to R10 represent the first channel number to be checked in the prefix. In U.K. teletext mode only 3 bits are required, so R13 = X.

Table 5 Format table

format byte B8, B6, B4 and B2	list 1	list 2	list 3	list 4
0000	0	0	0	0
0001	1	1	1	1
0010	2	2	2	2
0011	3	3	3	3
0100	4	5	6	7
0101	8	9	10	11
0110	12	13	14	15
0111	16	17	18	19
1000	20	21	22	23
1001	24	25	26	27
1010	28	29	30	31
1011	32	33	34	35
1100	36	37	38	39
1101	40	41	42	43
1110	44	45	46	47
1111	48	49	50	51

Note

B8 = MSB and B2 = LSB.

R2 register

Table 6 R2 Register contents

R27 to R24	R23 to R20
channel number, third digit	channel number, second digit
(hexadecimal value, third digit)	(hexadecimal value, second digit)

Note

R27 and R23 = MSB and R24 and R20 = LSB

The R2 register provides the other two parts of the channel number (depending on the prefix) that require checking.

R3 register

Table 7 R3 register contents

R35 to R30 6-bit format maximum/default value
000000 = 0 000001 = 1 – – – 111111 = 63

This 6-bit byte gives:

- In the DIDON long and short mode, a maximum format in case of corrupted transmission (multiple errors on the Hamming corrector)
- A possible 63-bit format for all types of prefix

R4 register

Table 8 R4 register contents

R47 to R40
8-bit register used for storing the framing code value which will be compared with the third byte of each data line

R5 register

Table 9 R5 register contents

R57 negative/positive	R56 to R50 synchronization delay
0 = negative edge for sync signal 1 = positive edge for sync signal	7-bit sync delay, giving a maximum delay of $(2^7 - 1) \times 10^6$ μs/F (Hz)

Note

F = data clock acquisition frequency (DCK).

Using R57 it is possible to start the internal synchronization delay (t_{DVAL}) on the positive or negative edge.

R6 write command register

This is a fictitious register. Only the address code (see Table 2) is required to reset the CIDAC. See Table 11 for the status of the FIFO memory on receipt of this command.

R7 register

Table 10 R7 register contents

R75 to R70
6-bit register used to give a maximum colour burst blanking signal of: $(2^6 - 1) \times 10^6\ \mu s/F$ (Hz)

Note

F = data clock acquisition frequency.

Fifo status register (read R0 register)

Table 11 Fifo register contents

DB2 to DB0		
DB2 = 1 memory empty	DB1 = 1, data not present in the read data register	DB0 = 0 memory not full

Once the relevant prefix and the right working modes have been given by the corresponding registers, a write command to the R6 register enables the CIDAC to accept and process serial data.

Channel comparator

This is a four bit comparator which compares the three user hexadecimal defined values in R1 and R2 to the corresponding bytes of the prefix coming from the Hamming corrector. If the three bytes match, the internal process of the prefix continues. If they do not match the CIDAC returns to a wait state until the next broadcast data package is received.

FIFO memory controller

The FIFO memory contains all the necessary functions required for the control of the 11-bit address memory (2 K byte). The functions contained in the FIFO memory are as follows:

- write address register (11-bits)
- read address register (11-bits)
- memory pointer (11-bits)
- address multiplexer (11-bits)
- write data register (8-bits)
- read data register (8-bits)
- data multiplexer
- control logic

The FIFO memory provides the memory interface with the following:

- 11-bit address bus (A10 to A0)
- 8-bit data bus (D7 to D0)
- two control signals, memory select ($\overline{MS}$) and write enable ($\overline{WE}$)

Operation

The CIDAC uses the same clock signal for data acquisition and internal processing, this allows the CIDAC to have a write and a read cycle during each character period (see Fig. 13). The first half of the character period is a write cycle and the second half is a read cycle. Consequently, for an 8 MHz bit rate the maximum memory cycle time is 500 ns.

When the first data byte is written into the FIFO memory, thus transferred into the read register, the FIFO memory enters the status shown in Table 12.

Table 12 FIFO status

DB2 to DB0		
DB2 = 1 memory empty	DB1 = 0 data available	DB0 = 0 memory not full

When the FIFO memory is full two events occur:

- the write address register points to the next address after the last written address
- when new data is to be written, the memory select signal output ceases

Memory interface

The memory interface contains all the buffers for the memory signals mentioned in the section 'FIFO memory controller'.

Page detection

This part of the CIDAC contains a parallel register with logic which detects (only in fast mode) a start of a page or data group (see section 'R0 register').

Hamming correction (see Tables 13 and 14)

The Hamming correction provides (see section 'Prefix processing'):

- hexadecimal value of the Hamming code
- accept/reject code signal
- parity information

Table 13 Hamming correction (coding)

Hexadecimal notation	B8	B7	B6	B5	B4	B3	B2	B1
0	0	0	0	1	0	1	0	1
1	0	0	0	0	0	0	1	0
2	0	1	0	0	1	0	0	1
3	0	1	0	1	1	1	1	0
4	0	1	1	0	0	1	0	0
5	0	1	1	1	0	0	1	1
6	0	0	1	1	1	0	0	0
7	0	0	1	0	1	1	1	1
8	1	1	0	1	0	0	0	0
9	1	1	0	0	0	1	1	1
A	1	0	0	0	1	1	0	0
B	1	0	0	1	1	0	1	1
C	1	0	1	0	0	0	0	1
D	1	0	1	1	0	1	1	0
E	1	1	1	1	1	1	0	1
F	1	1	1	0	1	0	1	0

Note

$B7 = B8 \oplus B6 \oplus \overline{B4}$
$B5 = B6 \oplus \overline{B4} \oplus \overline{B2}$
$B3 = \overline{B4} \oplus \overline{B2} \oplus B8$
$B1 = \overline{B2} \oplus B8 \oplus B6$

$\oplus$ = exclusive OR gate function
B8, B6, B4 and B2 = data bits
B7, B5, B3 and B1 = redundancy bits

Table 14 Hamming correction (decoding)

A	B	C	D	interpretation	information
1	1	1	1	no error	accepted
0	0	1	0	error on B8	corrected
1	1	1	0	error on B7	accepted
0	1	0	0	error on B6	corrected
1	1	0	0	error on B5	accepted
1	0	0	0	error on B4	corrected
1	0	1	0	error on B3	accepted
0	0	0	0	error on B2	corrected
0	1	1	0	error on B1	accepted
A.B.C = 0			1	multiple errors	rejected

Note

$A = B8 \oplus B6 \oplus B2 \oplus B1$
$B = B8 \oplus B4 \oplus B3 \oplus B2$
$C = B6 \oplus B5 \oplus B4 \oplus B2$
$D = B8 \oplus B7 \oplus B6 \oplus B5 \oplus B4 \oplus B3 \oplus B2 \oplus B1$

$\oplus$ = exclusive OR gate function

Format processing

The format processing consists of two parts:

part 1

A format transcoder produces a 6-bit code (up to 63) and uses the following as inputs:

- DIDON long and short prefixes;
  hamming corrected code (4-bits)
  accept/reject code condition
  table number (see section 'R1 register', bits R15 and R14)
- Other prefixes (R16 = 1)
- 6-bit maximum/default format (see section 'R3 register')

part 2

A format counter operating at the character clock frequency which receives the 6-bit code from the format transcoder and is used to check the data packet length following the prefix.

Serial/parallel converter

The serial/parallel converter consists of three parts:

- An 8-bit shift register which receives the SD input and operates at the bit frequency (DCK).
- An 8-bit parallel register used for storage.
- A framing code detection circuit. This logic circuit compares the 8-bits of the R4 register with that of the serial register. If seven bits out of eight match (in coincidence with a validation window), it produces a start signal for a new teletext data line to the sequence controller.

Clock generation

The clock generator does the following:

- acts as a buffer for the DCK clock
- generates the character clock

As soon as a framing code has been detected, a divide by 8 counter is initialized and the character clock is started. The clock drives the following:

- sequence controller
- parallel registers
- format counter

Processing of VAL and CBB signals

The circuit has one input (VAL IN/SYNC) and two outputs (VAL OUT and CBB). The circuit consists of:

- 7-bit counter operating at DCK frequency which produces the framing code validation pulse delay
- 7-bit comparator which compares the contents of the R5 register (bits R56 to R50) to the bit counter
- a 6-bit counter operating at DCK frequency which produces the CBB pulse width
- 6-bit comparator which compares the contents of the R7 register (bits R75 to R70) to the bit counter
- control logic required to provide the start condition for the VAL signal and the CBB pulse width (on the negative or positive edge of the sync signal)

The CBB signal usefulness occurs when the associated video processor:

- has no sandcastle pulse to send back to the demodulator
- carries out the synchronization of the time base clock. In this event the CBB acts as a data slicer reset pulse

The VAL OUT is a control signal which reflects the internal framing code window.

Prefix processing (see Table 21)

Figs 4 to 9 show the acquisition flow charts for each prefix type coded in the R0 register (bits R02 to R00).

As soon as an initialization command is received by the CIDAC, a write command to the R6 register (only the address is significant), is ready to receive data from a dedicated channel number and store the data in the FIFO memory (explained in the following paragraphs, each paragraph being dedicated to an individual type of prefix).

DIDON long (see Fig. 4)

In this mode, the continuity index, format and data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a page detection.)

Table 15 Continuity index processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	X	X	CI3	CI2	CI1	CI0

Table 16 Format processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	F5	F4	F3	F2	F1	F0

Note

A/R = 0, if rejected
A/R = 1, if accepted
X = don't care

DIDON mediun (see Fig. 5)

Only data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a page detection.)

DIDON short (see Fig. 6)

In this mode, format and data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a page detection.)

Table 17 Format processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	F5	F4	F3	F2	F1	F0

NABTS (see Fig. 7)

In this mode, the continuity index, packet structure and data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a page detection.)

Table 18 Continuity index processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	X	X	CI3	CI2	CI1	CI0

Table 19 Packet structure processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	X	X	PS3	PS2	PS1	PS0

U.K. teletext (see Fig. 8)

In this mode, the magazine and row address group (two bytes) and data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a flag detection.)

Table 20 Magazine and row address group processing results

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	X	RW4	RW3	RW2	RW1	RW0

Without prefix

All the data following the framing code are stored in the FIFO memory.

Table 21 Prefix processing

prefixes	construction of prefixes	bytes stored in FIFO memory during slow mode	bytes stored in FIFO memory during fast mode
DIDON long	A1, A2, A3, CI, F and D	CI, F and D	CI*, F* and D*
DIDON medium	A1, A2 and D	D	D*
DIDON short	A1, F and D	F and D	F* and D*
NABTS	A1, A2, A3 CI, PS and D	CI, PS and D	CI*, PS* and D*
U.K. teletext	MRAG and D	MRAG and D	MRAG* and D*
without prefix		all bytes of the data packet following the framing code are written into the FIFO memory	

Note

* = after page/flag detection
A1, A2, A3 are channel numbers
CI = continuity index
F = format
PS = packet structure
D = data
MRAG = magazine and row address group

DEVELOPMENT DATA

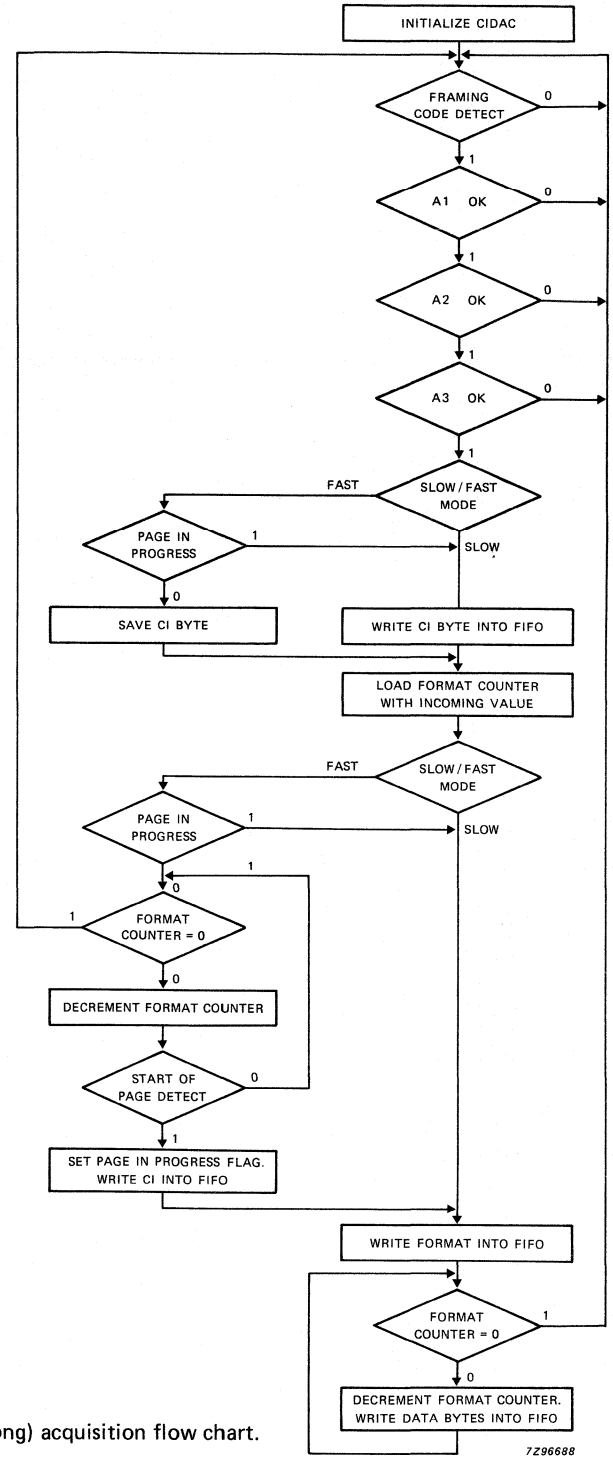


Fig. 4 DIDON (long) acquisition flow chart.

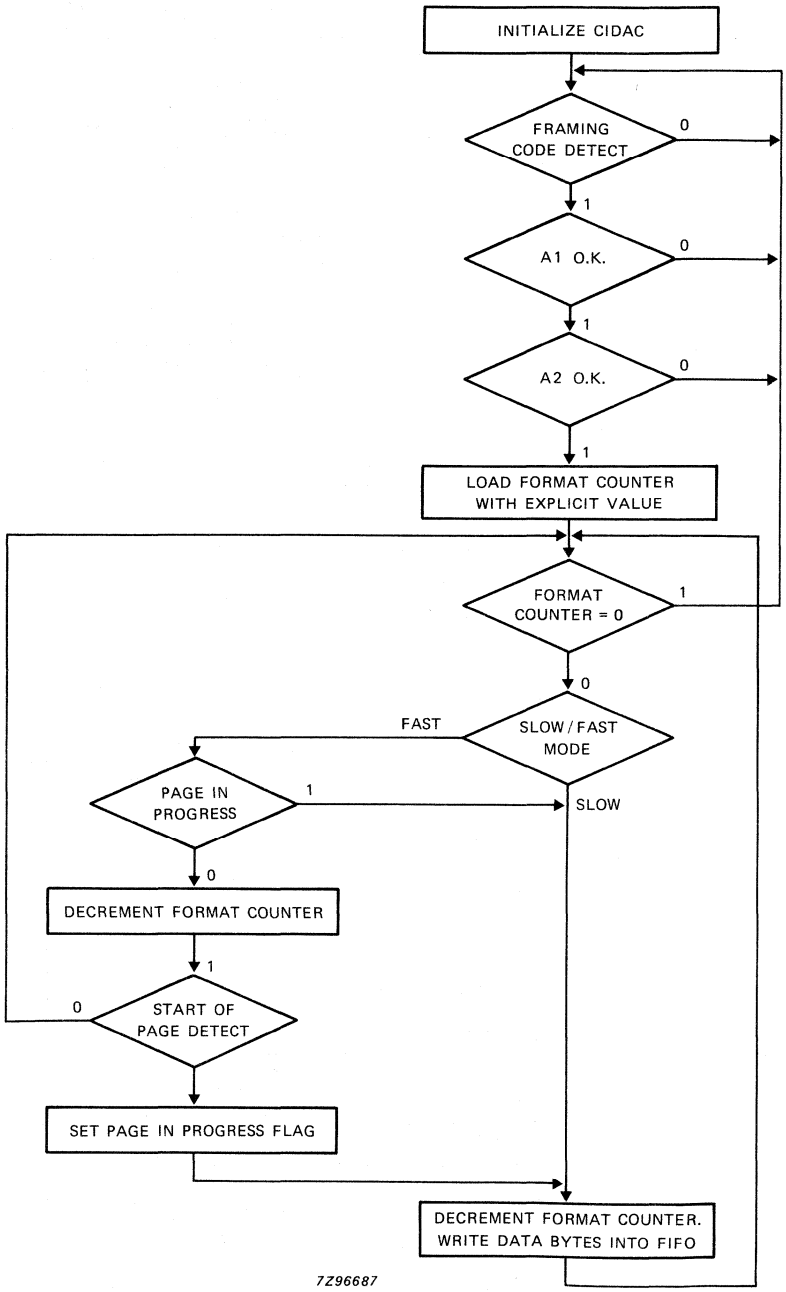


Fig. 5 DIDON (medium) acquisition flow chart.

DEVELOPMENT DATA

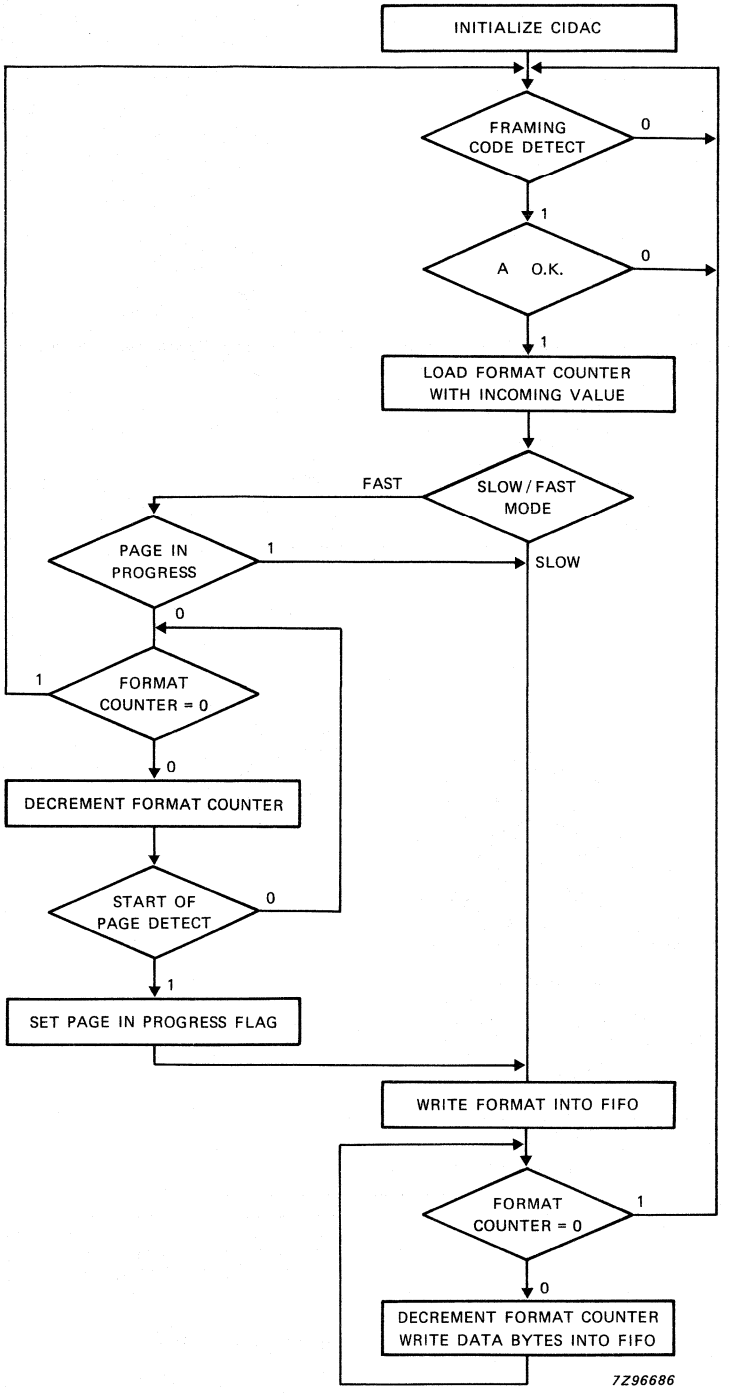


Fig. 6 DIDON (short) acquisition flow chart.

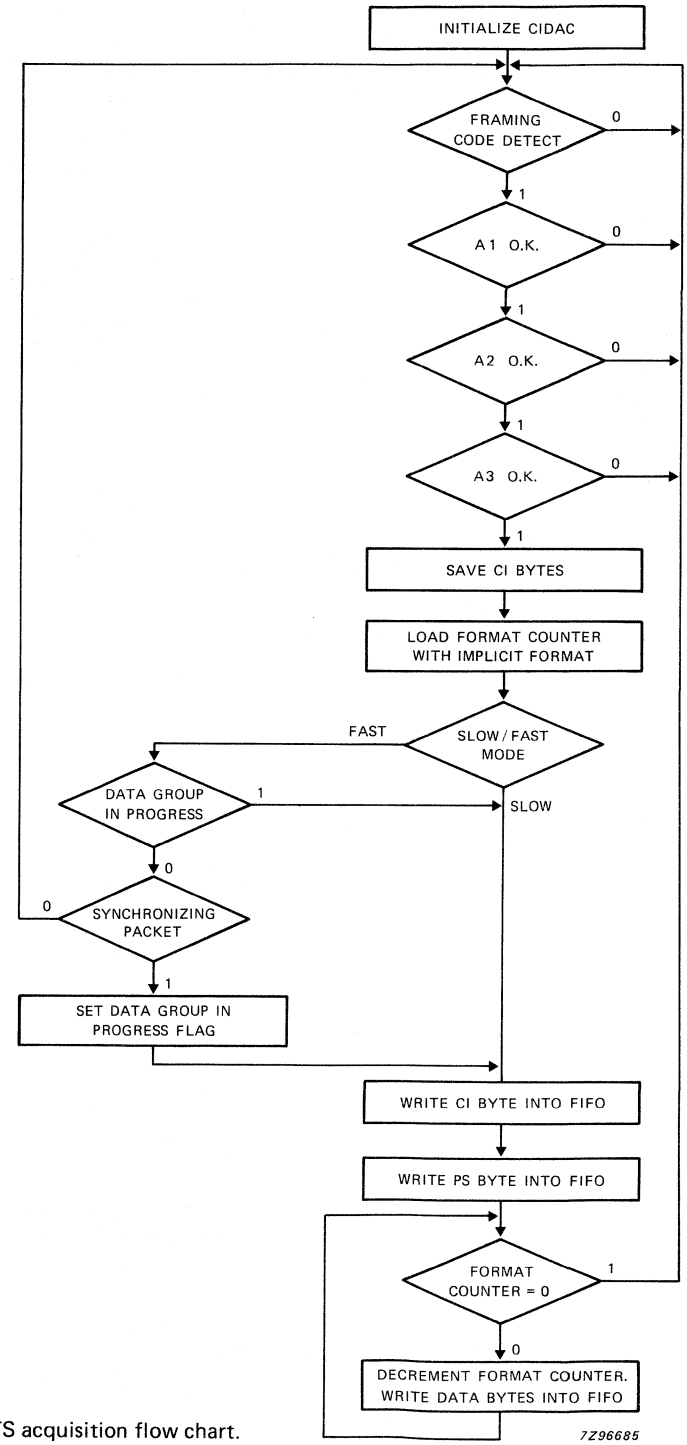


Fig. 7 NABTS acquisition flow chart.

DEVELOPMENT DATA

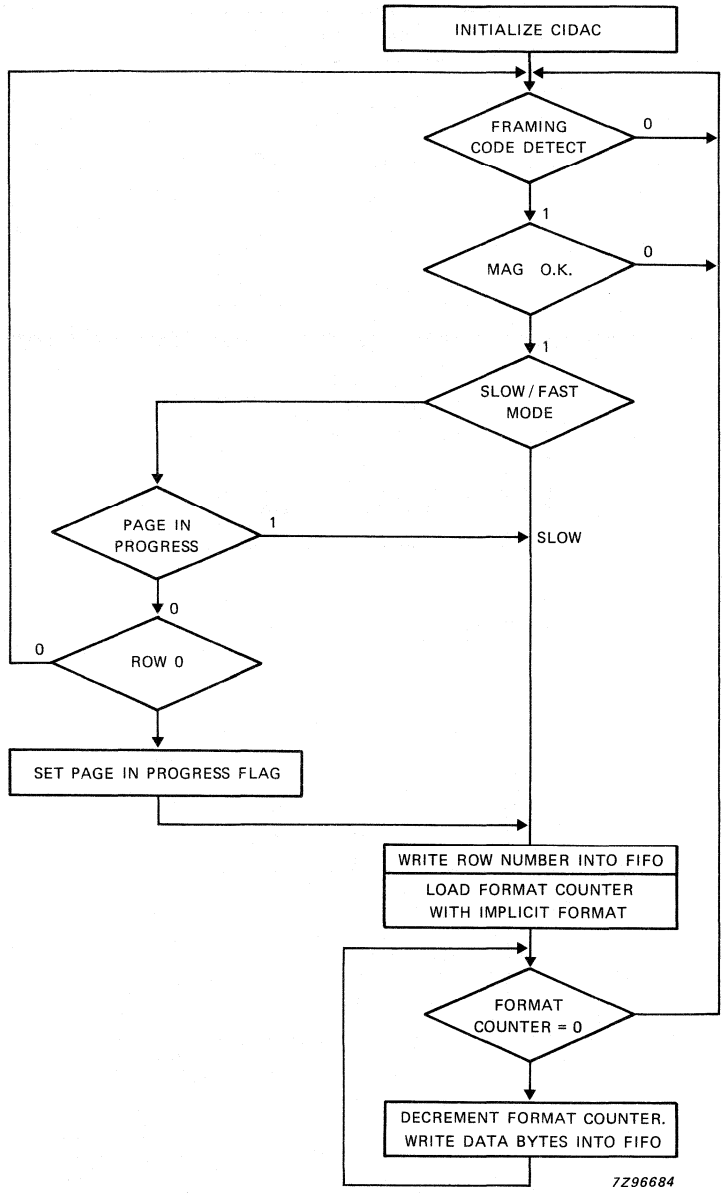


Fig. 8 U.K. teletext acquisition flow chart.

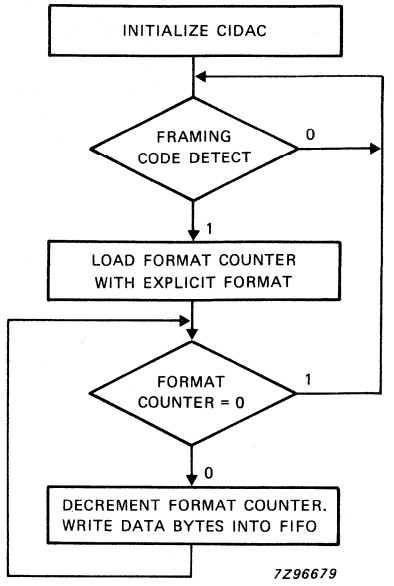


Fig. 9 Without prefix acquisition chart.

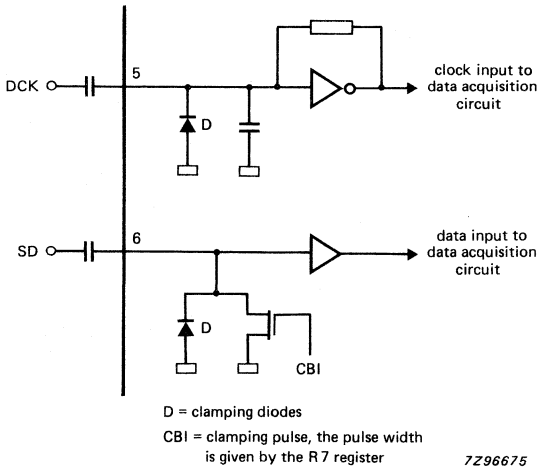


Fig. 10 SD and DCK input circuitry.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0,3	6,5	V
Input voltage range		V_I	−0,3	V_{DD}+0,3	V
Total power dissipation		P_{tot}	−	400	mW
Operating ambient temperature range		T_{amb}	0	70	°C
Storage temperature range		T_{stg}	−20	+125	°C

D.C. CHARACTERISTICS (except SD and DCK)

V_{DD} = 5 V ±10%; V_{SS} = 0 V; T_{amb} = 0 to 70 °C, unless otherwise specified

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_{DD}	4,5	5,0	5,5	V
Input voltage HIGH		V_{IH}	2	−	V_{DD}	V
Input voltage LOW		V_{IL}	−	−	0,8	V
Input leakage current		I_I	−	−	1,0	μA
Output voltage HIGH	I_{load} = 1 mA	V_{OH}	V_{DD}−0,4	−	−	V
Output voltage LOW	I_{load} = 4 mA, at pins 9 to 16 and 22 to 29	V_{OL}	−	−	0,4	V
	I_{load} = 1 mA all other outputs	V_{OL}	−	−	0,4	V
Power dissipation		P	−	5	−	mW
Input capacitance		C_I	−	−	7,5	pF

SD and DCK D.C. CHARACTERISTICS (see Fig. 10)

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 0 to 70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
DCK						
Input voltage range (peak-to-peak value)		$V_{I(p-p)}$	2,0	–	–	V
Input current	V_I = 0 to V_{DD}	I_I	5	–	200	μA
Input capacitance		C_I	–	–	30	pF
External coupling capacitor		C_{ext}	10	–	–	nF
SD						
D.C. input voltage range HIGH	note 1	V_{IH}	2,0	–	–	V
D.C. input voltage range LOW	note 2	V_{IL}	–	–	0,8	V
A.C. input voltage (peak-to-peak value)		$V_{I(p-p)}$	2,0	–	–	V
Input leakage current	V_I = 0 to V_{DD}	I_I	–	–	10	μA
Input capacitance		C_I	–	–	30	pF
External coupling capacitor		C_{ext}	10	–	–	nF

A.C. CHARACTERISTICS

V_{DD} = 5 V ±10%; Reference levels for all inputs and outputs, V_{IH} = 2 V; V_{IL} = 0,8 V; V_{OH} = 2,4 V; V_{OL} = 0,4 V; C_L = 50 pF on DB7 to DB0; T_{amb} = 0 to 70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Microcontroller interface	Figs 11 and 12					
Cycle time		t_{CY}	400	–	–	ns
Address pulse width		t_{LHLL}	50	–	–	ns
$\overline{RD}$ HIGH or $\overline{WR}$ to ALE HIGH	Fig. 11	t_{AHRD}	0	–	–	ns
DS LOW to AS HIGH	Fig. 12	t_{AHRD}	0	–	–	ns
ALE LOW to $\overline{RD}$ LOW or $\overline{WR}$ LOW	Fig. 11	t_{ALRD}	30	–	–	ns
AS LOW to DS HIGH	Fig. 12	t_{ALRD}	30	–	–	ns
Write pulse width		t_{WL}	120	–	–	ns
Address and chip select set-up time		t_{ASL}	10	–	–	ns
Address and chip select hold time		t_{AHL}	20	–	–	ns
Read to data out period		t_{RD}	–	–	130	ns
Data hold after $\overline{RD}$		t_{DR}	10	–	100	ns
R/$\overline{W}$ to DS set-up time	Fig. 12	t_{RWS}	40	–	–	ns
R/$\overline{W}$ to DS hold time	Fig. 12	t_{RWH}	10	–	–	ns
Data set-up time	write cycle	t_{DW}	50	–	–	ns
Data hold time	write cycle	t_{WD}	10	–	–	ns
Read pulse width	note 3	t_{RL}	150 or DCK + 50	–	–	ns

DEVELOPMENT DATA

A.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Memory interface	Fig. 13					
$\overline{WE}$ LOW to DCK falling edge		t_{WEL}	10	–	80	ns
$\overline{WE}$ HIGH to DCK falling edge		t_{WEH}	10	–	80	ns
$\overline{MS}$ LOW to DCK rising edge		t_{MSL}	10	–	80	ns
$\overline{MS}$ HIGH to DCK rising edge		t_{MSH}	10	–	85	ns
Address output from DCK rising edge		t_{AV}	10	–	120	ns
Data output from $\overline{WE}$ falling edge		t_{DWL}	0	–	10	ns
Data hold from $\overline{WE}$ rising edge		t_{DWH}	0	–	–	ns
Address set-up time to data	note 4	t_{AD}	–	–	3 x DCK – 110	ns
$\overline{WE}$ pulse width	note 5	t_{WEW}	3 x DCK	–	–	ns
$\overline{MS}$ pulse width	note 6	t_{MSW}	2 x DCK	–	–	ns
Demodulator interface (see SD and DCK D.C. CHARACTERISTICS)	Fig. 14					
DCK LOW	conversion rate < 7,5 MHz	t_{DCKL}	55	–	–	ns
DCK HIGH	conversion rate < 7,5 MHz	t_{DCKH}	55	–	–	ns
Serial data set-up time		t_{SSD}	0	–	–	ns
Serial data hold time		t_{HSD}	30	–	–	ns
Validation signal set-up time		t_{SVALI}	50	–	–	ns
Validation signal hold time		t_{HVALI}	50	–	–	ns
Other I/O signals	Fig. 15					
User definable width as a multiple of DCK period		t_{WCBB}	0	–	63	DCK
Validation signal width	note 7	t_{WVAL}	X	12	X	DCK
User definable delay as a multiple of DCK period		t_{DVAL}	0	–	127	DCK

Notes to the characteristics

1. Unless R7 = 00 the value given is unacceptable.
2. When CBI signal is maintained at 0 V (R7 = 00) and if SD input signal is correctly referenced to ground, no coupling capacitor is required.
3. DCK + 50 is the DCK period plus 50 ns.
4. 3 x DCK − 110 is 3 x DCK period − 110 ns.
5. 3 x DCK is 3 x DCK period.
6. 2 x DCK is 2 x DCK period.
7. X = irrelevant.

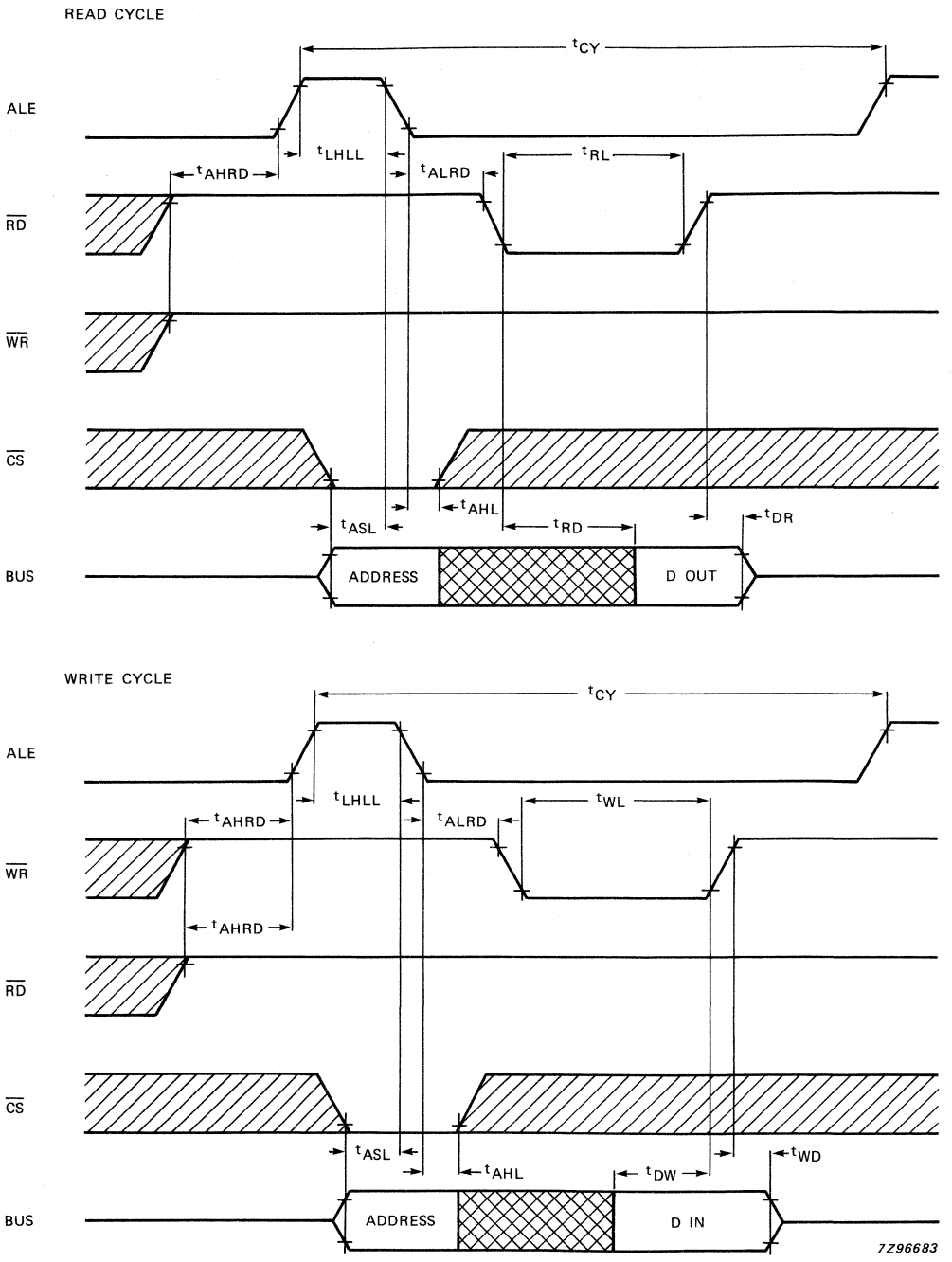


Fig. 11 Timing diagram for microcontroller interface (Intel).

DEVELOPMENT DATA

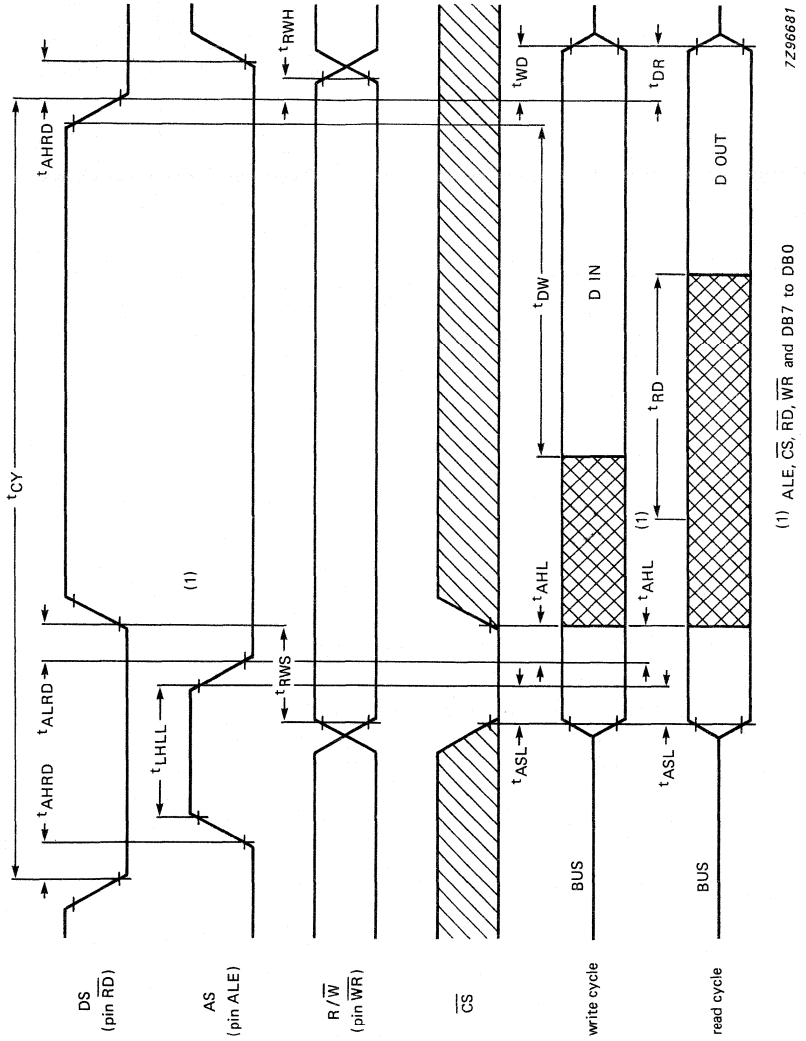


Fig. 12 Timing diagram for microcontroller interface (Motorola).

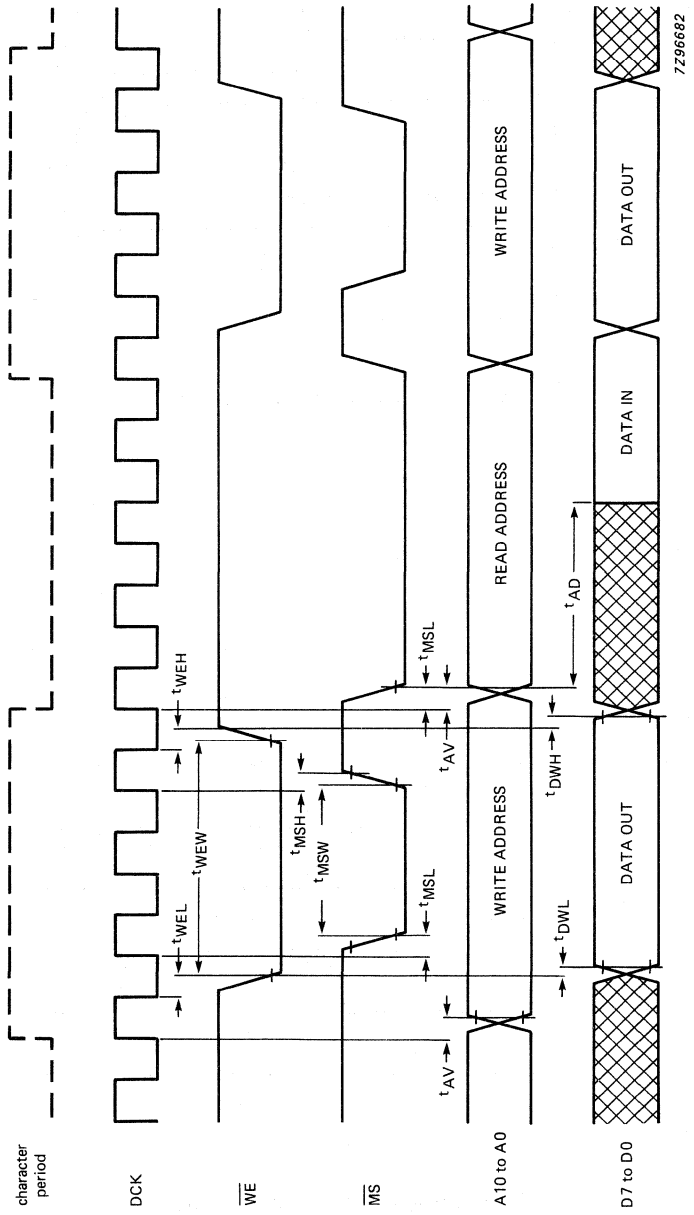


Fig. 13 Timing diagram for memory interface.

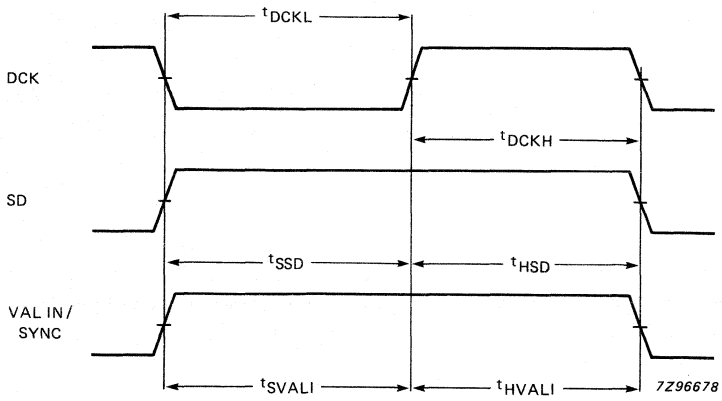


Fig. 14 Timing diagram for demodulator interface.

DEVELOPMENT DATA

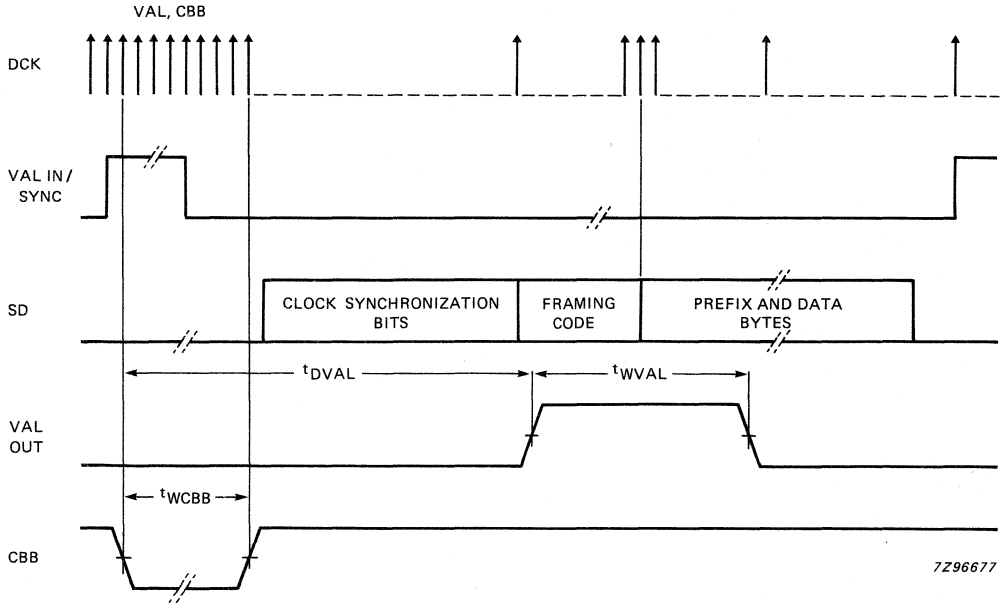


Fig. 15 Timing diagram for all other I/O signals.

Line twenty-one acquisition and display (LITOD)

SAA5252

FEATURES

- Complete stand-alone Line 21 decoder in one package
- On-chip display RAM allowing full page Text mode
- Enhanced character display modes
- Full colour captions
- RGB interface for standard colour decoder ICs
- Automatic handling of Field 2 data
- Automatic selection of (1H, 1V), (2H, 1V) or (2H, 2V) scan modes
- Onboard OSD facility using Character generator
- RGB inputs to support existing OSD ICs
- I²C bus or "stand alone" pin control
- Automatic data-ready signal generation on data acquisition
- Can decode signals recorded on standard VHS and S-VHS tape

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	30	–	mA
V_{syn}	CVBS sync amplitude	0.1	0.3	0.6	V
V_{vid}	CVBS video amplitude	0.7	1.0	1.4	V
T_{amb}	operating ambient temperature range	–20	–	+70	°C
T_{stg}	storage temperature range	–55	–	+125	°C

GENERAL DESCRIPTION

The SAA5252 (LITOD) is a single-chip CMOS device, which will acquire, decode and display Line 21 Closed Captioning data from a 525 line composite video signal. Operation as an On-Screen Display (OSD) device is also possible. Normal and line progressive scan modes are supported.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5252P	24	DIL	plastic	SOT101

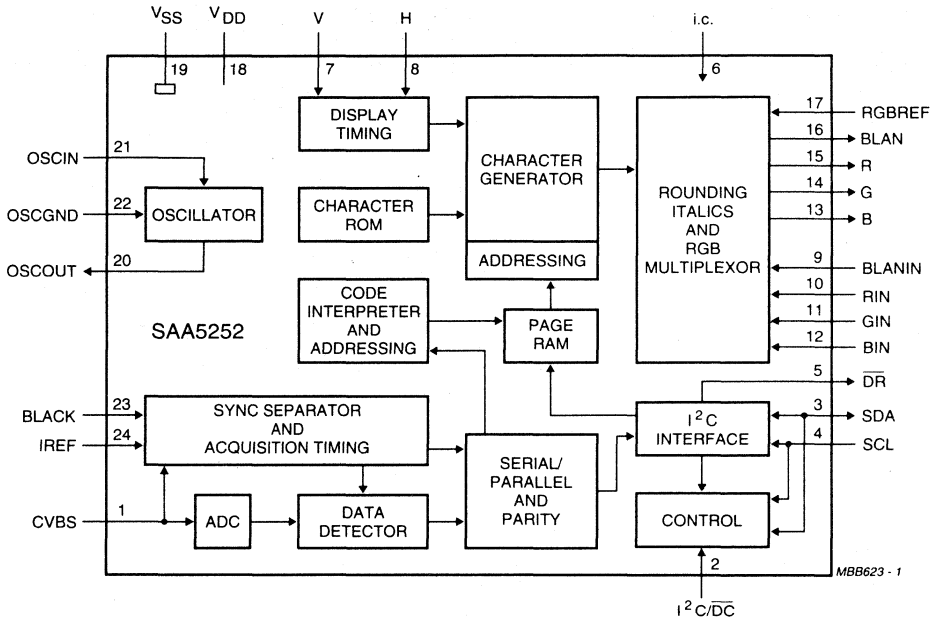


Fig.1 Block diagram.

Line twenty-one acquisition and display (LITOD) SAA5252

PINNING

SYMBOL	PIN	DESCRIPTION
CVBS	1	composite video input; signal should be connected via 100 nF capacitor
$I^2C/\overline{DC}$	2	selects I^2C or Direct Control
SDA	3	serial data port for I^2C-bus or mode select input for direct control
SCL	4	serial clock input for I^2C-bus or mode select input for direct control
$\overline{DR}$	5	data-ready signal to microcontroller (active-LOW) or mode select input for direct control
i.c.	6	internally connected; connect to V_{SS} for normal operation
V	7	field reference for display timing
H	8	line reference for display timing
BLANIN	9	video blanking input from external OSD device
RIN	10	RED video input from external OSD device
GIN	11	GREEN video input from external OSD device
BIN	12	BLUE video input from external OSD device
B	13	BLUE video output
G	14	GREEN video output
R	15	RED video output
BLAN	16	video blanking output
RGBREF	17	voltage defining output HIGH level for RGB pins for closed captioning output
V_{DD}	18	+5 V supply
V_{SS}	19	0 V ground
OSCOUT	20	oscillator output
OSCIN	21	oscillator input
OSCGND	22	oscillator ground
BLACK	23	video black level storage; connected to V_{SS} via 100 nF capacitor
IREF	24	reference current input; connected to V_{SS} via 27 kΩ resistor

PIN CONFIGURATION

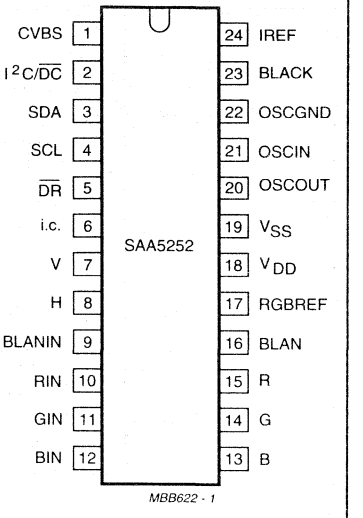


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)		−0.3	+6.5	V
V_I	maximum input voltage (any input)	note 1	−0.3	V_{DD} +0.5	V
V_O	maximum output voltage (any output)	note 1	−	V_{DD} +0.5	V
V_{dif}	difference between V_{SS} and OSCGND		−	±0.25	V
I_{IOK}	DC input or output diode current		−	±20	mA
I_O	maximum output current (each output)		−	±10	mA
T_{amb}	operating ambient temperature range		−20	+70	°C
T_{stg}	storage temperature range		−55	+125	°C
	electrostatic handling				
$V_{stat(HBM)}$	Human body model	note 2	−2000	+2000	V
$V_{stat(MM)}$	machine model	note 3	−200	+200	V

Notes to the limiting values

1. This maximum value has an absolute maximum of 6.5 V independent of V_{DD}.
2. The Human body model ESD simulation is equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor, which produces single discharge transient. Reference Philips Semiconductors Test Method UZW-BO/FQ-A302 (similar to MIL-STD 883C method 3015.7).
3. The Man machine ESD simulation is equivalent to discharging a 200 pF capacitor via a resistor and series inductor with effective dynamic values of 25 Ω and 2.5 μH, which produces a damped oscillating discharge. Reference Philips Semiconductors Test Method UZW-BO/FQ-B302 (similar to EIAJ IC-121 Test Method 20 condition C).

Quality

This device will meet the requirements of the Philips Semiconductors General Quality Specification UZW-BO/FQ-0601. This details the acceptance criteria for all Q & R tests applied to the product.

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −20 to +70 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	positive supply voltage		4.5	5.0	5.5	V
I_{DD}	total supply current		–	30	–	mA
Inputs						
CVBS						
V_{syn}	sync amplitude		0.1	0.3	0.6	V
V_{vid}	video input amplitude (peak-to-peak value)		0.7	1.0	1.4	V
V_{idat}	caption data amplitude		0.25	0.35	0.49	V
Z_{src}	source impedance		–	–	250	Ω
V_I	input switching level of sync separator		1.7	2.0	2.3	V
Z_I	input impedance		2.5	5	–	kΩ
C_I	input capacitance		–	–	10	pF
IREF						
R_{24}	resistor to ground		–	27	–	kΩ
V_{24}	voltage on pin 24		–	$V_{DD}/2$	–	V
H						
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
I_I	maximum input current		−1	–	+1	mA
C_I	input capacitance		–	–	10	pF
t_r	pulse rise time		–	–	5	µs
t_f	pulse fall time		–	–	5	µs
t_W	pulse width					
	1H		–	12	–	µs
	2H		–	6	–	µs
V						
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
I_I	maximum input current		−1	–	+1	mA
t_r	pulse rise time		–	–	5	ns
t_f	pulse fall time		–	–	5	ns
t_W	pulse width		1	–	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGBREF						
V_I	input voltage		−0.3	–	V_{DD}	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
RGB Inputs						
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
Z_I	input impedance		2.5	5	–	kΩ
BLANIN						
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
t_r	input rise time	between 10% and 90%	–	–	80	ns
t_f	input fall time	between 90% and 10%	–	–	80	ns
I²C/$\overline{DC}$						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
SCL						
V_{IL}	LOW level input voltage		−0.3	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
f_{CLK}	clock frequency		0	–	100	kHz
t_r	input rise time	between 10% and 90%	–	–	2	µs
t_f	input fall time	between 90% and 10%	–	–	2	µs
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
Inputs/Outputs						
Ceramic resonator (see Fig.5)						
f_{OSC}	oscillation frequency		11.32	12	12.18	MHz
C0	parallel capacitance		–	5.35	–	pF
C1	series capacitance		–	37.4	–	pF
L1	series inductance		–	35.5	–	µH
R1	series resistance		–	6	25	Ω
BLACK						
C_{blk}	storage capacitance to ground		–	100	–	nF
V_{blk}	black level voltage for nominal sync amplitude		1.8	2.15	2.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SDA (open drain)						
V_{IL}	LOW levelinput voltage		−0.3	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
t_r	input rise time	between 10% and 90%	–	–	2	µs
t_f	input fall time	between 90% and 10%	–	–	2	µs
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.5	V
t_f	output fall time	between 3 V and 1 V	–	–	200	ns
C_L	load capacitance		–	–	400	pF
$\overline{DR}$ (open drain)						
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
t_f	output fall time	measured between 4.0 V and 1.0 V with 3.3 kΩ to 5 V	–	–	50	ns
C_L	load capacitance		–	–	100	pF
Outputs						
R, G, B (caption mode)						
V_{OL}	LOW level output voltage	I_{OL} = +2 mA	0	–	0.2	V
V_{OH}	HIGH level output voltage	I_{OH} = −2 mA	RGBREF −0.3	RGBREF	RGBREF +0.4	V
Z_O	output impedance		–	–	200	Ω
C_L	load capacitance		–	–	50	pF
t_r	output rise time	between 10% and 90%	–	–	10	ns
t_f	output fall time	between 90% and 10%	–	–	10	ns
BLAN						
V_{OL}	LOW lecvel output voltage	I_{OL} = +0.2 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	1.1	–	2.8	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	between 10% and 90%	–	–	10	ns
t_f	output fall time	between 90% and 10%	–	–	10	ns
T_{sk}	skew delay between display and R, G, B, BLAN		–	–	10	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C Timings (see Fig.3)						
t_{LOW}	clock LOW period		4	–	–	µs
t_{HIGH}	clock HIGH period		4	–	–	µs
$t_{SU;\ DAT}$	data set-up time		250	–	–	ns
$t_{HD;\ DAT}$	data hold time		170	–	–	ns
$t_{SU;\ STO}$	set-up time from clock HIGH to STOP		4	–	–	µs
t_{BUF}	START set-up time following a STOP		4	–	–	µs
$t_{HD;\ STA}$	START hold time		4	–	–	µs
$t_{SU;\ STA}$	START set-up time following clock LOW-to-HIGH transition		4	–	–	µs
t_r	output rise time	between 10% and 90%	–	–	10	ns
t_f	output fall time	between 90% and 10%	–	–	10	ns

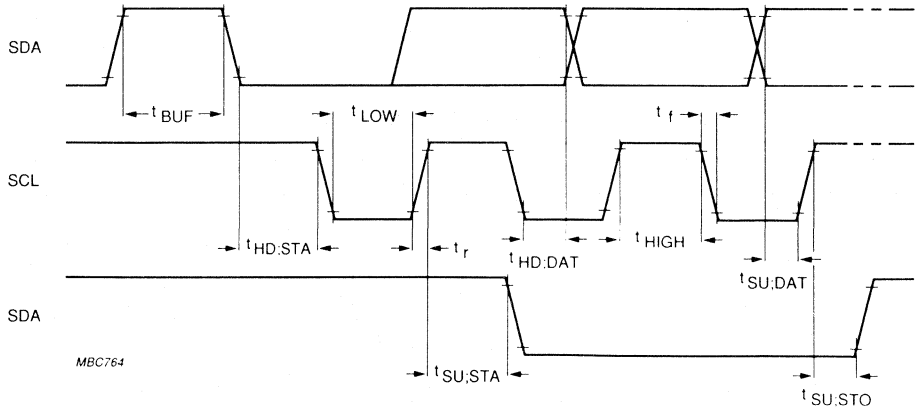
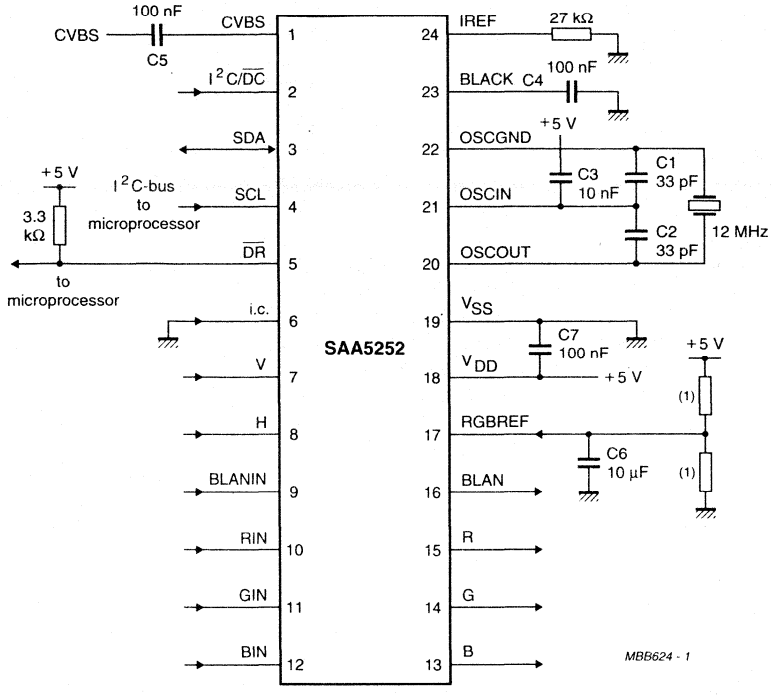


Fig.3 I²C timing diagram.

APPLICATION INFORMATION



(1) Value dependent on application

Fig.4 Application diagram.

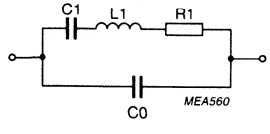


Fig.5 Ceramic resonator equivalent circuit.

DISPLAY GENERATOR

General Description

The displayed characters are defined on a 5 by 12 matrix within a 7 by 13 window, allowing one blank pixel either side of the character and a blank pixel row above. There are a number of display options available controlled by Register 1, or external pins in stand-alone mode.
The three display modes are video, text and caption, the device is powered up in the video mode.
The display generator reads the Pre-amble Address Code (PAC) then the data associated with that row. Each character is then rounded after which it can be italicised and/or underlined, depending on the PAC or mid-row codes, before being passed on to the output circuitry.
Figure 6 shows the character set.

Display of external On Screen Display (OSD) facilities

The R, G, B and BLAN outputs of the display have the capability to be put in a 3-state mode allowing other OSD devices to take control of the television R, G, B and BLAN signals.

When the BLANIN is held HIGH then the R, G, B and BLAN outputs from display are disabled and the R, G, B and BLAN signals come directly from the RGBIN and BLANIN inputs. This will allow On Screen Display to be placed on top of the captioning without any corruption, leaving the captions intact when the On Screen Display is switched off (BLANIN goes LOW). In this form of operation the RGBIN and RGBOUT pins can be considered transparent; BLANIN goes through the normal output buffer to BLAN.

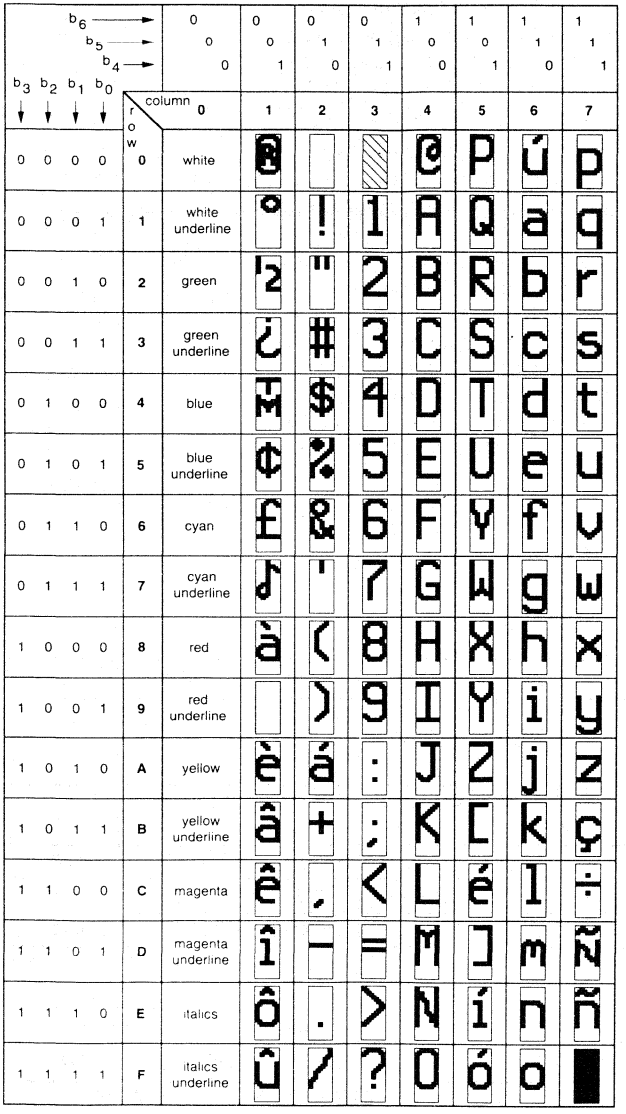
I²C INTERFACE

Table 1 Register map (WRITE)

REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
00	DF$\overline{1}$/2	RGB, BLAN $\overline{+ve}$/–ve	H +ve/$\overline{–ve}$	V +ve/$\overline{–ve}$	H3	H2	H1	H0
01	CLEAR	CH 2/$\overline{1}$	$\overline{\text{NARROW}}$/ WIDE	ACQ OFF	EN1	EN0	M1	M0
02	–	–	–	–	ROW3	ROW2	ROW1	ROW0
03	–	–	–	COL4	COL3	COL2	COL1	COL0
04	–	OSD6	OSD5	OSD4	OSD3	OSD2	OSD1	OSD0

Table 2 Register map (READ)

REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
00	POR	0	0	0	$\overline{F1}$/F2	EDS	PARITY SHUTDOWN	DATA READY
01	PARITY ERROR	DATA BIT 7	DATA BIT 6	DATA BIT 5	DATA BIT 4	DATA BIT 3	DATA BIT 2	DATA BIT 1
02	PARITY ERROR	DATA BIT 7	DATA BIT 6	DATA BIT 5	DATA BIT 4	DATA BIT 3	DATA BIT 2	DATA BIT 1



The '0' and 'zero' use the same character, 4Fh

Fig.6 Character set.

Description of WRITE registers

The write subaddresses auto increment from 0 through to 4 at which point they stay until a new write subaddress is sent. Registers are set to all logic 0 at power-up.

REGISTER 0 WRITE (CONTROL BYTE 1)

D0 to D3 H0 to H3 set the offset position from the start of the line sync pulse, this will be set to a nominal value on reset.

D4 Field sync pulse expected to be negative going logic 0 or positive going logic 1.

D5 Line sync pulse expected to be negative going logic 0 or positive going logic 1.

D6 Video outputs will be positive going logic 0 or negative going logic 1.

D7 Data field select. When set to logic 0 Field 1 is decoded, when set to logic 1 Field 2 is decoded.

REGISTER 1 WRITE (CONTROL BYTE 2)

D0, D1 Display mode selection bits. Table 3 shows the possible display modes.

D2,D3 Enhanced caption mode selection bits. Table 4 shows the possible enhanced caption modes.

D4 When set to logic 1 acquisition of caption data is inhibited to allow the display to be used for On Screen Display purposes.

D5 Acquisition window selection. When set to logic 0 only line 21 is checked for caption data. When set to logic 1, lines 19 to 23 of both fields are checked, allowing encrypted video signals to be handled.

D6 User channel selection.

D7 Clears the page memory when set HIGH. The page memory will be cleared within two fields (30 ms).

Table 3 Display modes

DISPLAY MODE OPTIONS	M1	M0
Video only	0	0
Text mode	0	1
Normal caption mode	1	0
Enhanced caption mode	1	1

Table 4 Enhanced caption modes

ENHANCED CAPTION MODES	EN1	EN0
Enhanced caption modes	EN1	EN0
Shadowed character/Video background	0	0
Shadowed character/Mesh background	0	1
Normal character/Video background	1	0
Normal character/Mesh background	1	1

REGISTER 2 WRITE (ON SCREEN DISPLAY DATA ROW ADDRESS)

D0 to D3 Row 0 to 3, sets the row address for on screen display. This stored value will be incremented by overflow increments of Register 3.

REGISTER 3 WRITE (ON SCREEN DISPLAY DATA COLUMN ADDRESS)

D0 to D4 Columns 0 to 4, sets the column address for On Screen Display. This stored value will be incremented by writes to Register 4.

REGISTER 4 WRITE (ON SCREEN DISPLAY DATA)

D0 to D6 OSD0 to 6, On Screen Display data bits writing to this register causes Register 3 to increment its stored value.

Description of READ registers

The read subaddresses auto increment from 0 through to 2 at which point they stay until a new read subaddress is sent.

REGISTER 0 READ (STATUS)

All these bits are reset to logic 0 after the register is read.

D0 Data ready (new data has been acquired)

D1 Parity error shut-down, goes HIGH when SAA5252 has a parity shut-down condition.

D2 Indicates the following bytes are extended data service bytes

D3 Indicates Field 1 or Field 2 data bytes

D7 Indicates a Power-On Reset (POR) has occurred, all I²C write registers have been reset to zero.

REGISTER 1 READ (FIRST DATA BYTE)

D0 to D6 Data Bit 1 to Data Bit 7 (see note).

D7 Parity error flag bit. Bit goes HIGH when a parity error has occurred.

REGISTER 2 READ (SECOND DATA BYTE)

D0 to D6 Data Bit 1 to Data Bit 7 (see note).

D7 Parity error flag bit. Bit goes HIGH when a parity error has occurred.

Note In the Line 21 Specification data bits are numbered D1 to D8

Interface to Microcontroller using I²C-bus

The interface to the microcontroller is via the two-wire serial I²C-bus, and optionally by a Data-Ready signal ($\overline{DR}$). On power up the microcontroller initializes the device by an I²C WRITE to Registers 0 (Control Byte 1). The I²C subaddress is then auto incremented to point to Register 1 (Control Byte 2). These two registers configure the device to the users requirements.

If the device is to be used for data acquisition only, then there are three methods by which the microcontroller can be informed of the arrival of valid Line 21 data:

- It can poll the $\overline{DR}$ pin, if the function has been enabled, and wait for it to go LOW.
- It can use the negative edge of the $\overline{DR}$ signal to cause an interrupt.
- It can poll the Data Ready bit (bit D0 of the status byte, I²C READ Register 0).

When valid data is detected, the microcontroller must initiate an I²C READ of Registers 0, 1 and 2. The first and second data bytes from the most recently received Line 21 are in Register 1 and Register 2 respectively.

The $\overline{DR}$ pin, and the Data Ready bit (Status Byte D0) will be cleared after any register has been read. POR is reset after Register 0 has been read.

STAND-ALONE (NON I²C) OPERATION

To set the SAA5252 for stand-alone operation pin 2 (I²C/$\overline{DC}$) is tied LOW. This will change the operation of the SCL, SDA and $\overline{DR}$ pins to mode select inputs which will select as shown in Table 5.

In the caption mode the SAA5252 operates in the basic Normal character/Black background mode. This complies with the FCC ruling. In the Enhanced caption mode the set up will be Shadowed character/Video background. SDA and SCL in the stand-alone operation act as bits M0 and M1 in Table 3

Table 5 Stand-alone modes

$\overline{DR}$	SCL	SDA	MODE OF OPERATION	CHANNEL RECEPTION
0	0	0	Video mode	Channel 1
0	0	1	Text mode	Channel 1
0	1	0	Normal captions	Channel 1
0	1	1	Enhanced captions	Channel 1
1	0	0	Video mode	Channel 2
1	0	1	Text mode	Channel 2
1	1	0	Normal captions	Channel 2
1	1	1	Enhanced captions	Channel 2

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

Integrated VIP and teletext decoder (IVT2.0)

SAA5260

FEATURES

- Complete teletext decoder in a single 48-pin DIL package
- Single +5 V power supply
- Digital data slicer and display clock phase-locked loop reduce peripheral components to a minimum
- Both video and scan related synchronization modes are supported
- 4096 colour palette, with 16 different foreground plus 16 different background colours
- Full row and border background colours covering the whole screen area
- Background colour control characters for highlighting text areas
- 224 characters in ROM (12 x 10 matrix), giving wide language coverage and additional graphics symbols for on-screen displays
- Double width and double size decoding as well as double height
- Foreground character processing for language extension possible without display flicker
- Analog RGB outputs with simple interface to colour decoder ICs
- Data capture performance similar to SAA5231 (VIP2)
- 5 channel acquisition system for fast page capture
- Pointer system to connect any acquisition channel to any page memory
- Interfaces to 32 K x 8-bit static RAM (8 K x 8 also possible)
- Extension packet option including full error correction in hardware (8/4 and 24/18 Hamming)
- 7-bit + parity, 8-bit, full page Hamming and mixed Hamming/7-bit + parity acquisition options, selected per channel to allow e.g. optimum TOP decoding
- End of page detectors with interrupt generation for fast data processing
- Separate text and video signal quality detectors, 625/525 video status and language version all readable via I²C-bus
- Automatic ODD/$\overline{\text{EVEN}}$ output control with manual override
- Control of display PLL free-run and rolling header via I²C-bus
- VCS to SCS mode for stable 525 line status display
- Option for battery back-up of page memory.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5	5.5	V
I_{DD}	supply current	–	75	150	mA
V_{syn}	sync amplitude	0.1	0.3	0.6	V
V_{vid}	video amplitude	0.7	1	1.4	V
f_{XTAL}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature range	–20	–	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5260P/E	48	DIL	plastic	SOT240

DESCRIPTION

The SAA5260 is a single-chip teletext decoder IC for decoding 625-line based World System Teletext transmissions. The device is based on the IVT1.0 (SAA5246) with additional features to provide a higher performance decoder. A larger memory (32 K x 8) can be connected for faster access to pages and better display facilities are provided, including more symbols and colours.

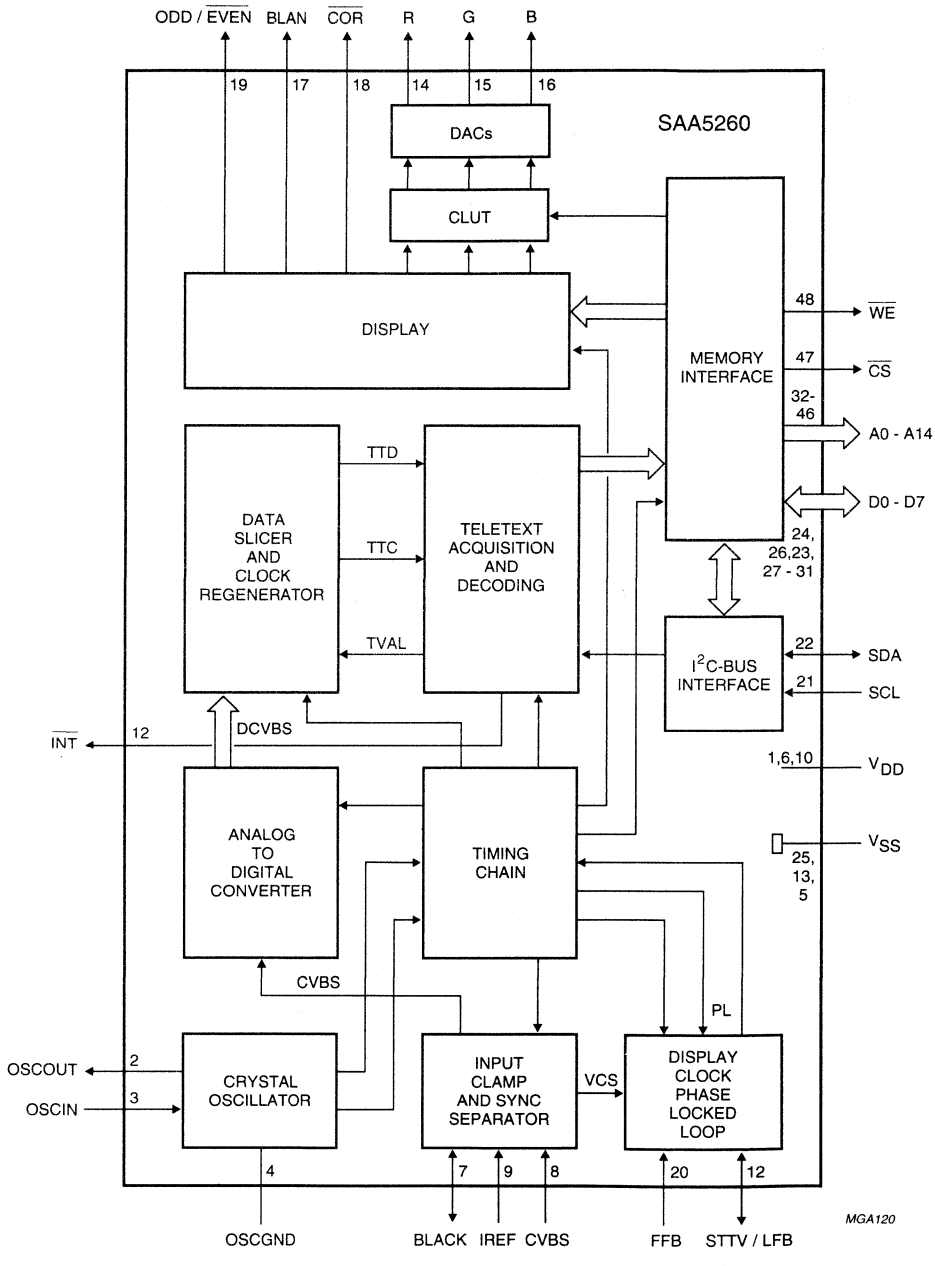


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DD}	1, 6, 10	+5 V supply
OSCOUT	2	27 MHz crystal oscillator output
OSCIN	3	27 MHz crystal oscillator input
OSCGND	4	0 V crystal oscillator ground
V_{SS}	5, 13, 25	0 V ground
BLACK	7	video black level storage pin, connected to ground via a 100 nF capacitor
CVBS	8	composite video input pin. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor
IREF	9	reference current input pin, connected to ground via a 27 kΩ resistor
STTV/LFB	11	sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode)
$\overline{INT}$	12	interrupt output from end of page detector, X/27, X/29 and 8/30 flags
R	14	dot rate character output of the RED colour information
G	15	dot rate character output of the GREEN colour information
B	16	dot rate character output of the BLUE colour information
BLAN	17	dot rate fast blanking output
$\overline{COR}$	18	programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages. Open drain output
ODD/$\overline{EVEN}$	19	25 Hz output synchronized with the CVBS input's field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents
FFB	20	field flyback input
SCL	21	serial clock input for I²C-bus. It can still be driven HIGH during power-down of the device
SDA	22	serial data port for the I²C-bus. Open drain output. It can still be driven HIGH during power-down of the device
D2	23	data input/output for external RAM
D0	24	data input/output for external RAM
D1	26	data input/output for external RAM
D3 to D7	27 to 31	data inputs/outputs for external RAM
A0 to A14	32 to 46	address outputs for external RAM
$\overline{CS}$	47	output to RAM if memory not to be cleared on power-up
$\overline{WE}$	48	write enable to external RAM

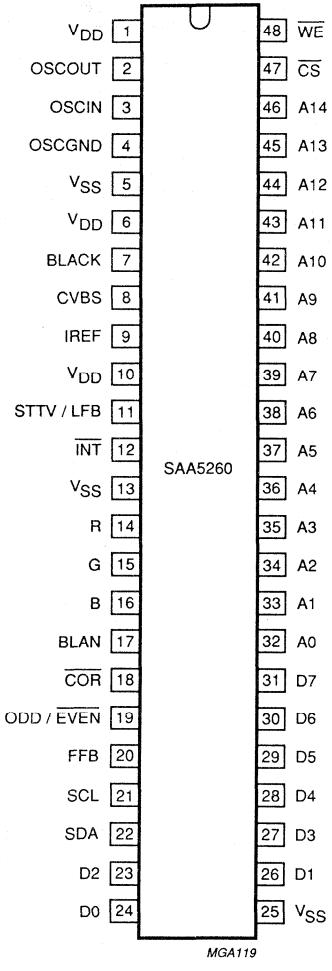


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	−0.3	6.5	V
V_I	input voltage (any input)	−0.3	V_{DD}+0.5	V
V_O	output voltage (any output)	−0.3	V_{DD}+0.5	V
I_O	output current (each output)	−	±10	mA
I_{IOK}	DC input or output diode current	−	±20	mA
T_{amb}	operating ambient temperature range	−20	70	°C
T_{stg}	storage temperature range	−55	125	°C
V_{stat}	electrostatic handling human body model (note 1)	−2000	2000	V

Note

1. The human body model ESD simulation is equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor; this produces a single discharge transient. Reference Philips Semiconductors test method UZW-B0/FQ-A302 (compatible with MIL-STD method 3015.7).

Failure Rate

The failure rate at T_{amb} = 55 °C will be a maximum of 1000 FITS (1 FIT = 1 x 10^{-9} failures per hour).

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = −20 to +70 °C, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range		4.5	5	5.5	V
I_{DD}	total supply current		–	75	150	mA
Inputs						
CVBS						
V_{syn}	sync amplitude		0.1	0.3	0.6	V
t_{syn}	delay from CVBS to TCS output from STTV buffer (nominal video, average of leading/trailing edge)		−150	0	150	ns
t_{syd}	change in CVBS to TCS delay between all black and all white video input at nominal levels		0	–	25	ns
$V_{vid(p-p)}$	video input amplitude (peak-to-peak)		0.7	1	1.4	V
	display PLL catching range		±7	–	–	%
Z_{src}	source impedance		–	–	250	Ω
C_I	input capacitance		–	–	10	pF
IREF						
R_g	resistor to ground		–	27	–	kΩ
V_g	voltage on pin 9		–	$V_{DD}/2$	–	V
LFB						
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	µA
I_I	input current	note 1	−1	–	1	mA
t_{LFB}	delay between LFB front edge and input video line sync		–	250	–	ns
FFB						
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	µA
I_I	input current	note 1	−1	–	1	mA
SCL						
V_{IL}	LOW level input voltage		−0.3	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	µA
f_{SCL}	clock frequency		0	–	150	kHz
t_r	input rise time	10% to 90%	–	–	2	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_f	input fall time	90% to 10%	–	–	2	µs
C_I	input capacitance		–	–	10	pF
Inputs/outputs						
BLACK						
C_{blk}	storage capacitor to ground		–	100	–	nF
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	10	µA
D0 TO D7						
V_{IL}	LOW level input voltage		–0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	10	µA
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA	2.4	–	V_{DD}	V
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
C_L	load capacitance		–	–	120	pF
SDA						
V_{IL}	LOW level input voltage		–0.3	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	10	µA
C_I	input capacitance		–	–	10	pF
t_r	input rise time	10% to 90%	–	–	2	µs
t_f	input fall time	90% to 10%	–	–	2	µs
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.5	V
t_f	output fall time	3 to 1 V	–	–	200	ns
C_L	load capacitance		–	–	400	pF
Outputs						
STTV						
G_{stt}	gain of STTV relative to video input		0.9	1.0	1.1	
V_{tcs}	TCS amplitude		0.2	0.3	0.45	V
V_{DCs}	DC shift between TCS output and nominal video output		–	–	0.15	V
I_O	output drive		–	–	3.0	mA
C_L	load capacitance		–	–	100	pF
A0 TO A14 ADDRESS OUTPUT TO MEMORY						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA	2.4	–	V_{DD}	V
C_I	input capacitance		–	–	120	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
$\overline{WE}$						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
CS						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
C_L	load capacitance		–	–	120	pF
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
R, G AND B						
R_L	load resistance to V_{SS}		–	150	–	Ω
I_{OL}	output current (black level)		–10	0	10	μA
I_{OL}	output current (full amplitude)	at nominal V_{DD}	–6.0	–6.67	–7.3	mA
C_L	load capacitance		–	–	20	pF
t_r	output rise time	10% to 90%; R_L = 150 Ω; C_L = 20 pF	–	–	20	ns
t_f	output fall time	90% to 10%; R_L = 150 Ω; C_L = 20 pF	–	–	20	ns
BLAN						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA	1.1	–	–	V
V_{OH}	HIGH level output voltage	I_{OH} = 0 mA	–	–	2.8	V
V_{OH}	allowed voltage at pin	with extenal pull-up	–	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
ODD/$\overline{EVEN}$						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –1.6 mA	V_{DD}–0.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
$\overline{COR}$ (OPEN DRAIN)						
V_{OH}	pull-up voltage at pin		–	–	V_{DD}	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.4	V
V_{OL}	LOW level output voltage	I_{OL} = 5 mA	0	–	1.0	V
C_L	load capacitance		–	–	25	pF
t_f	output fall time	load resistor of 1.2 kΩ to V_{DD}; measured between V_{DD} –0.5 and 1.5 V	–	–	50	ns
I_{LO}	output leakage current	V_I = 0 to V_{DD}	–10	–	10	µA
TSK	skew delay between display outputs R, G, B, $\overline{COR}$, and BLAN		–	–	20	ns
$\overline{INT}$ (OPEN DRAIN)						
V_{OH}	pull-up voltage at pin		–	–	V_{DD}	V
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
I_{LO}	output leakage current		–10	–	10	µA
C_L	load capacitance		–	–	25	pF
t_f	output fall time	load resistor of 3.3 kΩ to V_{DD} measured between 4 V and 1 V	–	–	50	ns
Timing						
I²C-BUS						
f_{DAT}	I²C data rate for:					
	all registers		–	–	150	kHz
	all registers except display RAM write/reads		–	–	350	kHz
	other devices on bus (IVT will not lock up)		–	–	400	kHz
t_{LOW}	clock LOW period		1.4	–	–	µs
t_{HIGH}	clock HIGH period		1.4	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		170	–	–	ns
$t_{SU;STO}$	set-up time from clock HIGH to STOP		4	–	–	µs
t_{BUF}	START set-up time following a STOP		4	–	–	µs
$t_{HD;STA}$	START hold time		1.4	–	–	µs
$t_{SU;STA}$	START set-up time following clock LOW-to-HIGH transition		1.4	–	–	µs
RAM INTERFACE						
t_{CY}	cycle time		–	500	–	ns
t_{ADDR}	address active time		450	500	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{ACC}	access time from address		–	–	150	ns
t_{DH}	data hold time from address		0	–	–	ns
t_{WE}	$\overline{WE}$ LOW from address change		40	–	–	ns
t_{WEW}	$\overline{WE}$ pulse width		100	–	–	ns
t_{DS}	data set-up time to $\overline{WE}$ HIGH		60	–	–	ns
t_{DHWE}	data hold time from $\overline{WE}$ HIGH		0	–	20	ns
t_{WR}	write recovery time		20	–	–	ns
t_{DE}	data enable from $\overline{WE}$ LOW		10	–	–	ns

Note to the characteristics

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. Series current limiting resistors must be used to limit the input currents to ± 1 mA.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

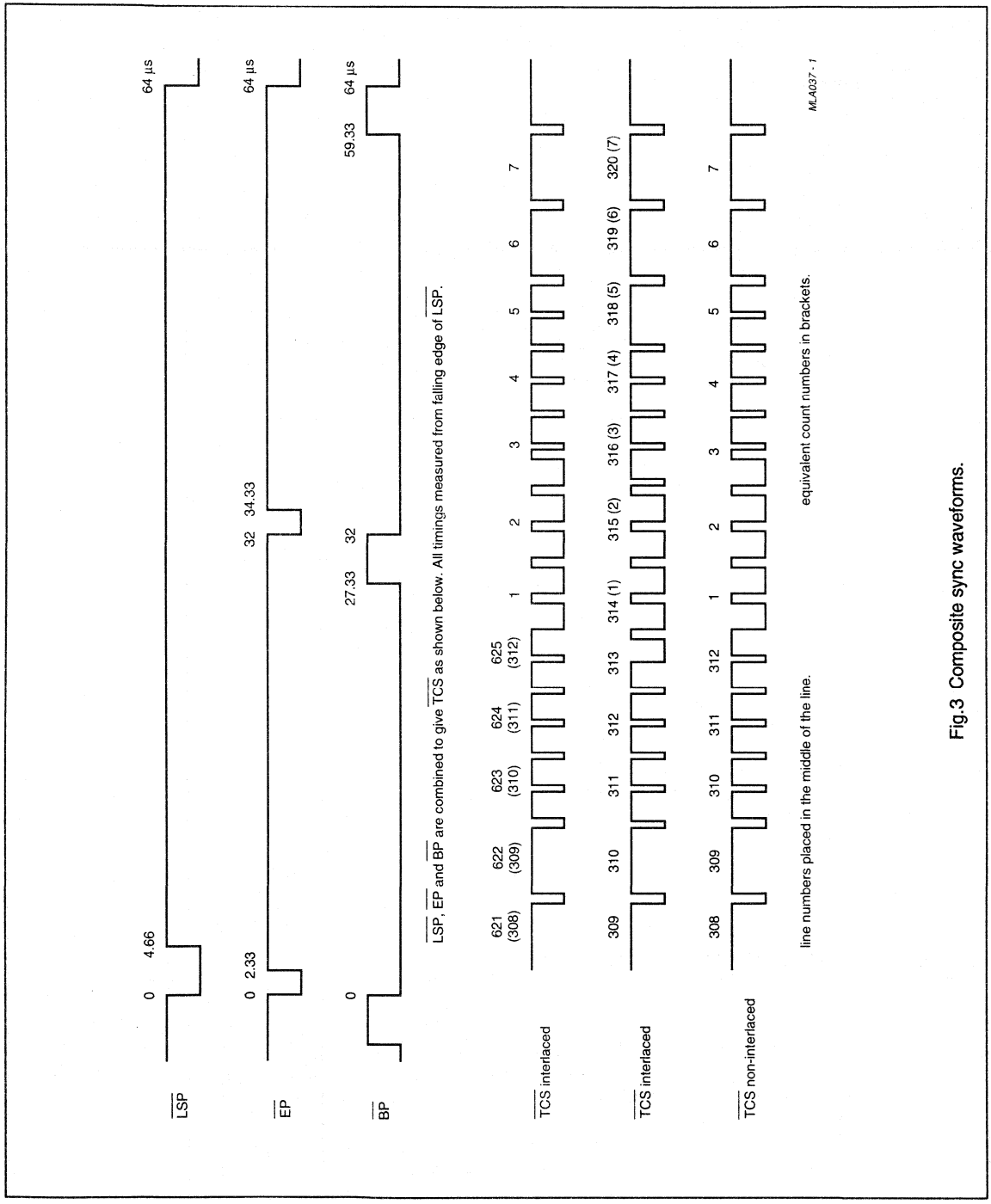


Fig.3 Composite sync waveforms.

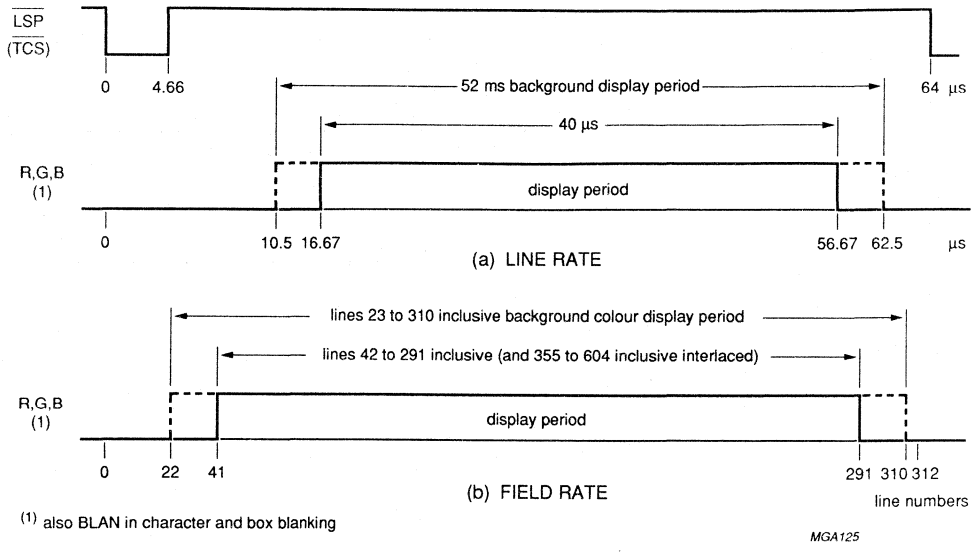


Fig.4 Display output timing (a) line rate (b) field rate.

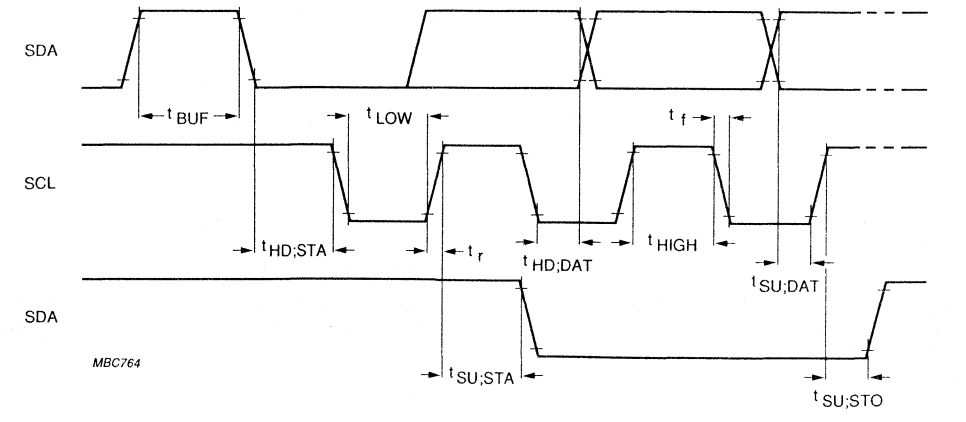


Fig.5 I²C-bus timing.

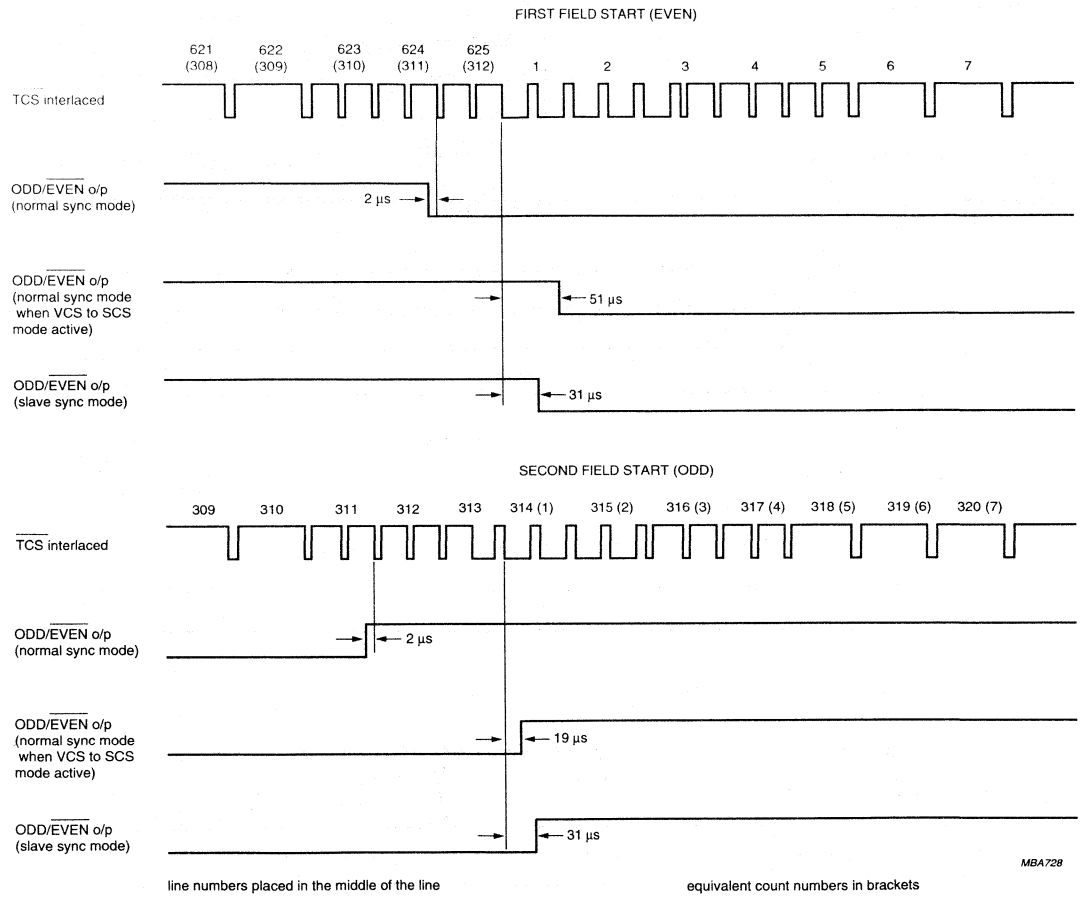


Fig.6 ODD/EVEN timing.

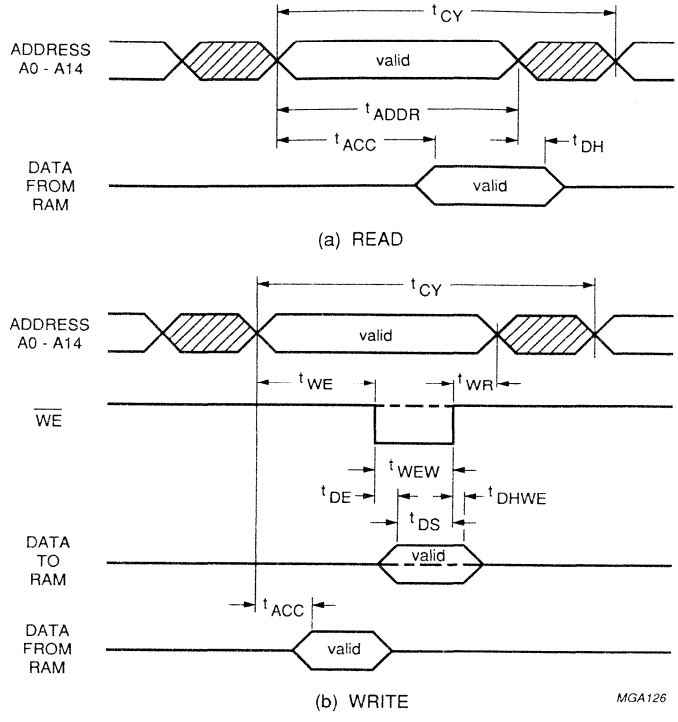


Fig.7 Memory interface timing (a) read (b) write.

APPLICATION INFORMATION

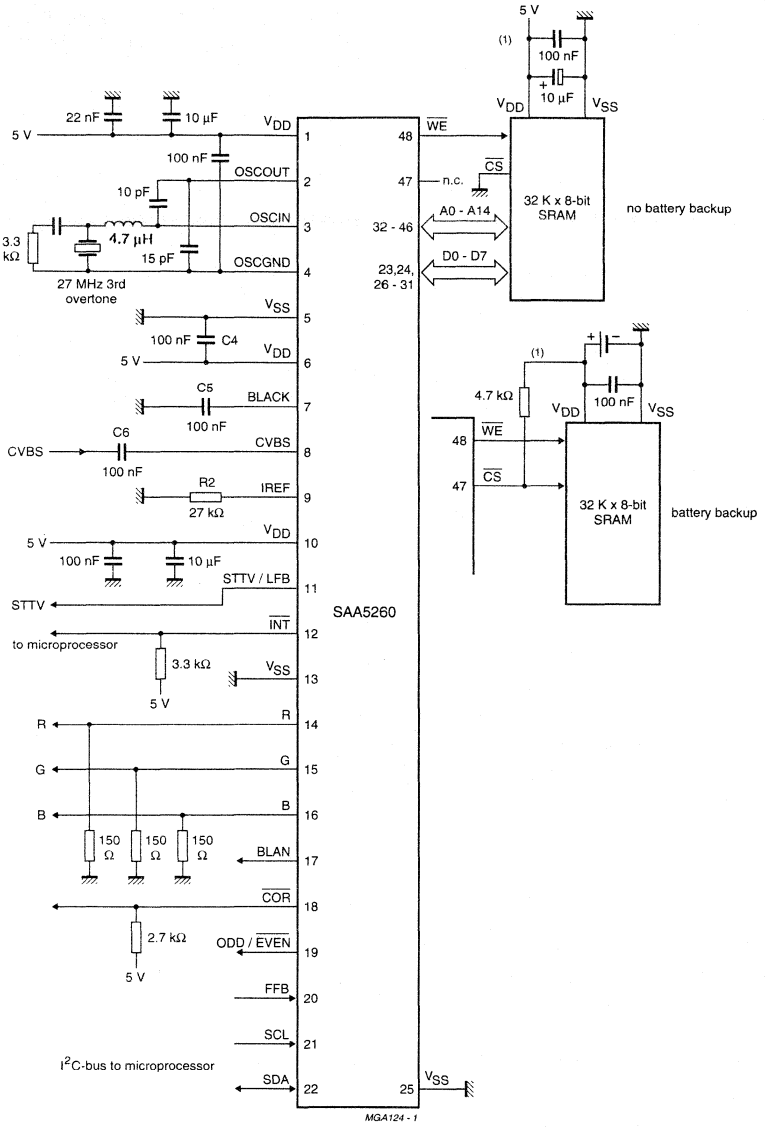
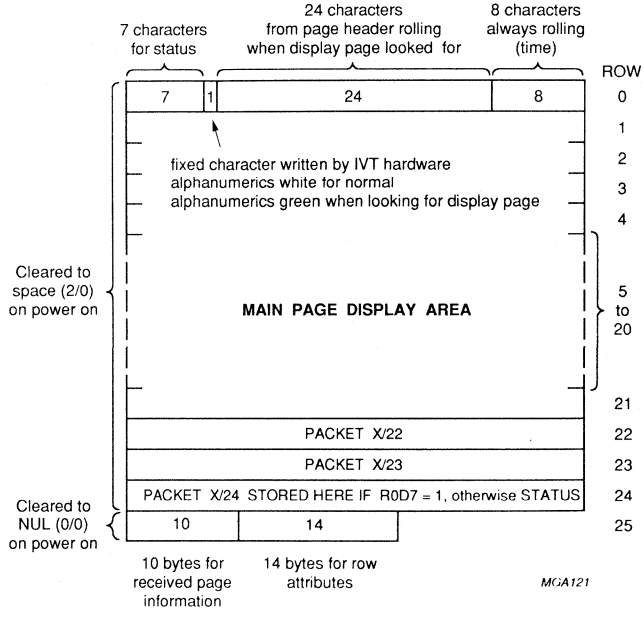


Fig.8 Application diagram.

(1) Optional connections if battery backed up memory required. The 5 V supply shown comes from battery. If battery back-up is not used, then $\overline{CS}$ of RAM is connected to ground and the $\overline{CS}$ output from the device is not used.

SAA5260 page memory organization

The organization of the page memory is shown in Fig.9. The display format is 40 characters by 25 rows. Rows 0 to 23 form the teletext page; row 24 is available for software generated status messages and FLOF/FASTEXT prompt information.



Row 0:
Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by SAA5260 to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25:
The first 10 bytes of row 25 contain control data relating to the received page as shown in Table 1.

Fig.9 Basic page memory organization.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

Page number

MAG magazine

PU page units

PT page tens

PBLF page being looked for

$\overline{\text{FOUND}}$ LOW for page has been found

HAM.ER Hamming error in corresponding byte

Page sub-code

MU minutes units

MT minutes tens

HU hours units

HT hours tens

C4-C14 transmitted control bits.

The remaining 14 bytes of row 25 contain the row attributes for defining the default background colour of each row and the chapter from which it is to be displayed, as shown in Table 2.

Table 2 Row 25 row attributes

D0	TR	R0R	R2R	R4R	R6R	R8R	R10R	R12R	R14R	R16R	R18R	R20R	R22R	R24R
D1	TG	R0G	R2G	R4G	R6G	R8G	R10G	R12G	R14G	R16G	R18G	R20G	R22G	R24G
D2	TB	R0B	R2B	R4B	R6B	R8B	R10B	R12B	R14B	R16B	R18B	R20B	R22B	R24B
D3	-	DR0	DR2	DR4	DR6	DR8	DR10	DR12	DR14	DR16	DR18	DR20	DR22	DR24
D4	BR	R1R	R3R	R5R	R7R	R9R	R11R	R13R	R15R	R17R	R19R	R21R	R23R	-
D5	BG	R1G	R3G	R5G	R7G	R9G	R11G	R13G	R15G	R17G	R19G	R21G	R23G	-
D6	BB	R1B	R3B	R5B	R7B	R9B	R11B	R13B	R15B	R17B	R19B	R21B	R23B	-
D7	-	DR1	DR3	DR5	DR7	DR9	DR11	DR13	DR15	DR17	DR19	DR21	DR23	-
COLUMN	10	11	12	13	14	15	16	17	18	19	20	21	22	23

R, G and B are the settings of the default background colour attribute. They only correspond to RED, GREEN and BLUE colour outputs when the colour look-up table is in the default condition; at other times, they are simply entries in the colour look-up table.

T Top border of screen, above row 0 (or above status row if R1D7 = 1)

B Bottom border of screen, below the status row (or below row 23 if R10D7 = 1)

R1 etc. Row 1 display

DR2 etc. Display row 2 etc. defines whether the text for this display row comes from the normal display chapter register (0) or supplementary display chapter register (1)

These letters are combined as appropriate, e.g. R8R = red default background for row 8, BG = green default background for bottom screen border.

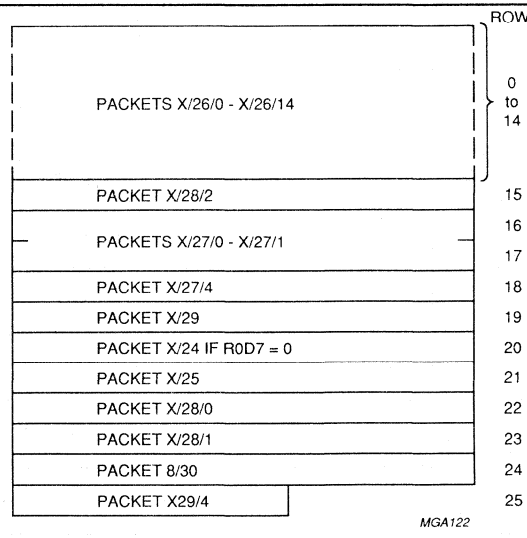


Fig.10 Organization of the extension memory.

Extension packet memory organization

When in extension packet enable mode, the rows of information are organized as shown in Fig.10.

The page-related extension packets are stored in the next higher memory chapter relative to the corresponding basic page data, e.g. basic page chapter 6, extension packets chapter 7.

Some extension packets are not page related; these are stored in the chapters as shown in Tables 3 and 4.

Packet 8/30: Stored in a chapter according to the designation code. Pairs of designation codes are stored in the same chapter, owing to the use of the LSB as a flag indicating VBI or full channel.

Table 3 Packet 8/30 storage

PACKET	CHAPTER
8/30/0, 8/30/1	1
8/30/2, 8/30/3	3
8/30/4, 8/30/5	5
8/30/6, 8/30/7	7
8/30/8, 8/30/9	9
8/30/10, 8/30/11	11
8/30/12, 8/30/13	13
8/30/14, 8/30/15	15

Packet 29: Two versions are stored in row 19, X/29/0 (for colour definition) and X/29/1 (for character set definition) and one in row 25, X/29/4.

Table 4 Packet 29 storage

PACKET	CHAPTER
8/30/0 and 4	1
1/29/0 and 4	3
2/29/0 and 4	5
3/29/0 and 4	7
4/29/0 and 4	9
5/29/0 and 4	11
6/29/0 and 4	13
7/29/0 and 4	15
8/29/1	17
1/29/1	19
2/29/1	21
3/29/1	23
4/29/1	25
5/29/1	27
6/29/1	29
7/29/1	31

Register maps

SAA5260 mode registers are shown in Table 5. R0 to R15 are WRITE only; R16A is READ/WRITE; R16B and R16C are READ only.

Table 5 Register map

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
Mode	0	X24 POS	EXTN. PACKET ENABLE	$\overline{\text{DEW}}$/ FULL FIELD	DISABLE HDR ROLL	B.T. NUMBER ENABLE	POL	BOX TIME	BOX HEADER
Sync	1	VCS TO SCS	FREE RUN PLL	AUTO ODD/ $\overline{\text{EVEN}}$	DISABLE ODD/ $\overline{\text{EVEN}}$	VCR	TCS ON	T1	T0
Acq. control	2	ACQ. $\overline{\text{ON}}$/OFF	ACQ. CCT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request	3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
Acq. Mode A	4	–	–	–	H4	H3	H2	H1	H0
Acq. Mode B	5	–	–	–	S4	S3	S2	S1	S0
Display chapter (normal)	6	–	–	–	A4	A3	A2	A1	A0
Display chapter (supplm.)	7	–	–	CLUT SELECT	A4	A3	A2	A1	A0
Display (normal)	8	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display (news flash)	9	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control	10	STATUS $\overline{\text{BTM}}$/TOP	CURSOR ON	$\overline{\text{CONCEAL}}$ REVEAL	$\overline{\text{TOP}}$/ BOTTOM	$\overline{\text{SINGLE}}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0
CLUT data 1	11	G3	G2	G1	G0	R3	R2	R1	R0
CLUT data 2	12	A3	A2	A1	A0	B3	B2	B1	B0
Active chapter	13	–	–	CLEAR MEM.	A4	A3	A2	A1	A0
Active row	14	–	CURSOR MOVE	INC BY ROW	R4	R3	R2	R1	R0
Active column	15	$\overline{\text{R16C}}$/ R16C	$\overline{\text{R16A}}$/ R16B	C5	C4	C3	C2	C1	C0

Table 5 Register map *(continued)*

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
Active data	16A	D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)
Device status	16B	$\overline{625}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	TEXT SIGNAL QUALITY	VCS SIGNAL QUALITY
End of page flags	16C	8/30 ARRIVED	X/29 ARRIVED	X/27 ARRIVED	AC4	AC3	AC2	AC1	AC0

Notes to Table 5

1. – indicates these bits are inactive and must be written to logic 0 for future compatibility.
2. All bits in registers R0 to R15 are cleared to logic 0 on power-up, except bits D0 and D1 of registers R1, R8 and R9 which are set to logic 1. The CLUT data (accessed from R11 and R12) is cleared to normal "level 1" colours.

Register description

R0 MODE - auto increments to Register 1

BOX HEADER	Selects automatic boxing of first 7 characters on display Row 0
BOX TIME	Selects automatic boxing of last 8 characters on display Row 0
POL	Selects polarity of STTV output or LFB and FFB input signals. (When POL = 1, then TCS will be positive-going syncs and LFB/FFB will be negative; when POL = 0, TCS will be negative-going syncs and LFB/FFB positive)
B.T.NUMBERS ENABLE	Selects blast-through numbers instead of supplementary background colour attributes
DISABLE HDR ROLL	Stops the display update of rolling time and green rolling header during page request when = 1. Time updates on page reception only
$\overline{\text{DEW}}$/FULL FIELD	Field-flyback or full channel mode
EXTN. PACKET ENABLE	Enables reception and storage of extension packets in 2 K x 8-bits per page when = 1
X24 POS	Automatic display of FASTEXT prompt row when = 1

R1 SYNC - auto increments to Register 2

T0, T1	Interlace/non-interlace 312/313 line or scan sync control
TCS ON	Text composite sync or direct sync select
VCR	Selects VCR mode for display PLL
DISABLE ODD/$\overline{\text{EVEN}}$	ODD/$\overline{\text{EVEN}}$ unconditionally forced low if = 1
AUTO ODD/$\overline{\text{EVEN}}$	If = 1 then ODD/$\overline{\text{EVEN}}$ output only active when no picture is present
FREE RUN PLL	Forces display PLL to free run at 6 MHz when = 1
VCS TO SCS	Connects VCS from video sync separator to display field sync detector to enable stable display status messages with 60 Hz rasters

R2 ACQ. CONTROL - auto increments to Register 3

START COLUMN	Start column for page request data
TB	Must be logic 0 for normal operation
ACQ. CCT	Selects one of five acquisition circuits
ACQ. $\overline{\text{ON}}$/OFF	Entire acquisition function turned off when = 1

R3 PAGE REQUEST DATA - does not auto increment

Table 6 shows the full register map for page requests. The mapping of Register 3 is dependent on the start column indicated in Register 2.

Table 6 Register map for page requests (R3)

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	$\overline{\text{CLEAR}}$ $\overline{\text{RX}}$	$\overline{\text{ROLL}}$	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0
7	CH4	CH3	CH2	CH1	CH0

Notes to Table 6

1. When the DO CARE bit is set to logic 1, this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0, the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
2. There are five versions of Table 6, one for each acquisition channel. This allows five simultaneous page requests.
3. $\overline{\text{ROLL}}$ set low to give rolling headers on page search.
4. $\overline{\text{CLEAR}}$ $\overline{\text{RX}}$ set low to clear old page on first reception.
5. Columns auto-increment on successive I²C-bus transmission bytes. Column 7 auto increments back to Column 0.
6. CH0 to CH4 are pointer bits (LSB to MSB) giving the current chapter address for that acquisition channel.

Where:

Page number

MAG	magazine
PU	page units
PT	page tens
$\overline{\text{HOLD}}$	set LOW to hold and not update page
CH	chapter address bit

Page sub-code

MU	minutes units
MT	minutes tens
HU	hours units
HT	hours tens.

R4 ACQ. MODE A - auto increments to Register 5

R5 ACQ. MODE B - auto increments to Register 6

These bits determine the type of acquisition to be performed by each of the five acquisition channels. H is Hamming and S is select. The four combinations are shown in Table 7.

Table 7 Truth table for acquisition Modes A and B

H	S	FUNCTION
0	0	7-bit plus parity
0	1	8-bit (no error checking)
1	0	8/4 Hamming checking over the full page
1	1	mixed 8/4 Hamming (Columns 0 to 7, 20 to 27) and 7-bit plus parity (Columns 8 to 9, 28 to 39)

R6 NORMAL DISPLAY CHAPTER - auto increments to Register 7

A0 to A4 Selects one of 32 chapters for display. This register is used for full pages of display, when the current display row bit is set to 0

R7 SUPPLEMENTARY DISPLAY CHAPTER - auto increments to Register 8

A0 to A4 Selects one of 32 chapters for display This register is used when the current display row bit is set to 1, for e.g. status messages on a text page

CLUT SELECT Determines which CLUT will be written to by Registers 11 and 12. If set to 1, access is to the supplementary display chapter colour entries

R8 NORMAL DISPLAY CONTROL - auto increments to Register 9

R9 NEWSFLASH/SUBTITLE DISPLAY CONTROL - auto increments to Register 10

PON Picture on

TEXT Text on

COR Contrast reduction on

BKGND Background colour on.

These functions have IN and OUT bits referring to inside and outside the boxing function respectively.

R10 DISPLAY CONTROL - does not auto increment

BOX ON 0 Boxing function allowed on Row 0

BOX ON 1-23 Boxing function allowed on Row 1-23

BOX ON 24 Boxing function allowed on Row 24

STATUS ROW $\overline{\text{BTM}}$/TOP Row 24 displayed above or below the main text

R11 CLUT DATA 1 - auto increments to Register 12

R0 to R3	Red colour value
G0 to G3	Green colour value

R12 CLUT DATA 2 - auto increments to Register 11

B0 to B3	Blue colour value
A0 to A3	Address of colour entry

R13 ACTIVE CHAPTER - auto increments to Register 14

A0 to A4	Active chapter address for I²C-bus

CLEAR MEM.Clears the external memory to power-on state

R14 ACTIVE ROW - auto increments to Register 15

R0 to R4	Active row address for I²C-bus
INC BY ROW	When set the active address increments by row on R16A accesses instead of by column
CURSOR MOVE	When set the active I2C Row and columns are read and used to update the cursor position on the display

R15 ACTIVE COLUMN - auto increments to Register 16A/16B/16C depending on bits D6/7 of Register 15

C0 to C5	Active column address for I²C-bus
$\overline{\text{R16A}}$/R16B	Selects either Register 16A (read/write) or 16B (read only)
$\overline{\text{R16C}}$/R16C	Selects Register 16C (read only) or allows selection of Registers 16A or 16B

R16A ACTIVE DATA

D0 to D7 (R/W)	Data bits (read/write)

R16B DEVICE STATUS - does not auto increment

VCS SIGNAL QUALITY	Indicates that video signal quality is good and PLL is phase-locked to input video signal when = 1
TEXT SIGNAL QUALITY	If a good teletext signal is being received, then = 1
ROM VER R4-0	Indicates language/ROM variant. For Western European = 10000
$\overline{\text{625}}$/525 SYNC	If the input video is a 525 line signal then = 1

R16C END OF PAGE AND PACKET FLAGS - does not auto increment

AC0 to AC4	Set to 1 if an end of page has been detected in the corresponding acquisition channel
X/27 ARRIVED	Set to 1 if packet X27/0-1 and 4 arrives
X/29 ARRIVED	Set to 1 if packet X29/0-1 arrives
8/30 ARRIVED	Set to 1 if packet 8/30/0-3 arrives

Table 8 Crystal characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Crystal (27 MHz, 3rd overtone)					
C1	series capacitance	-	1.7	-	pF
C0	parallel capacitance	-	5.2	-	pF
CL	load capacitance	-	20	-	pF
Rr	resonant resistance	-	-	50	Ω
R1	series resistance	-	20	-	Ω
Xa	ageing	-	-	±5	10^{-6}/yr
Xj	adjustment tolerance	-	-	±25	10^{-6}
Xd	drift	-	-	±25	10^{-6}

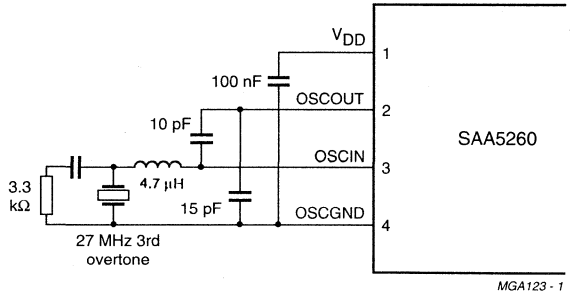


Fig.11 Crystal oscillator application diagram.

CLOCK SYSTEMS

Crystal oscillator

The crystal is a conventional 2-pin design operating at 27 MHz. It is capable of oscillating with both fundamental and third overtone mode crystals. External components should be used to suppress the fundamental output of the third overtone, as shown in Fig.11. The crystal characteristics are given in Table 8.

Character sets

The WST specification allows the selection of national character sets via the page header transmission bits, C12 to C14. For languages based on the Roman alphabet, the basic 96 character sets differ only in 13 national option characters. For the Western European version of SAA5260, these national option characters are shown in Table 9, with reference to their position in the basic character matrix illustrated in Table 10.

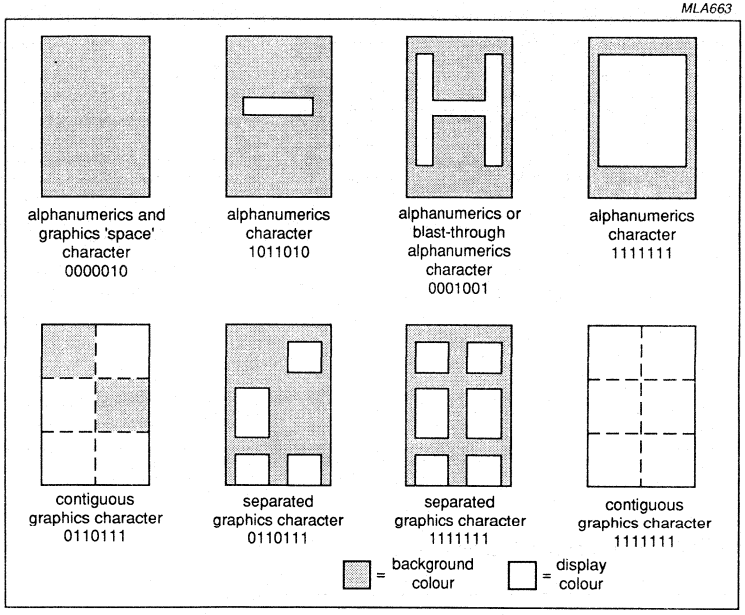


Fig.12 Character format.

Table 9 SAA5260P/E Western European national option character set

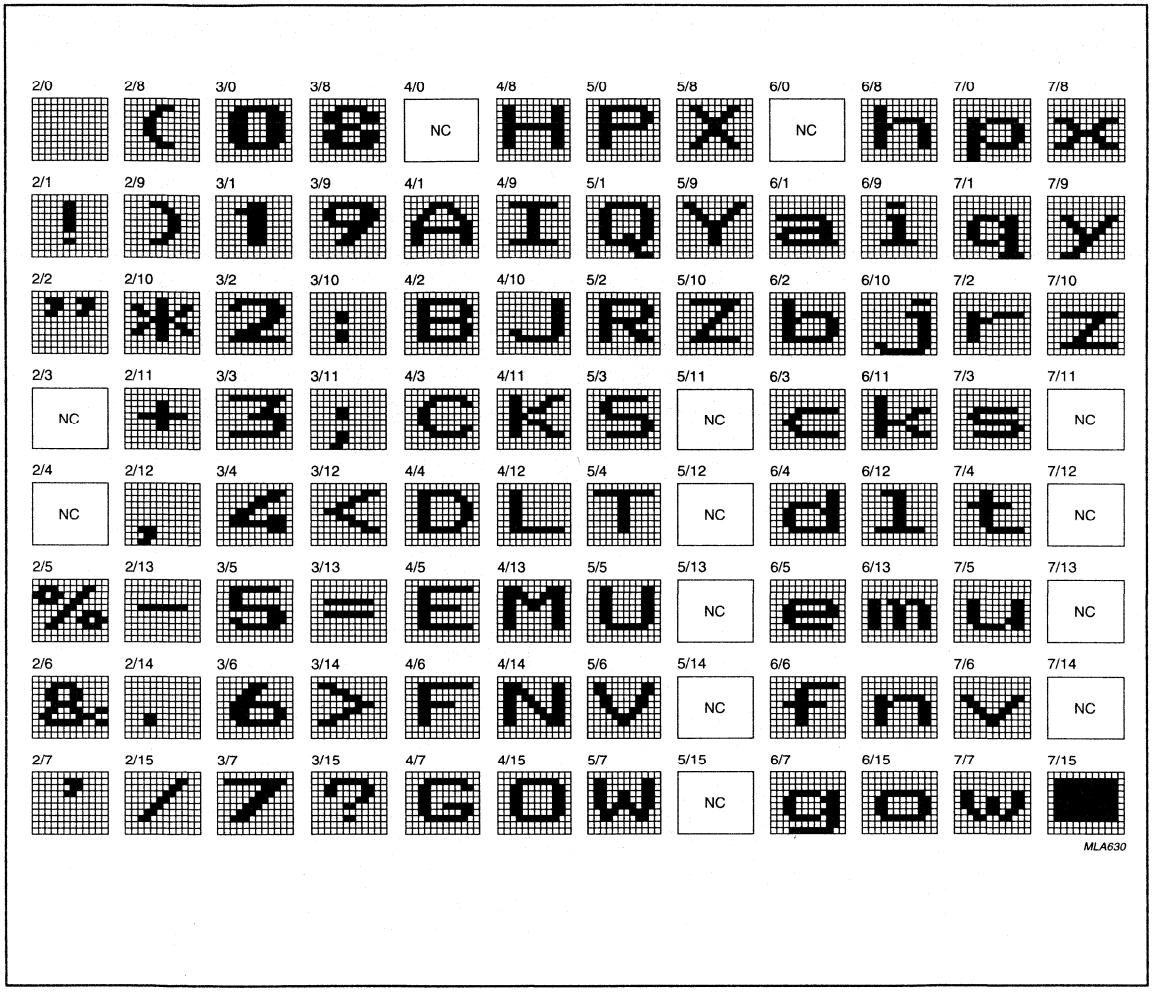
The SAA5260 automatically decodes transmission bits C12 to C14. Table 11 illustrates the 8-bit decoding of the character matrices.

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MEA559

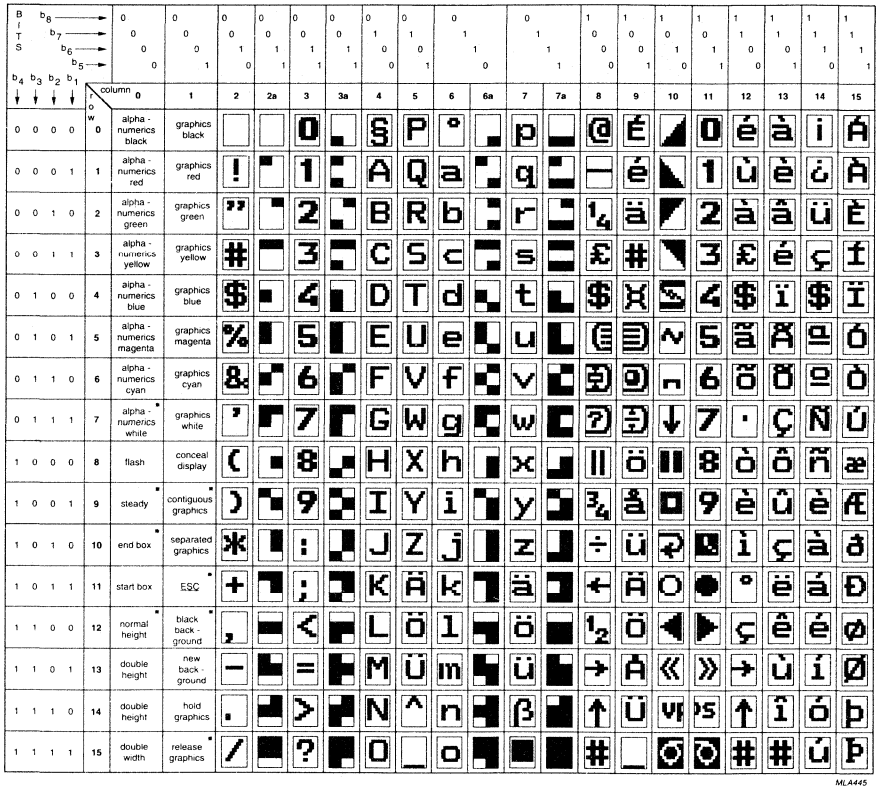
(1) PHCB are the Page Header Control Bits. Other combinations default to English.

Table 10 SAA5260 Western European basic character matrix



Where: NC = national option character position.

Table 11 SAA5260P/E character data input decoding (Western European Version)



For character version number (10000), see Register 16B.

* These control characters are presumed before each row begins.

Notes to Table 11

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Columns may be referred to by columns and row, for example 2/5 refers to %.
3. Black represents displayed colour. White represents background.
4. The SAA5260 national option characters are illustrated in Table 9.
5. Character 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters for combining with character 8/5.
6. With bit 8 = 0, national characters will be decoded according to the setting of control bits C12 to C14 (see Table 9).
7. Columns 2a, 3a, 6a and 7a are displayed in graphics mode.
8. Column 11 rows 0 to 7 are normally special attributes for setting the background colour. The numerals 0 to 7 are obtained instead when R0D3 is set to 1, to allow blast-through alphanumeric numbers in graphics mode.

Colour Facilities

Table 12 shows the format for both supplementary and normal page colour look-up tables (CLUTs). 12 bits are used for each colour entry. This allows the display colours to be chosen from a palette of 4096 different shades (16 levels possible on each of the R, G, B output pins from the internal DAC).

There are a total of 16 addresses in each CLUT, allowing each of the 8 foreground colour and 8 background colour values defined by the control characters to be assigned a particular shade, and separate colours to be assigned for normal and supplementary display pages.

On power-on, both CLUTs are cleared to full amplitude values corresponding to the R, G and B address inputs to give the normal 'level 1' display colours as shown in Table . They can then be re-defined by the microcomputer via the I²C-bus if required; registers R11 and R12 defining CLUT data and address, and R7D5 defining the CLUT to be used. R7D5 = 0 selects the CLUT for the normal page, while R7D5 = 1 selects the CLUT for the supplementary display page.

CLUT addressing and defaults

ADDRESS		MEANING	DEFAULT VALUE		
binary	decimal		R	G	B
0 0 0 0	0	BLACK background	0000	0000	0000
0 0 0 1	1	RED background	1111	0000	0000
0 0 1 0	2	GREEN background	0000	1111	0000
0 0 1 1	3	YELLOW background	1111	1111	0000
0 1 0 0	4	BLUE background	0000	0000	1111
0 1 0 1	5	MAGENTA background	1111	0000	1111
0 1 1 0	6	CYAN background	0000	1111	1111
0 1 1 1	7	WHITE background	1111	1111	1111
1 0 0 0	8	BLACK foreground	0000	0000	0000
1 0 0 1	9	RED foreground	1111	0000	0000
1 0 1 0	10	GREEN foreground	0000	1111	0000
1 0 1 1	11	YELLOW foreground	1111	1111	0000
1 1 0 0	12	BLUE foreground	0000	0000	1111
1 1 0 1	13	MAGENTA foreground	1111	0000	1111
1 1 1 0	14	CYAN foreground	0000	1111	1111
1 1 1 1	15	WHITE foreground	1111	1111	1111

Single chip teletext/VPS and line 23 decoder including 4/8 page memory

SAA5280

FEATURES

- Hardware compatible with SAA5246 and SAA5248
- Software compatible with SAA5248 and most applications of SAA5246
- Built-in 8 K memory for 4/8 page storage
- Meshing display within boxes
- Cursor decoupling from I²C-bus
- Automatic display of Packet X/24 from extension memory
- Separate data checking algorithms and points for each acquisition channel
- 24 : 18 Hamming checking
- Automatic Packet X/26 extension character processing
- VPS and Line 23 decoding and storage

GENERAL DESCRIPTION

The SAA5280 is hardware compatible with the SAA5246 and SAA5248 devices and may be used with existing boards and software. It contains 8K8 of on-chip memory allowing the device to be used as a single-chip teletext receiver. It also contains additional features (see features).

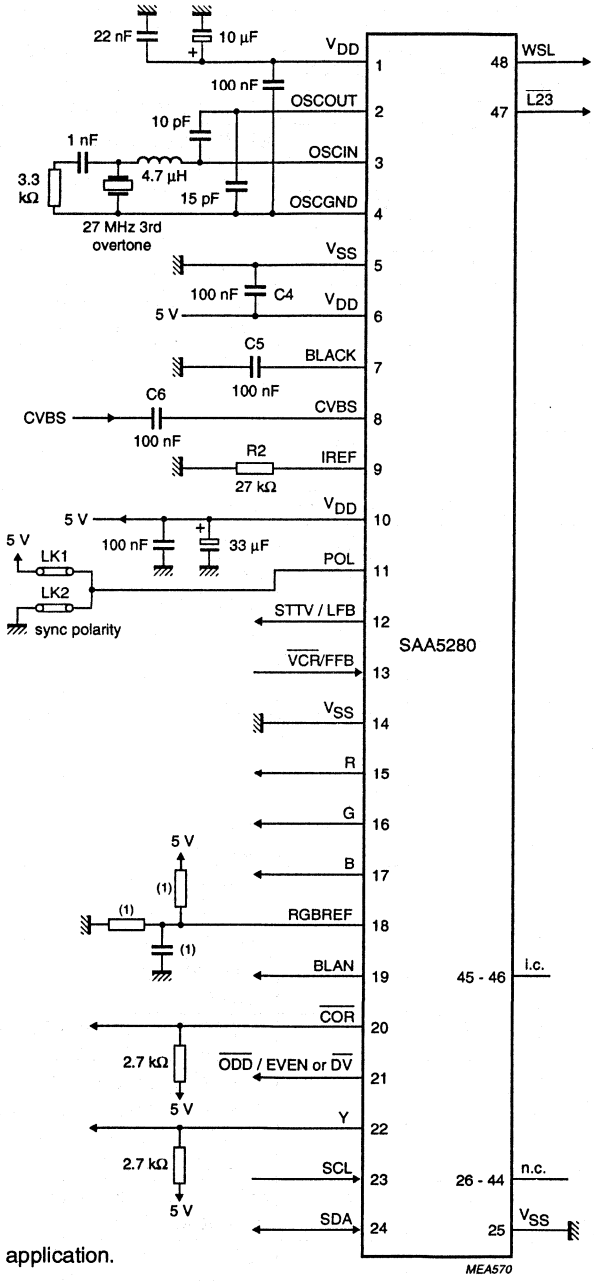
On power-up all new features remain transparent and no functional difference will be observed. To maintain software compatibility, the existing register map has been modified to include the extra device functions. These new features are controlled from two new registers, R12 and R12B.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5	5.5	V
I_{DD}	supply current	–	75	150	mA
V_{syn}	sync amplitude	0.1	0.3	0.6	V
V_{vid}	video amplitude	0.7	1	1.4	V
f_{xtal}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature	–20	–	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5280P/E	48	DIL	plastic	SOT240
SAA5280ZP/E	52	SDIL	plastic	SOT247
SAA5280GP/E	64	QFP	plastic	SOT208



(1) Value dependent upon application.

Fig.1 Application diagram.

PINNING

SYMBOL	PIN			DESCRIPTION
	SOT240	SOT247	SOT208	
OSCOUT	2	1	27	27 MHz crystal oscillator output
OSCIN	3	2	28	27 MHz crystal oscillator input
OSCGND	4	3	29	0 V crystal oscillator ground
V_{SS}	5, 14, 25	4, 5, 15, 26	30, 31, 43, 58, 26	0 V ground
n.c.	–	7	–	not connected
BLACK	7	8	35	video black level storage pin, connected to analog ground via a 27 kΩ resistor
CVBS	8	9	36	composite video input pin. A positive-going 1 V (peak-to-peak) input is required; connected via 100 nF capacitor
IREF	9	10	37	reference current input pin; connected to analog ground via a 27 kΩ resistor
V_{DD}	1, 10, 6	6, 11, 52	32, 38, 25	+5 V supply
POL	11	12	39	STTV/LFB/FFB polarity selection pin
STTV/LFB	12	13	40	sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode)
$\overline{VCR}$/FFB	13	14	42	PLL time constant switch/field input pin. Function controlled by an internal register bit (scan sync mode)
R	15	16	44	dot rate character output of the RED colour information
G	16	17	45	dot rate character output of the GREEN colour information
B	17	18	47	dot rate character output of the BLUE colour information
RGBREF	18	19	48	input DC voltage to define the output high level on the RGB pins
BLAN	19	20	52	dot rate fast blanking output
$\overline{COR}$	20	21	53	programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages. Open drain output
$\overline{ODD}$/EVEN or $\overline{DV}$	21	22	54	in $\overline{ODD}$/EVEN mode a 25 Hz output synchronized to the input CVBS field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents. In $\overline{DV}$ mode a VPT data valid signal used to indicate reception of error-free VPS or 8/30/format 2 data
Y	22	23	55	dot rate character output of teletext foreground colour information. Open drain output
SCL	23	24	56	serial clock input for I²C-bus. It can still be driven HIGH during device power-down
SDA	24	25	57	serial data port for the I²C-bus. Open drain output. It can still be driven HIGH during device power-down

SYMBOL	PIN			DESCRIPTION
	SOT240	SOT247	SOT208	
SDA	24	25	57	serial data port for the I²C-bus. Open drain output. It can still be driven HIGH during device power-down
n.c.	26-44	27-47	1-20, 34, 41, 46, 49-51	not connected
i.c.	45, 46	48, 49	21, 22	internally connected; normally connected to ground
WSL	48	51	24	Line 23 decoder output "wide screen letterbox"
$\overline{L23}$	47	50	23	interrupt on detection of Line 23 signalling bits "wide screen"

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

REGISTER MAP

SAA5280 mode registers R0 to R12B are shown below. R0 to R10 and R12 are WRITE only; R11 is READ/WRITE.

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
Adv. control	0	X24 POS	FREE RUN PLL	AUTO $\overline{\text{ODD}}$/ EVEN	DISABLE HDR ROLL	$\overline{\text{R12}}$/R12B	DISABLE $\overline{\text{ODD}}$/ EVEN	VCR MODE	$\overline{\text{R11}}$/R11B
Mode	1	VCS TO SCS	$\overline{7+P}$/ 8-BIT	ACQ $\overline{\text{ON}}$/OFF	EXT. PACKET ENABLE	$\overline{\text{DEW}}$/ FULL FIELD	TCS ON	T1	T0
Page request address	2	HAM. CHECK 27, 28, 8/30	BANK SELECT A2	ACQ CIRCUIT A1	ACQ CIRCUIT A0	MESH $\overline{\text{OFF}}$/ON	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request data	3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
Display chapter	4	–	–	–	–	–	A2	A1	A0
Display control (normal)	5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash /subtitle)	6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	7	STATUS TOP	CURSOR ON	REVEAL ON	BOTTOM HALF	DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0
Active chapter	8	–	–	–	VPS ENABLE	CLEAR MEM.	A2	A1	A0
Cursor row	9	–	–	–	R4	R3	R2	R1	R0
Cursor column	10	–	–	C5	C4	C3	C2	C1	C0
Cursor data	11	D7	D6	D5	D4	D3	D2	D1	D0
Device status	11B	$\overline{625}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	DATA QUALITY	VCS SIGNAL QUALITY
Advanced Control 2A	12	H3	H2	H1	H0	S3	S2	S1	S0
Advanced Control 2B	12B	–	WSL LEVEL	WSL OVERRIDE	L23 ENABLE	VPS ENABLE	HAM CHECK X/26	PROCESS PK X/26	DISPLAY PK X26

EUROM 50 Hz

GENERAL DESCRIPTION

The SAA5351 EUROM is a single-chip VLSI NMOS crt controller capable of handling all display functions required by the CEPT videotex terminal, model A4. Only minimal hardware is required to produce a videotex terminal using EUROM – the simplest configuration needs just a microcontroller and 4 Kbytes of display memory.

Features

- Minimal additional hardware required
- Screen formats of 40/80 character by 1-to-25 row display
- 512 alphanumeric or graphical characters on-chip or extendable off-chip
- Serial attribute storage (STACK) and parallel attribute storage
- Dynamically redefinable character (DRCS) capability over full field
- Interfaces with 8/16-bit microprocessors with optional direct memory access
- On-chip scroll map minimizes data to be transferred when scrolling
- On-chip colour map RAM (4096 locations) and three on-chip digital-to-analogue converters allow 32 colours on-screen
- On-chip digital-to-analogue converters are non-linear to compensate for crt non-linearity
- Memory interface capable of supporting multi-page terminals. EUROM can access up to 128 Kbytes of display memory
- Programmable cursor
- Programmable local status row
- Three synchronization modes:

stand-alone	built-in oscillator operating with an external 6 MHz crystal
simple slave	directly synchronized from the source of text composite sync
phase-locked slave	indirect synchronization allows picture-in-text displays (e.g. VCR/VLP video with text overlay)

- On-chip timing composite sync output
- Zoom feature which allows the height of any group of rows to be increased to enhance legibility

PACKAGE OUTLINE

40-lead DIL; plastic (SOT129).

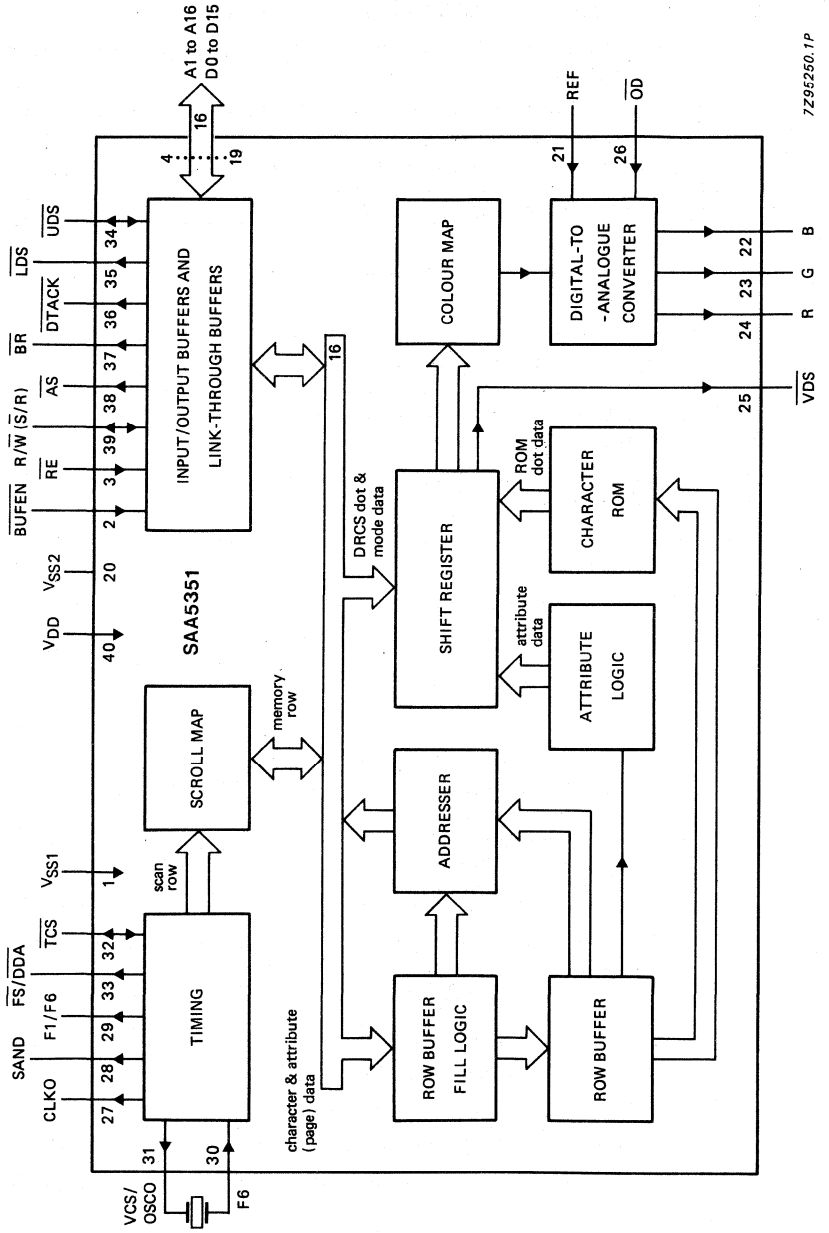


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

1	V_{SS1}	Ground 0 V.
2	$\overline{BUFEN}$	Buffer enable input to the 8-bit link-through buffer.
3	$\overline{RE}$	Register enable input. This enables A1 to A6 and $\overline{UDS}$ as inputs, and D8 to D15 as input/outputs.
4 to 19	A16 to A1/ D15 to D0	Multiplexed address and data bus input/outputs. These pins also function as the 8-bit link-through buffer.
20	V_{SS2}	Ground (0 V).
21	REF	Analogue reference input.
22	B	Analogue outputs (signals are gamma-corrected).
23	G	
24	R	
25	$\overline{VDS}$	Switching output for dot, screen (row), box and window video data; for use when video signal is present (e.g. from tv, VLP, alpha + photographic layer). This output is LOW for tv display and HIGH for text and will interface directly with a number of colour decoder ICs (e.g. TDA3560, TDA3505).
26	$\overline{OD}$	Output disable causing R, G, B and $\overline{VDS}$ outputs to go to high-impedance state. Can be used at dot-rate.
27	CLKO	12 MHz clock output for hard-copy dot synchronization (referenced to output dots).
28	SAND	Sandcastle feedback output for SAA5230 teletext video processor or other circuit. Used when the display must be locked to the video source (e.g. VLP). The phase-lock part of the sandcastle waveform can be disabled to allow free-running of the SAA5230 phase-locked loop.
29	F1/F6	1 MHz or 6 MHz output.
30	F6	6 MHz clock input (e.g. from SAA5230). Internal a.c. coupling is provided.
31	VCS/OSCO	Video composite sync input (e.g. from SAA5230) for phase reference of vertical display timing when locking to a video source (e.g. VLP) or, in stand-alone sync mode, output from internal oscillator circuit (fixed frequency).
32	$\overline{TCS}$	Text composite sync input/output depending on master/slave status.
33	$\overline{FS}/\overline{DDA}$	Field sync pulse output or defined-display-area flag output (both referenced to output dots).
34	$\overline{UDS}$	Upper data strobe input/output.
35	$\overline{LDS}$	Lower data strobe output.
36	$\overline{DTACK}$	Data transfer acknowledge (open drain output).
37	$\overline{BR}$	Bus request to microprocessor (open drain output).
38	$\overline{AS}$	Address strobe output to external address latches.
39	R/$\overline{W}$ ($\overline{S}$/R)	Read/write input/output. Also serves as send/receive for the link-through buffer.
40	V_{DD}	Positive supply voltage (+5 V).

PINNING (continued)

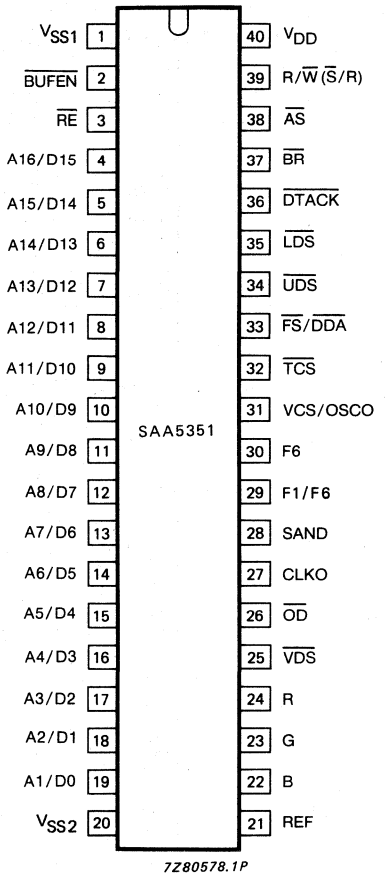


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 40)	V_{DD}	−0,3 to + 7,5 V
Maximum input voltage (except F6, $\overline{TCS}$, REF)	V_{Imax}	−0,3 to + 7,5 V
Maximum input voltage (F6, $\overline{TCS}$)	V_{Imax}	−0,3 to + 10,0 V
Maximum input voltage (REF)	V_{REF}	−0,3 to + 3,0 V
Maximum output voltage	V_{Omax}	−0,3 to + 7,5 V
Maximum output current	I_{Omax}	10 mA
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

Outputs other than CLKO, OSCO, R, G, B, and $\overline{VDS}$ are short-circuit protected.

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 5 V ± 5%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 40)	V_{DD}	4,75	5,0	5,25	V
Supply current (pin 40)	I_{DD}	–	–	390	mA
INPUTS					
F6					
Slave modes (Fig. 3)					
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	1,0	2,0	7,0	V
Input leakage current at V_I = 0 to $V_{CC\,max}$; T_{amb} = 25 °C	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	12	pF
Stand-alone mode (Fig. 4)					
Series capacitance of crystal	C_1	–	28	–	fF
Parallel capacitance of crystal	C_0	–	7,1	–	pF
Resonance resistance of crystal	R_r	–	–	60	Ω
$\overline{\text{BUFEN}}$, $\overline{\text{RE}}$, $\overline{\text{OD}}$					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,5	V
Input leakage current at V_I = 0 to V_{DD}+ 0,3 V; T_{amb} = 25 °C	I_{IL}	−10	–	+ 10	μA
Input capacitance	C_I	–	–	7	pF
REF (Fig. 5)					
Input voltage	V_{REF}	0	1 to 2	2,7	V
Resistance (pin 21 to pin 20) with REF supply and R, G, B outputs OFF	R_{REF}	–	125	–	Ω

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
OUTPUTS					
SAND					
Output voltage high level at I_O = 0 to −10 μA	V_{OH}	4,2	–	V_{DD}	V
Output voltage intermediate level at I_O = −10 to + 10 μA	V_{OI}	1,3	2,0	2,7	V
Output voltage low level at I_O = 0,2 mA	V_{OL}	0	–	0,2	V
Load capacitance (note 1)	C_L	–	–	130	pF
F1/F6, $\overline{DDA}$/$\overline{FS}$					
Output voltage HIGH	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance (note 1)	C_L	–	–	50	pF
$\overline{LDS}$, $\overline{AS}$					
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2,0	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,8	V
Load capacitance (note 1)	C_L	–	–	200	pF
$\overline{DTACK}$, $\overline{BR}$ (open drain outputs)					
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance (note 1)	C_L	–	–	150	pF
Capacitance (OFF state)	C_{OFF}	–	–	7	pF
R, G, B (note 2)					
Output voltage HIGH (note 3) at I_{OH} = −100 μA; V_{REF} = 2,7 V	V_{OH}	2,4	–	–	V
Output voltage LOW at I_{OL} = 2 mA (note 10)	V_{OL}	–	–	0,4	V
Output resistance during line blanking	R_{OBL}	–	–	150	Ω
Output capacitance (OFF state)	C_{OFF}	–	–	12	pF
Output leakage current (OFF state) at V_I = 0 to V_{DD}+0,3 V; T_{amb} = 25 °C	I_{OFF}	−10	–	+ 10	μA
CLOCKO					
Output voltage HIGH	V_{OH}	2,0		V_{DD}	V
Output voltage LOW	V_{OL}	0		0,8	V
Load capacitance (note 1)	C_L	–		50	pF

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
$\overline{VDS}$					
Output voltage HIGH	V_{OH}	2,0	–	V_{DD}	V
Output voltage LOW	V_{OL}	0	–	0,8	V
Output leakage current (OFF state) at V_I = 0 to V_{DD} + 0,3 V; T_{amb} = 25 °C	I_{LO}	−10	–	+ 10	μA
INPUTS/OUTPUTS					
VCS/OSCO					
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Output leakage current (output OFF) at V_I = 0 to V_{DD} + 0,3 V; T_{amb} = 25 °C	I_{LO}	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Load capacitance (note 1)	C_L	–	–	50	pF
$\overline{TCS}$					
Input voltage HIGH	V_{IH}	3,5	–	10,5	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Output leakage current at V_I = 0 to V_{DD} + 0,3 V; T_{amb} = 25 °C	I_{LO}	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at I_{OH} = −200 to 100 μA	V_{OH}	2,0	–	6,0	V
Output voltage LOW at V_{OL} = 3,2 mA	V_{OL}	0	–	0,8	V
Load capacitance (note 1)	C_L	–	–	50	pF
A1/D0 to A16/D15					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Output leakage current V_I = 0 to V_{DD} + 0,3 V; T_{amb} = 25 °C	I_{LO}	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance (note 1)	C_L	–	–	200	pF
$\overline{UDS}$; R/$\overline{W}$					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Output leakage current at V_I = 0 to V_{DD} + 0,3 V; T_{amb} = 25 °C	I_{LO}	−10	–	+ 10	μA
Input capacitance	C_{IN}	–	–	10	pF
Output voltage HIGH (I_{OH} = −200 μA)	V_{OH}	2,0	–	V_{DD}	V
Output voltage LOW (I_{OH} = 3,2 mA)	V_{OL}	0	–	0,8	V
Load capacitance (note 1)	C_L	–	–	200	pF

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TIMING					
Values guaranteed at 0,8 V and 2,0 V levels F6 input frequency at 6 MHz					
F6 (Fig. 3)					
Rise and fall times	t_r, t_f	10	–	80	ns
Frequency	f_{F6}	5,9	–	6,1	MHz
CLKO, F1/F6, R, G, B, $\overline{\text{VDS}}$, $\overline{\text{FS}}$/$\overline{\text{DDA}}$, $\overline{\text{OD}}$ (notes 4, 5 and Fig. 6)					
CLKO HIGH time	t_{CLKH}	25	–	–	ns
CLKO LOW time	t_{CLKL}	15	–	–	ns
CLKO rise and fall times	t_{CLKr} t_{CLKf}	–	–	10	ns
CLKO HIGH to R, G, B, $\overline{\text{VDS}}$ floating after $\overline{\text{OD}}$ fall	t_{FOD}	0	–	30	ns
Skew between outputs R, G, B, $\overline{\text{VDS}}$	t_{VS}	–	–	20	ns
R, G, B, $\overline{\text{VDS}}$ rise and fall times	t_{Vr}, t_{Vf}	–	–	30	ns
CLKO HIGH to R, G, B, $\overline{\text{VDS}}$ active after $\overline{\text{OD}}$ rise	t_{AOD}	0	–	60	ns
F1 HIGH time (note 5)	t_{F1H}	400	500	580	ns
F1 LOW time (note 5)	t_{F1L}	400	500	580	ns
F6 HIGH time	t_{F6H}	40	83	120	ns
F6 LOW time	t_{F6L}	40	83	120	ns
$\overline{\text{OD}}$ to CLKO rise set-up	t_{ODS}	–	–	45	ns
$\overline{\text{OD}}$ to CLKO HIGH hold	t_{ODH}	–	–	0	ns
MEMORY ACCESS TIMING (notes 1, 6, 7 and Fig. 7)					
$\overline{\text{UDS}}$, $\overline{\text{LDS}}$, $\overline{\text{AS}}$					
Cycle time	t_{cyc}	–	500	–	ns
$\overline{\text{UDS}}$ HIGH to bus-active for address output	t_{SAA}	75	–	–	ns
Address valid set-up to $\overline{\text{AS}}$ fall	t_{ASU}	20	–	–	ns
Address valid hold from $\overline{\text{AS}}$ LOW	t_{ASH}	20	–	–	ns
Address float to $\overline{\text{UDS}}$ fall	t_{AFS}	0	–	–	ns

parameter	symbol	min.	typ.	max.	unit
$\overline{AS}$ LOW to $\overline{UDS}$ fall delay	t_{ATD}	50	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ HIGH time	t_{HDS}	220	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ LOW time (note 9)	t_{LDS}	200	–	–	ns
$\overline{AS}$ HIGH time	t_{HAS}	125	–	–	ns
$\overline{AS}$ LOW time	t_{LAS}	290	–	–	ns
$\overline{AS}$ LOW to $\overline{UDS}$ HIGH	t_{AUH}	280	–	–	ns
Data valid set-up to $\overline{UDS}$ rise	t_{DSU}	30	–	–	ns
Data valid hold from $\overline{UDS}$ HIGH	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{AS}$ rise delay	t_{UAS}	0	–	15	ns
$\overline{AS}$ LOW to data valid	t_{AFA}	–	–	270	ns
Link-through buffers (notes 6, 7 and Fig. 8)					
$\overline{BUFEN}$ LOW to output valid	t_{BEA}	–	–	100	ns
Link-through delay time	t_{LTD}	–	–	85	ns
Input data float prior to direction change	t_{IFR}	0	–	–	ns
Output float after direction change	t_{OFR}	–	–	60	ns
Output float after $\overline{BUFEN}$ HIGH	t_{BED}	–	–	60	ns
Microprocessor READ from EUROM (Fig. 9)					
R/$\overline{W}$ HIGH set-up to $\overline{UDS}$ fall	t_{RUD}	0	–	–	ns
$\overline{UDS}$ LOW to returned-data access time	t_{UDA}	–	–	210	ns
$\overline{RE}$ LOW to returned data access time	t_{REA}	–	–	210	ns
Data valid to $\overline{DTACK}$ LOW delay	t_{DTL}	40	–	–	ns
$\overline{DTACK}$ LOW to $\overline{UDS}$ rise	t_{DLU}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	75	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	10	–	–	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ fall	t_{UDR}	0	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DSD}	250	–	350	ns
Address valid to $\overline{UDS}$ fall	t_{AUL}	0	–	–	ns

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
MEMORY ACCESS TIMING (continued)					
Microprocessor WRITE to EUROM (Fig. 10)					
Write cycle time (note 8)	t_{WCY}	500	–	–	ns
R/$\overline{W}$ LOW set-up to $\overline{UDS}$ fall	t_{WUD}	0	–	–	ns
$\overline{RE}$ LOW to $\overline{UDS}$ fall	t_{RES}	30	–	–	ns
Address valid to $\overline{UDS}$ fall	t_{ASS}	30	–	–	ns
$\overline{UDS}$ LOW time	t_{LUS}	100	–	–	ns
Data valid to $\overline{UDS}$ rise	t_{DSS}	80	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DTA}	0	–	60	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	75	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ rise	t_{UDW}	0	–	–	ns
F1/F6 to memory access cycle (Fig. 11)					
$\overline{UDS}$ HIGH to F6 (component of F1/F6) rise (notes 1, 6 and 7)	t_{UF6}	20	–	–	ns
F6 (component of F1/F6) HIGH to $\overline{UDS}$ rise	t_{F6U}	40	–	–	ns
SYNCHRONIZATION and BLANKING					
$\overline{TCS}$, SAND, $\overline{FS}$/$\overline{DDA}$					
See Fig. 12 for timing relationships and Fig. 13 for vertical sync and blanking waveforms.					

Notes to the characteristics

1. All pins are tested with a 150 pF load capacitor.
2. 16-level analogue voltage outputs.
3. Output voltage guaranteed when programmed for top level.
4. CLKO, F1/F6, $\overline{VDS}$, $\overline{FS}$/$\overline{DDA}$: reference levels = 0,8 to 2,0 V.
   R, G, B: reference levels = 0,8 to 2,0 V with V_{REF} = 2,7 V.
5. These times may momentarily be reduced to a nominal 83 ns in slave-sync mode at the moment of re-synchronization.
6. Reference levels = 0,8 to 2,0 V.
7. F6 input at 6 MHz.
8. Microprocessor write cycle times of less than 500 ns are permitted but often result in Wait States being generated, the precise timing of $\overline{DTACK}$ will then depend on the internal synchronization time.
9. This timing may be infringed at the beginning and end of the memory access window.
10. Output voltage guaranteed when programmed for bottom level.

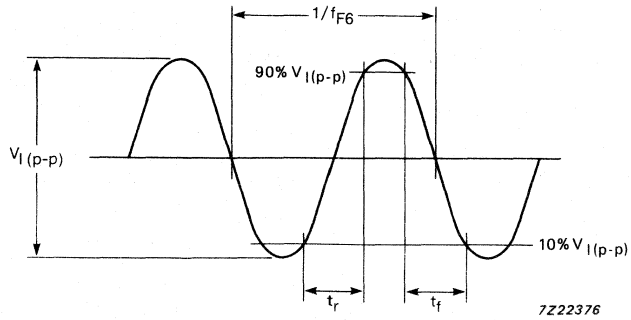
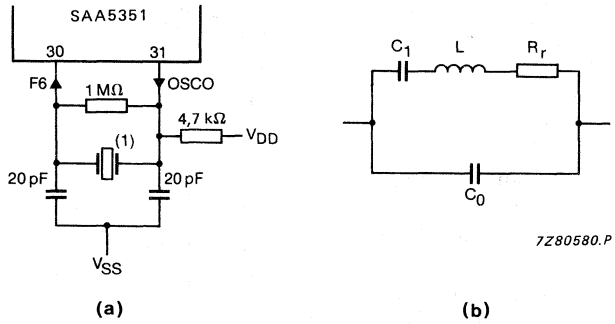


Fig. 3 F6 input waveform.

DEVELOPMENT DATA



(1) Catalogue number of crystal: 4322 143 04101

Fig. 4(a) Oscillator circuit for SAA5351 stand-alone sync mode and (b) equivalent circuit of crystal at resonance (see **characteristics** for values).

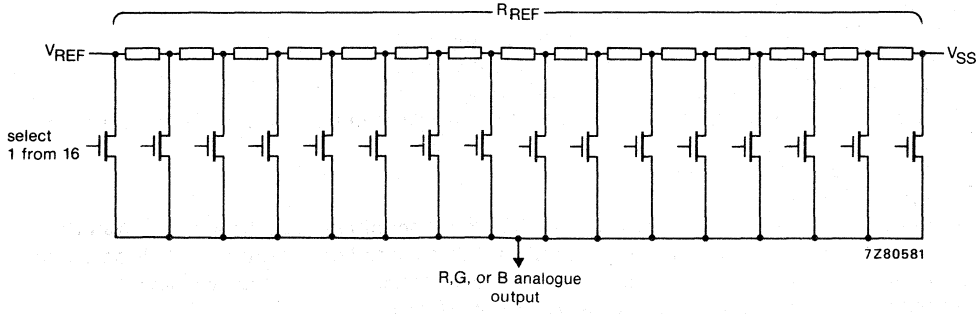


Fig. 5 Circuit arrangement giving one-of-sixteen reference voltage levels for the R, G or B analogue outputs.

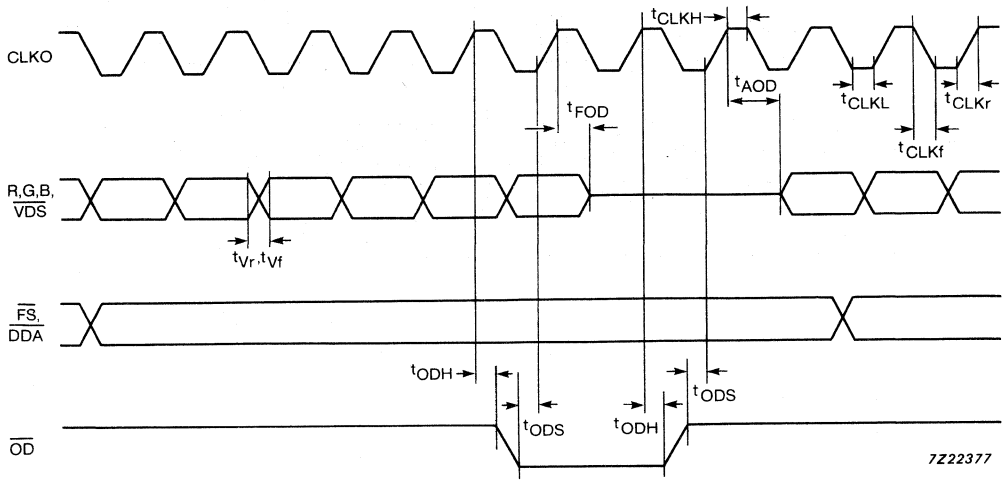


Fig. 6 Video timing.

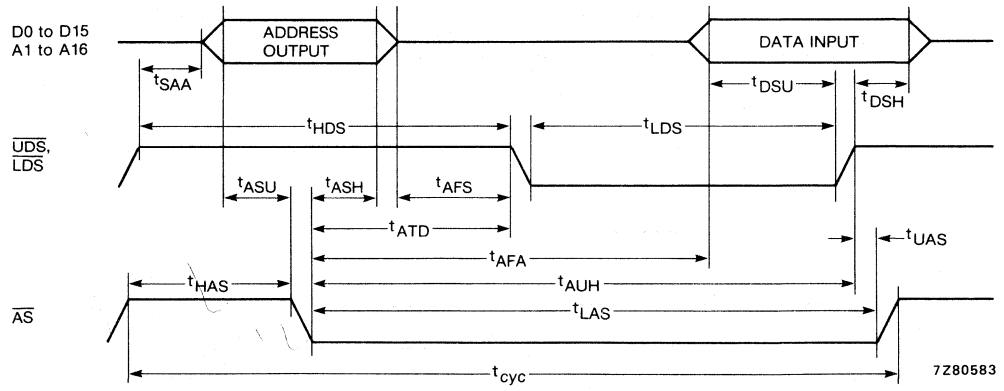


Fig. 7 Memory access timing.

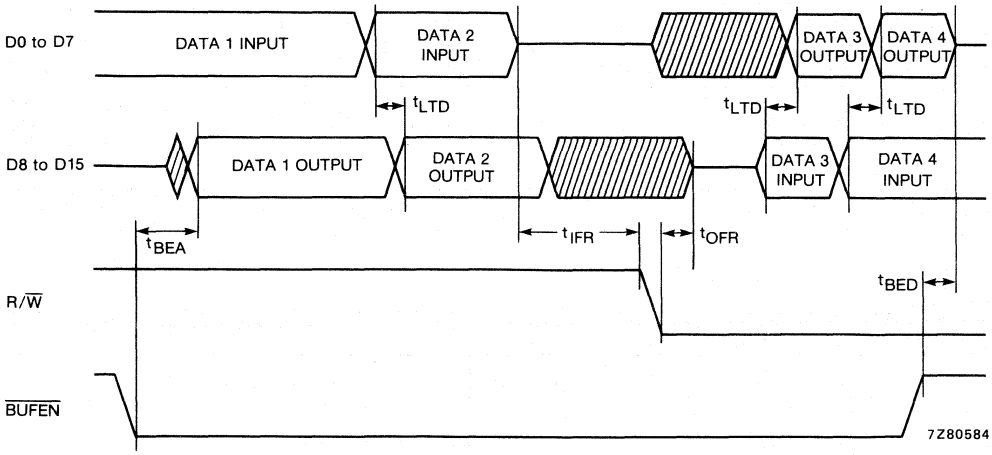


Fig. 8 Timing of link-through buffers.

DEVELOPMENT DATA

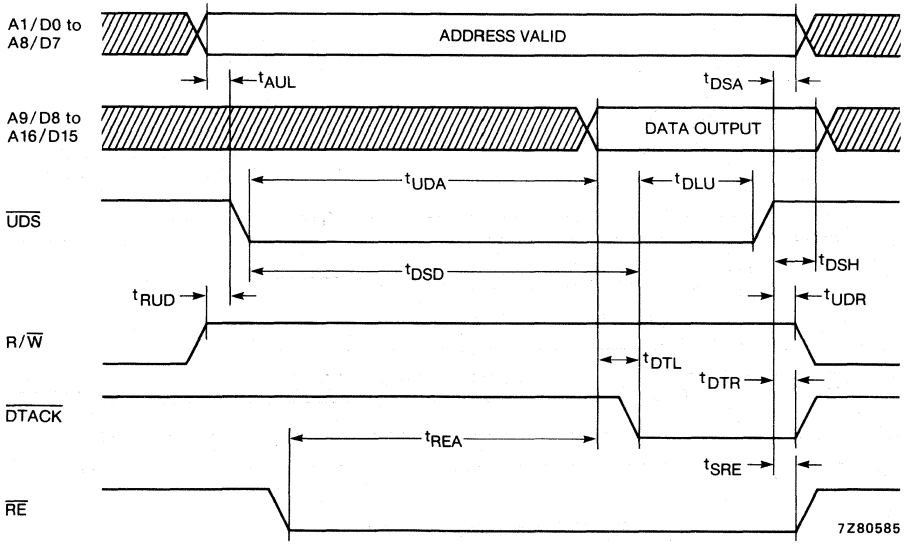


Fig. 9 Timing of microprocessor read from EUROM.

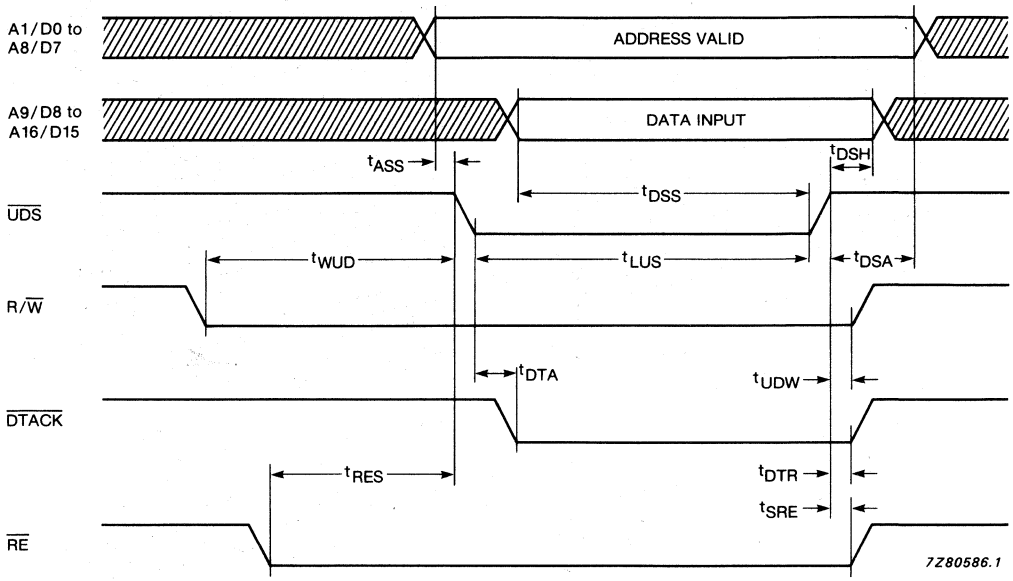


Fig. 10 Timing of microprocessor write to EUROM.

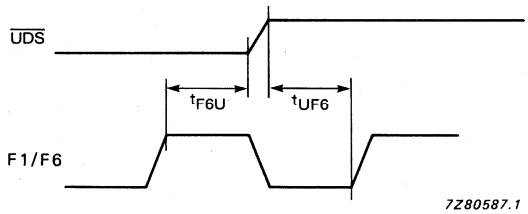


Fig. 11 Timing of F1/F6 to memory access cycle.

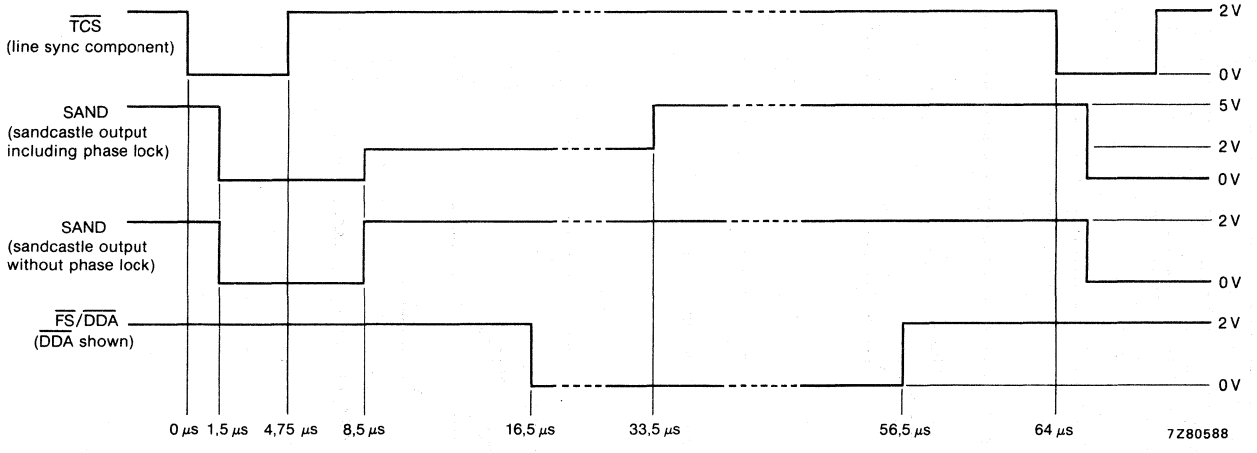


Fig. 12 Timing of synchronization and blanking outputs; all timings are nominal and assume f_{F6} = 6 MHz.

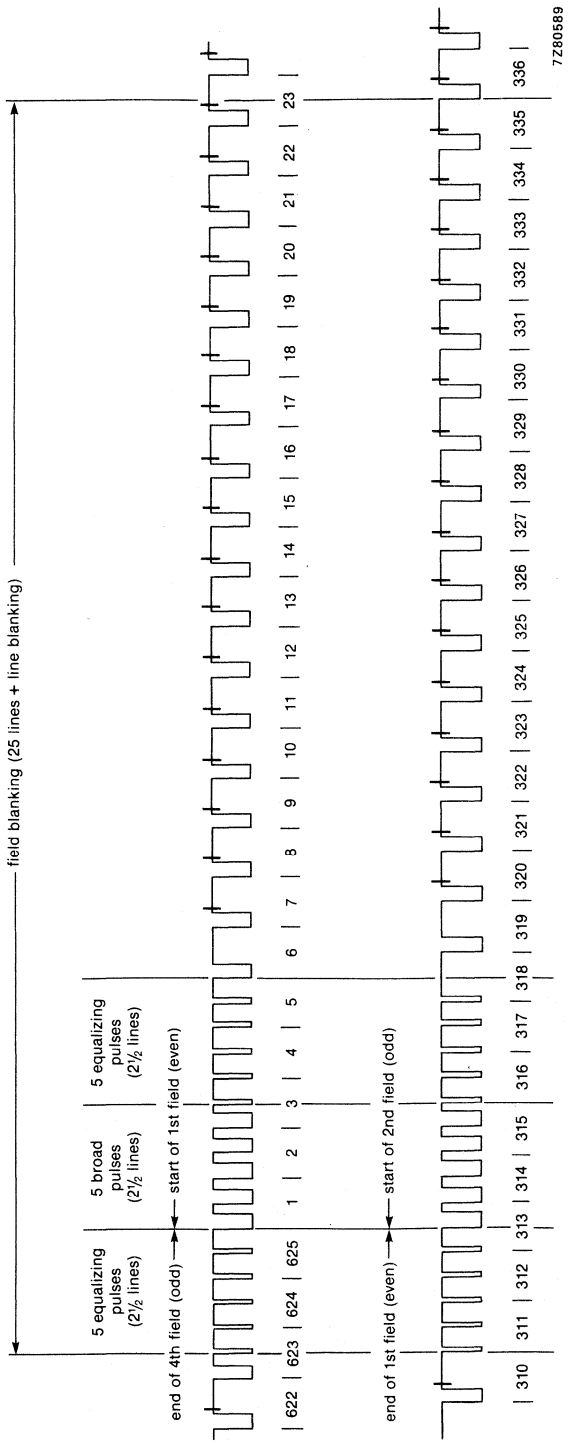


Fig. 13 Vertical synchronization and blanking waveforms; separation of broad pulses = 4,75 μs; equalizing pulse widths = 2,25 μs.

APPLICATION INFORMATION

More detailed application information is available on request

BASIC VIDEOTEX DECODER CONFIGURATION

A basic, practical decoder configuration is shown in Fig. 14, reference should also be made to the block diagram Fig. 1.

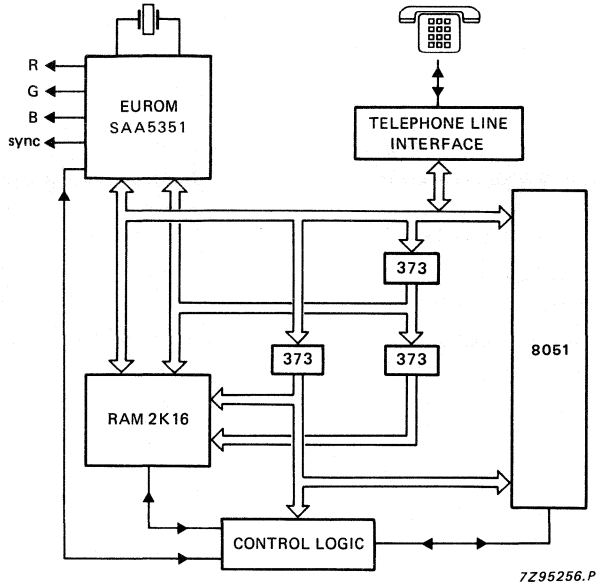


Fig. 14 Basic videotex decoder configuration.

Character and attribute data is fetched from the external memory, processed by the row buffer fill logic according to the stack coding scheme (in stack mode) and then fed into one half of the dual display row buffer. The data fetch process takes place during one line-flyback period (per row) and, since time is required to complete the fill, the other half of the dual row buffer is used for display. The row buffers exchange functions on alternate rows – each holds the 40 columns of 32 bits required to define explicitly every character in a row.

The addresser is used for row buffer filling and for fetching screen colours, and during the display time it is also used for addressing DRCS characters.

Timing

The timing chain operates from an external 6 MHz clock or an on-chip fixed-frequency crystal oscillator. The basic video format is 40 characters per row, 24/25 rows per page and 10 video lines per row. EUROM will also operate with 20/21 rows per page and 12 video lines per row. The two extra lines per row are added symmetrically and contain background colour only for ROM-based alpha-numeric characters. DRCS characters, block and smooth mosaics and line drawing characters occupy all 12 lines.

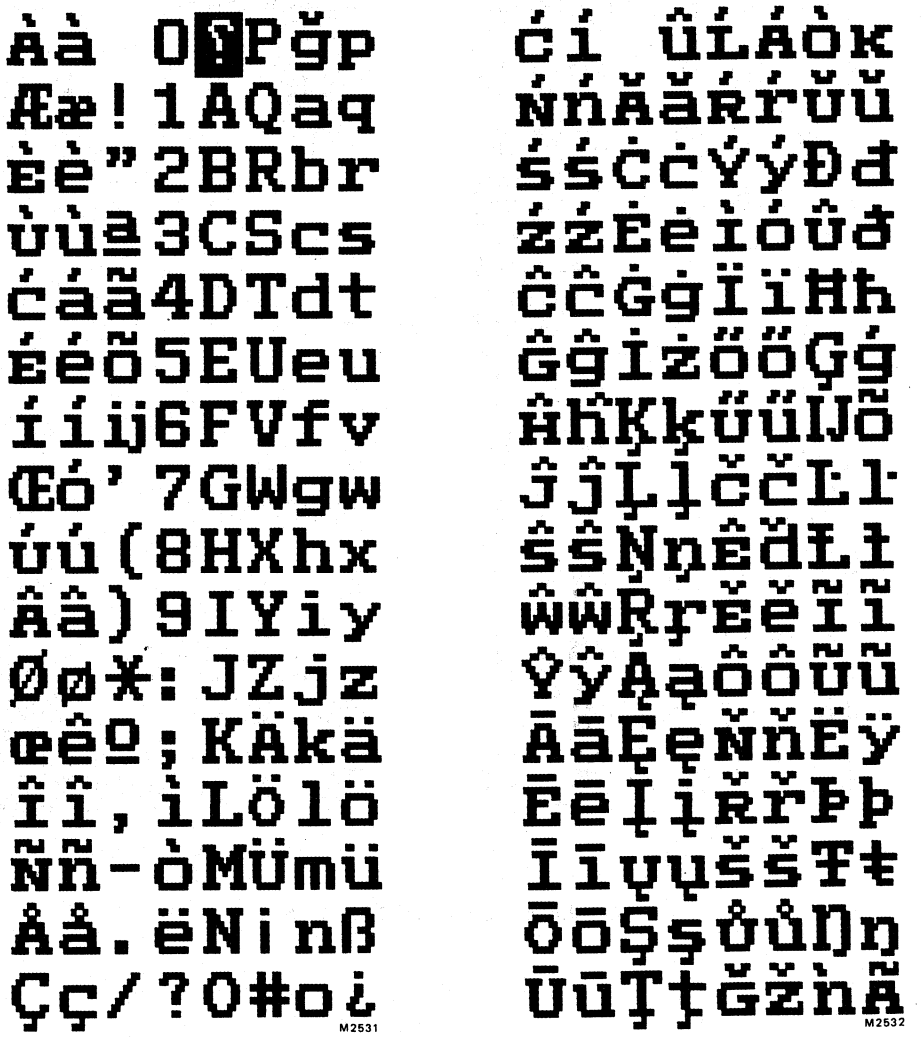
The display is generated to the normal 625-line/50 Hz scanning standard (interlaced or non-interlaced). In addition to composite sync (pin 32) for conventional timebases, a clock output at 1 MHz or 6 MHz (pin 29) is available for driving other videotex devices, and a 12 MHz clock (pin 27) is available for hard-copy dot synchronization. A defined-display-area timing signal (pin 33) simplifies the application of external peripherals such as a light pen; this signal is nominally coincident with the character dot information.

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

Character generation

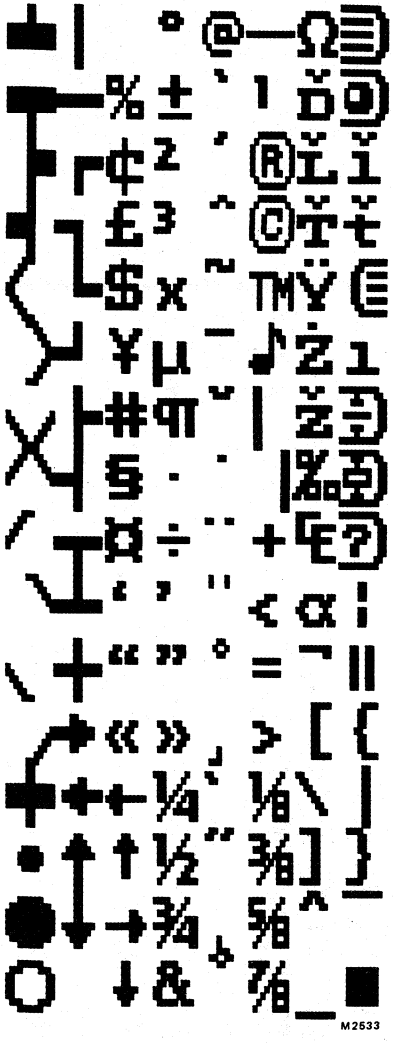
EUROM supports eight character tables, each of (nominally) 128 characters. Four tables are in on-chip ROM and contain fixed characters and four are stored in an external RAM. The contents of the fixed character tables (Tables 0 to 3) are shown in Figs 15 and 16.



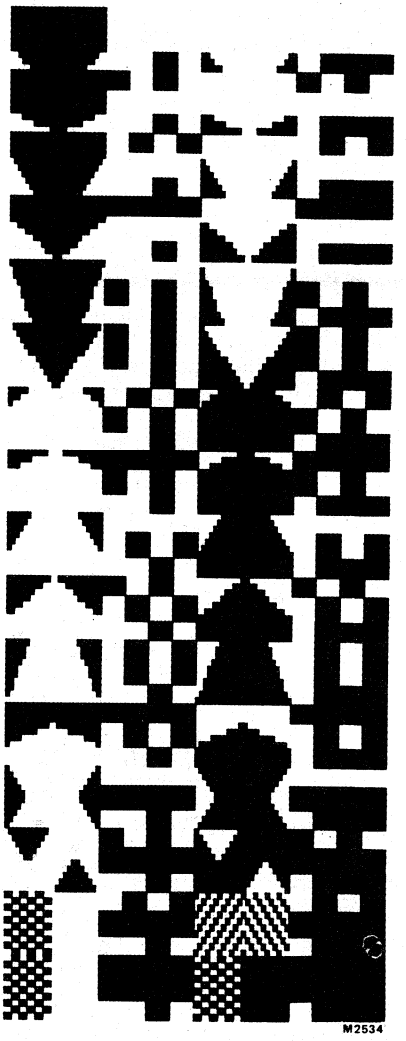
(a) (b)

Fig. 15 On-chip characters: (a) Table 0; (b) Table 1.

DEVELOPMENT DATA



(a)



(b)

Fig. 16 On-chip characters: (a) Table 2; (b) Table 3.

APPLICATION INFORMATION (continued)

Character generation (continued)

The 128 most commonly used characters are contained in Table 0, these are the standard upper and lower-case letters of the Roman alphabet, numerals, punctuation and the more common accented characters. In normal text transmission, Table 0 is used most of the time. Table 1 contains other accented characters. Miscellaneous characters, mathematical symbols, the line drawing character set and accents without associated symbols are contained in Table 2. Table 3 contains the block mosaics for the basic alpha-mosaic service and also the new smooth mosaics.

The four tables stored in the external RAM (Tables 4 to 7) are used for DRCS.

Scroll map

The scroll map uses a 26-byte area of on-chip RAM and functions in association with the timing chain. It maps the scan row on to the fetched memory row so allowing the stored page to be displayed in any row order. For each row, a 1-byte pointer to the display memory row is stored in the scroll map. This allows scrolling without the need for data transfer to, or from, side storage.
Additional control bits are stored, allowing 1 to 25 rows to be displayed at any location on the screen.

Colour map and digital-to-analogue converters

The colour map RAM contains thirty-two 12-bit words that are loaded by the microprocessor and read out in three 4-bit groups at pixel rate. Each group is fed to a non-linear (gamma-corrected) D-A converter. The resulting R, G and B outputs are low-impedance with peak-to-peak amplitudes controlled by the reference voltage applied at pin 21.

Cursor

The cursor is available in the stack mode. Its position, character code, character table, foreground colour, background colour, lining and flash attributes are all software programmable via internal register bits.

NON-VIDEOTEX APPLICATIONS

For non-Videotex applications, the device will also support the following operating modes:

Explicit fill mode. An alternative 40 character/rows mode which does not use the memory compression technique of stack coding. More display memory is required but there are no limitations on the number of display attribute changes per row.

80 characters/rows mode. When operating with 80 characters per row, the available display attributes are eight foreground colours, eight (potentially different) background colours (including transparent) as well as underline and blink.

Full field DRCS mode. This mode is not mutually exclusive to the explicit fill and 80 characters/rows modes but rather the available DRCS memory is expanded so that the whole screen can be covered, thus enabling a 'bit map'. All ROM-based characters and all display attributes remain available.

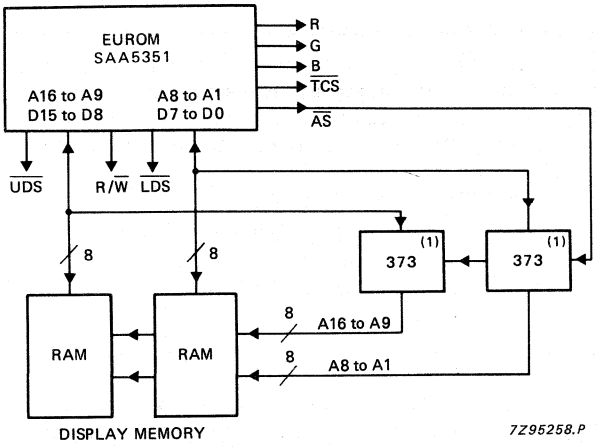
MICROPROCESSOR and RAM BUS INTERFACE

Three types of data transfer take place at the bus interface:

- EUROM fetches data from the display memory
- The microprocessor reads from, or writes to, EUROM's internal register map
- The microprocessor accesses the display memory

EUROM access to display memory (Figs 17 and 18)

EUROM accesses the external display memory via a 16-bit multiplexed address and data bus with a cycle time of 500 ns. The address strobe ($\overline{AS}$) signal from EUROM flags the bus cycle and writes the address into octal latches (74LS373). The display data is stored in bytes of upper (most-significant) and lower (least-significant) display information and is always fetched in pairs of bytes (upper + lower = 16 bits). The upper and lower display RAM sections are enabled simultaneously by the upper and lower data strobes (respectively $\overline{UDS}$ and $\overline{LDS}$) which are always asserted together to fetch a 16-bit word. The read/write control R/$\overline{W}$ is included although EUROM only reads from the display memory.



(1) 74LS373 octal transparent latch (3-state)

Fig. 17 Simple RAM interface circuit for display memory access.

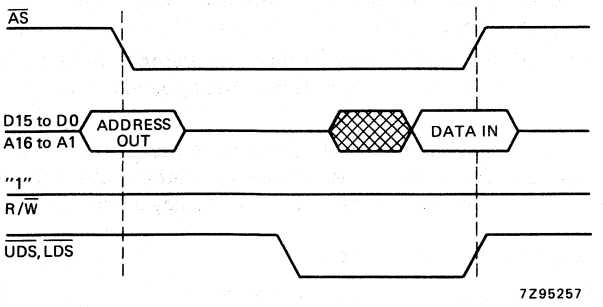


Fig. 18 Bus timing for display memory access.

APPLICATION INFORMATION (continued)

EUROM access to display memory (continued)

The display memory organization uses the word/byte addressing convention adopted for the SCN68000 microprocessor series. Data fetched on the 16-bit bus is considered in terms of bytes where the even numbered bytes use the upper (most-significant) part of the bus as shown in Fig. 19. The word addresses are numerically the same as the upper byte that they contain — there are no odd-numbered word addresses.

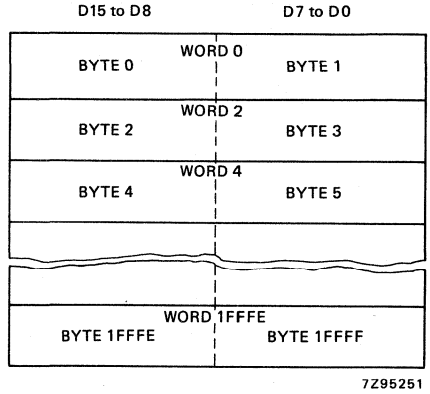


Fig. 19 Display memory word/byte organization.

Warning time

As EUROM is a real-time display device, it must have direct access to the display memory with priority over the microprocessor and other peripheral devices. This is achieved by EUROM issuing a bus request ($\overline{BR}$) signal for the duration of the memory access plus a programmable advance warning time which allows the microprocessor to complete its current bus cycle.

In systems where the buses of the microprocessor and EUROM are intimately connected (connected systems), $\overline{BR}$ may be used to suspend all microprocessor activity so that EUROM can act as a dedicated DMA controller. In systems where the two buses are separated by buffers (disconnected systems), $\overline{BR}$ may be used either to generate an interrupt or as a direct signal. To these ends, the warning time between the assertion of $\overline{BR}$ and the beginning of EUROM's bus activity is programmable to be between 0 and 23 μs.

Microprocessor access to register map

EUROM has a set of internal registers which, when memory-mapped, behave as an 8-bit wide RAM connected to the upper part of the data bus (Fig. 20). The control signals $\overline{UDS}$ and R/$\overline{W}$ are reversed to become inputs and the register map is enabled by the signal $\overline{RE}$. Addresses are input via the lower part of the bus. A data transfer acknowledge signal ($\overline{DTACK}$) indicates to the microprocessor that the data transfer is complete.

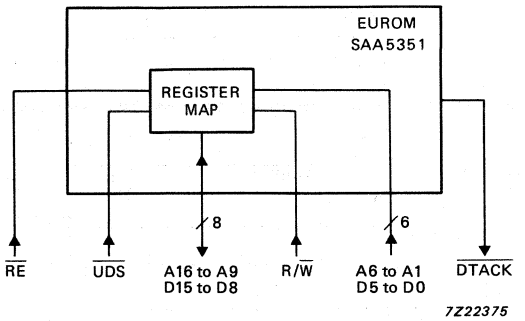


Fig. 20 Microprocessor access to register map.

The main data and address paths used in a connected 68000 interface are shown in Fig. 21. The outputs from the octal latches (74LS373) are enabled only when the 68000 has made the bus available in response to a bus request ($\overline{BR}$). When the register map is accessed data is transferred via the upper part of the bus and the microprocessor's low-order address is passed to EUROM via the octal buffers (74LS244). At the same time the bidirectional buffers (74LS245) disable the signals from the low order data bus of the 68000.

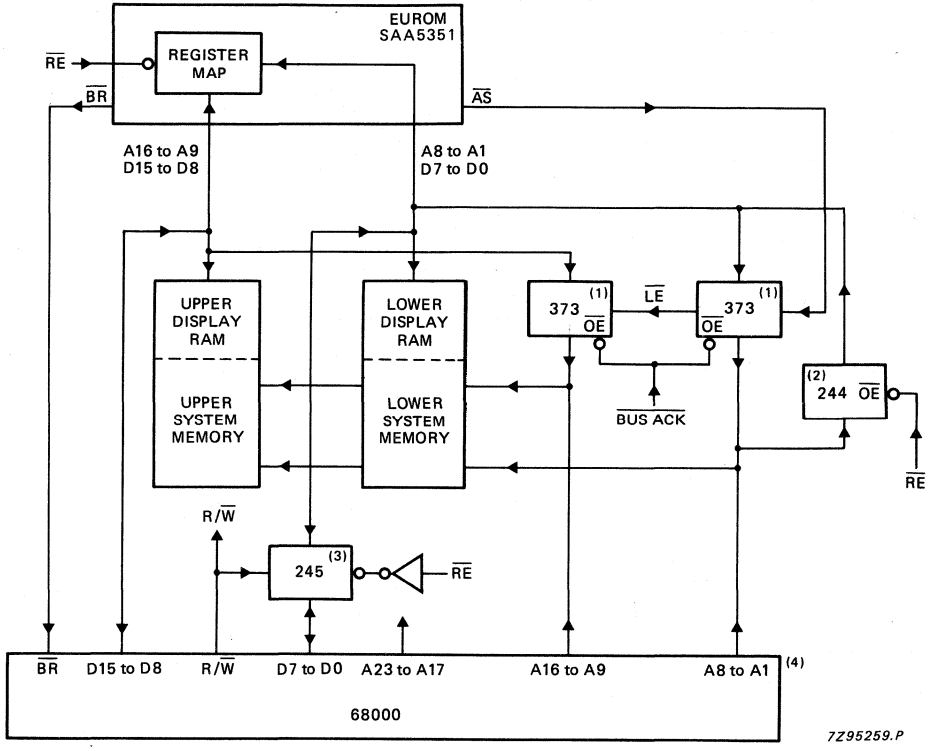
The buffers '244 and '245 may be omitted in a 16-bit write-only configuration where the least-significant data byte is interpreted by EUROM as an address. Here it will generally be necessary for the microprocessor to hold a (readable) 'master copy' of EUROM's scroll map contents at a location in its main memory.

8-bit microprocessors

Although the control bus is optimised for the SCN68000 16-bit microprocessor unit, EUROM will operate with a number of widely differing industry-standard 8, 16 or more-bit microprocessors or microcontrollers (e.g. SCN68008, MAB8051). The interfacing of 8-bit microprocessors to the 16-bit wide display memory is made simple by EUROM's on-chip link-through buffer which provides the microprocessor with bidirectional access to the lower (odd) half of the memory. The link-through buffer is enabled by the buffer-enable signal $\overline{BUFEN}$, and the send/receive direction is controlled by the signal $\overline{S}$/R.

The main data and address paths used in a connected 8-bit microprocessor system are shown in Fig. 22. The interface is similar to that of the 16-bit system but here the display memory does not receive A0 as an address, rather A0 is used as the major enabling signal for $\overline{BUFEN}$ (enables when HIGH).

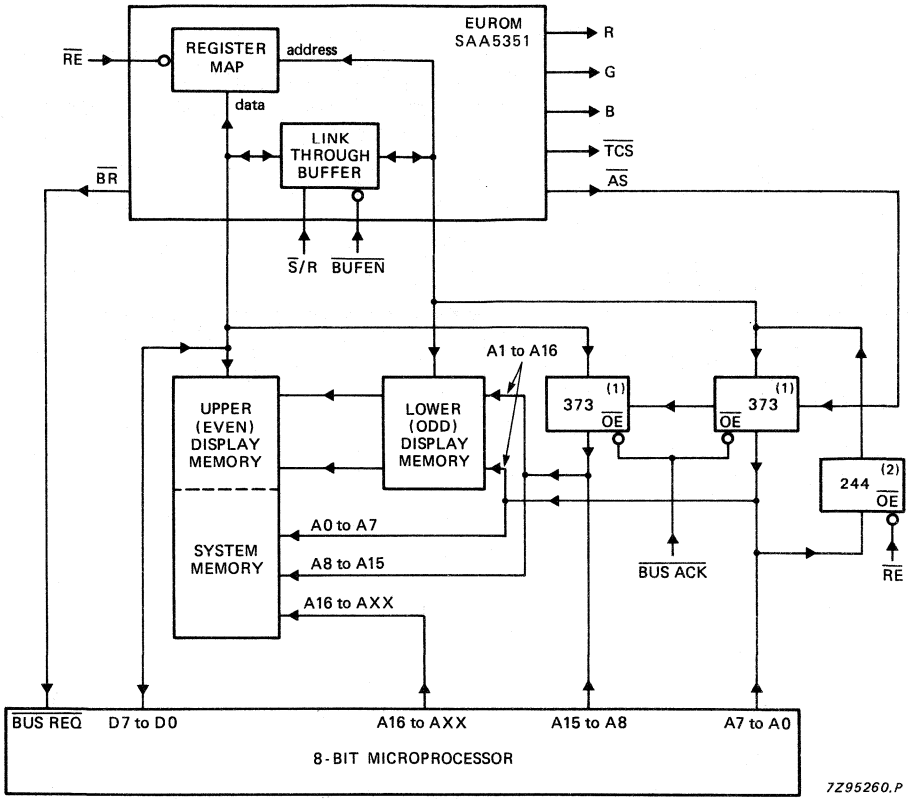
APPLICATION INFORMATION (continued)



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 74LS245 octal bus transceiver (3-state)
(4) SCN68000 microprocessor unit

Fig. 21 Connected 16-bit microprocessor system.

DEVELOPMENT DATA



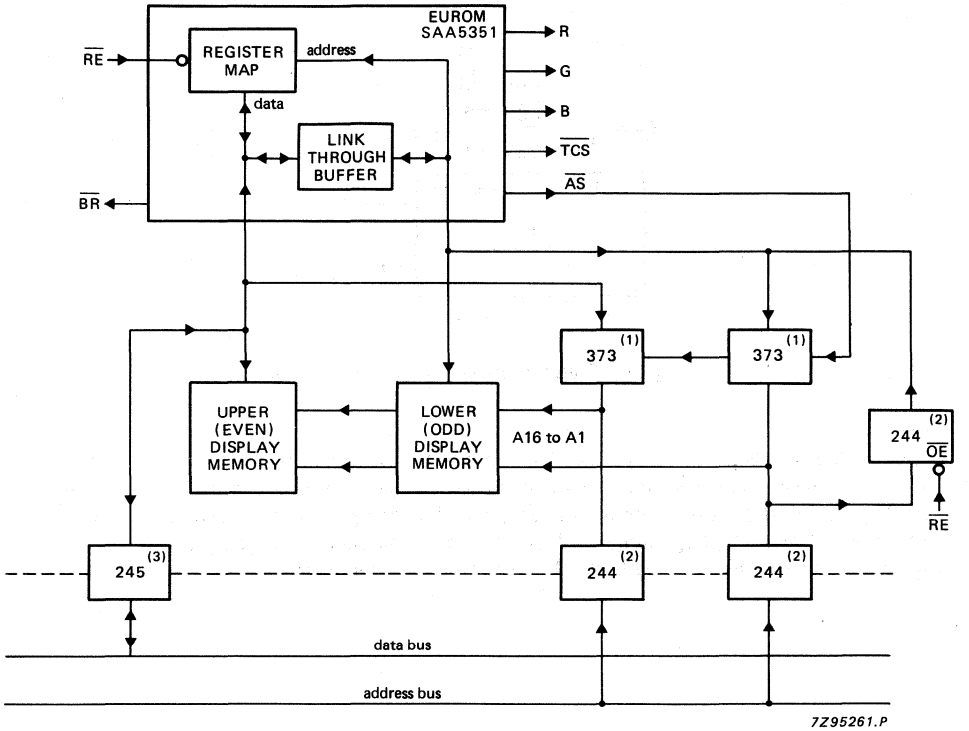
(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)

Fig. 22 Connected 8-bit microprocessor system.

APPLICATION INFORMATION (continued)

Disconnected systems

For many applications it may be desirable to disconnect EUROM and the display memory from the microprocessor and its ROM, RAM and other peripherals by using isolating buffers as shown in Fig. 23. The two parts of the system then operate independently and communicate only when the microprocessor accesses EUROM's register map or the display memory.



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 75LS245 octal bus transceiver (3-state)

Fig. 23 Disconnected 8-bit system.

Synchronization

Stand-alone mode

As a stand-alone device (e.g. in terminal applications) EUROM can output a composite sync signal ($\overline{TCS}$) to the display timebase IC or to a monitor. Timing is obtained from a 6 MHz on-chip oscillator using an external crystal as shown in Fig. 24.

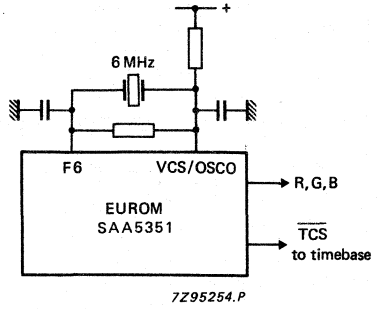


Fig. 24 Stand-alone synchronization mode.

Simple-slave

In the simple-slave mode EUROM synchronizes directly to another device, such as to the $\overline{TCS}$ signal from the SAA5240 European computer-controlled teletext circuit (CCT) or from another EUROM as shown in Fig. 25. EUROM's horizontal counter is reset by the falling edge of $\overline{TCS}$. A dead time of 250 ns is built in to avoid resetting the counter at every tv line and so prevents screen jitter.
Field synchronization is made using EUROM's internal field sync separator.

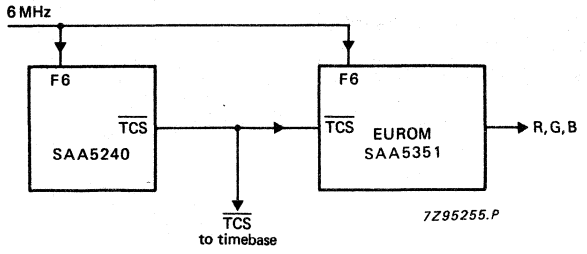


Fig. 25 Simple-slave (direct sync) mode.

APPLICATION INFORMATION (continued)

Synchronization (continued)

Phase-locked slave

The phase-locked slave (indirect sync) mode is shown in Fig. 26. A phase-locked VCO in the SAA5231 teletext video processor provides sync to the timebases. When EUROM is active, its horizontal counter forms part of the phase control loop – a horizontal reference is fed back to the SAA5230 from the SAND output and a vertical reference is generated by feeding separated composite sync to EUROM's field sync separator via the VCS input. In the phase-locked slave mode, the display derived from EUROM can sync with that from a tv source or a local VLP player, thus giving picture-in-text display possiblities.

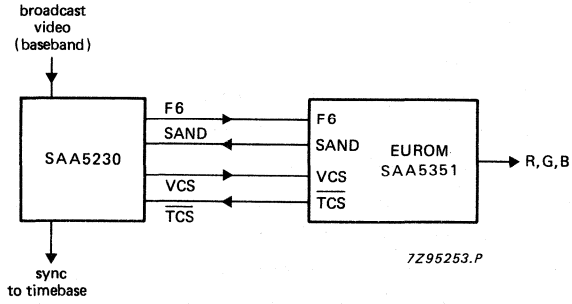


Fig. 26 Phase-locked slave (indirect sync) mode.

SINGLE-CHIP COLOUR CRT CONTROLLER (FTFROM)

GENERAL DESCRIPTION

The SAA5355 FTFROM (Five-Two-Five-ROM) is a single-chip VLSI NMOS crt controller capable of handling the display functions required for a 525-line, level-3 videotex decoder. Only minimal hardware is required to produce a videotex terminal using FTFROM — the simplest configuration needs just a microcontroller and 4 Kbytes of display memory.

Features

- Minimal additional hardware required
- Screen formats of 40/80 character by 1-to-25 row display
- 512 alphanumeric or graphical characters on-chip or extendable off-chip
- Serial attribute storage (STACK) and parallel attribute storage
- Dynamically redefinable character (DRCS) capability over full field
- Interfaces with 8/16-bit microprocessors with optional direct memory access
- On-chip scroll map minimizes data to be transferred when scrolling
- 32 on-screen colours redefinable from a palette of 4096
- Three on-chip digital-to-analogue converters which compensate for crt non-linearity
- Memory interface capable of supporting multi-page terminals. FTFROM can access up to 128 Kbytes of display memory
- Programmable cursor
- Programmable local status row
- Three synchronization modes:

stand-alone	built-in oscillator operating with an external 6,041957 MHz crystal
simple slave	directly synchronized from the source of text composite sync
phase-locked slave	indirect synchronization allows picture-in-text displays (e.g. VCR/VLP video with text overlay)

- On-chip timing with composite sync output
- Zoom feature which allows the height of any group of rows to be increased to enhance legibility

PACKAGE OUTLINE

40-lead DIL; plastic (SOT129).

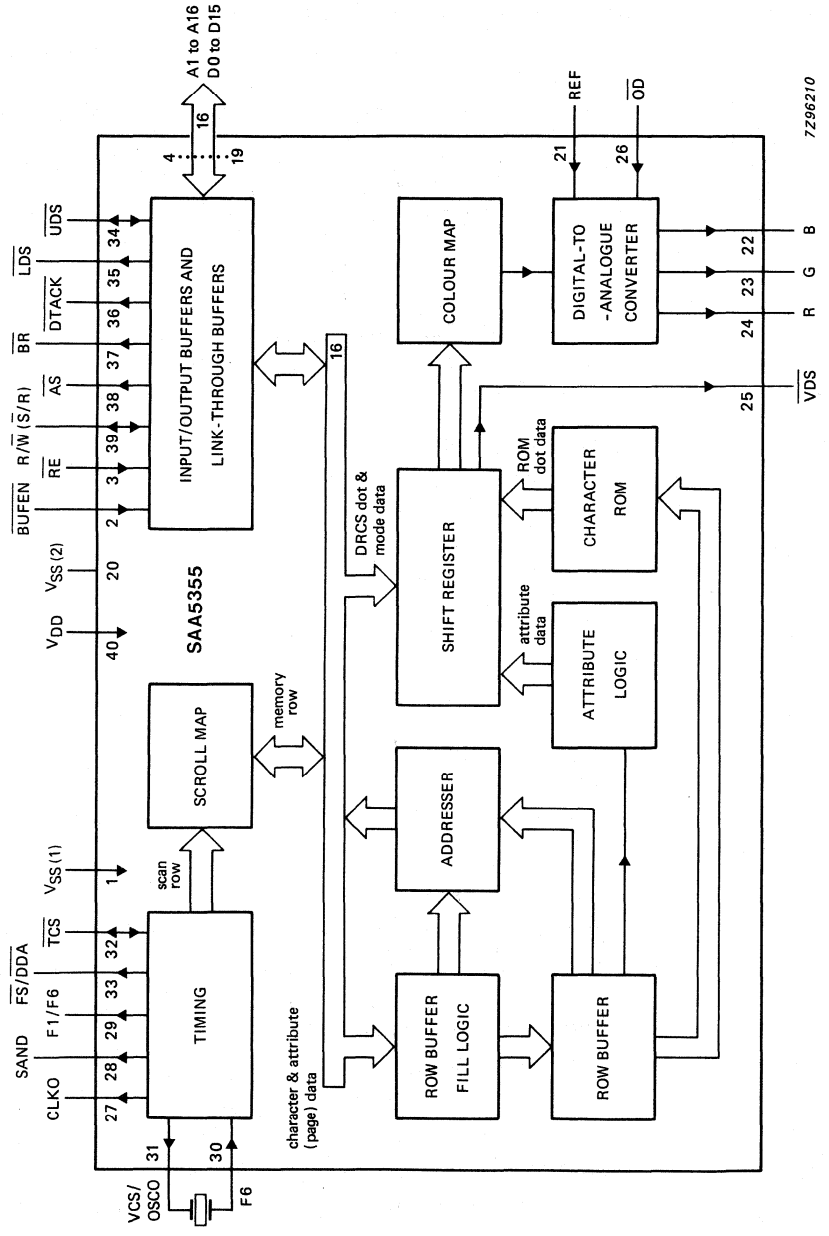


Fig. 1 Block diagram.

PINNING

1	$V_{SS(1)}$	Ground (0 V).
2	$\overline{BUFEN}$	Buffer enable input to the 8-bit link-through buffer.
3	$\overline{RE}$	Register enable input. This enables A1 to A6 and $\overline{UDS}$ as inputs, and D8 to D15 as input/outputs.
4 to 19	A16 to A1/ D15 to D0	Multiplexed address and data bus input/outputs. These pins also function as the 8-bit link-through buffer.
20	$V_{SS(2)}$	Ground (0 V).
21	REF	Analogue reference input.
22	B	Analogue outputs (signals are gamma-corrected).
23	G	
24	R	
25	$\overline{VDS}$	Switching output for dot, screen (row), box and window video data; for use when video signal is present (e.g. from tv, VLP, alpha + photographic layer). This output is LOW for tv display and HIGH for text and will interface directly with a number of colour decoder ICs (e.g. TDA3563, TDA3562A).
26	$\overline{OD}$	Output disable causing R, G, B and $\overline{VDS}$ outputs to go to high-impedance state. Can be used at dot-rate.
27	CLKO	12 MHz clock output for hard-copy dot synchronization (referenced to output dots).
28	SAND	Sandcastle feedback output for SAA5230 teletext video processor or other circuit. Used when the display must be locked to the video source (e.g. VLP). The phase-lock part of the sandcastle waveform can be disabled to allow free-running of the SAA5230 phase-locked loop.
29	F1/F6	1,00699 MHz or 6,041957 MHz output.
30	F6	6,041957 MHz clock input (e.g. from SAA5230). Internal a.c. coupling is provided.
31	VCS/OSCO	Video composite sync input (e.g. from SAA5230) for phase reference of vertical display timing when locking to a video source (e.g. VLP) or, in stand-alone sync mode, output from internal oscillator circuit (fixed frequency).
32	$\overline{TCS}$	Text composite sync input/output depending on master/slave status.
33	$\overline{FS}/\overline{DDA}$	Field sync pulse output or defined-display-area flag output (both referenced to output dots).
34	$\overline{UDS}$	Upper data strobe input/output.
35	$\overline{LDS}$	Lower data strobe output.
36	$\overline{DTACK}$	Data transfer acknowledge (open drain output).
37	$\overline{BR}$	Bus request to microprocessor (open drain output).
38	$\overline{AS}$	Address strobe output to external address latches.
39	R/$\overline{W}$ ($\overline{S}$/R)	Read/write input/output. Also serves as send/receive for the link-through buffer.
40	V_{DD}	Positive supply voltage (+ 5 V).

PINNING (continued)

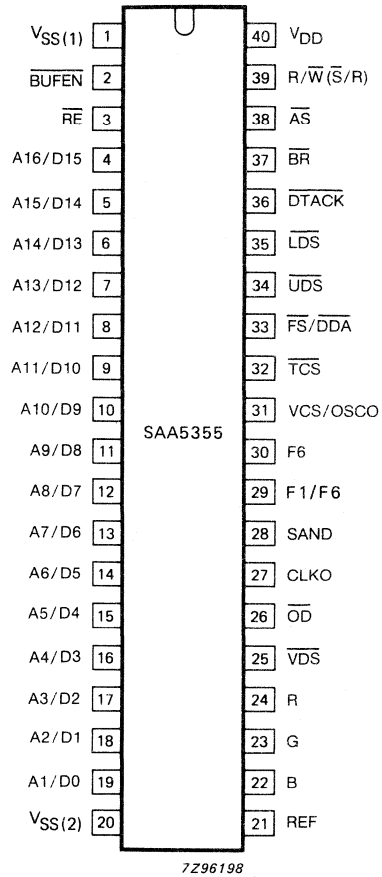


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 40)	V_{DD}	−0,3 to + 7,5 V
Maximum input voltage (except F6, $\overline{TCS}$, REF)	V_{Imax}	−0,3 to + 7,5 V
Maximum input voltage (F6, $\overline{TCS}$)	V_{Imax}	−0,3 to + 10,0 V
Maximum input voltage (REF)	V_{REF}	−0,3 to + 3,0 V
Maximum output voltage	V_{Omax}	−0,3 to + 7,5 V
Maximum output current	I_{Omax}	10 mA
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

Outputs other than CLKO, OSCO, R, G, B, and $\overline{VDS}$ are short-circuit protected.

CHARACTERISTICS

V_{DD} = 5 V ± 5%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 40)	V_{DD}	4,75	5,0	5,25	V
Supply current (pin 40)	I_{DD}	–	–	350	mA
INPUTS					
F6 (note 1)					
Slave modes (Fig. 3)					
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	1,0	–	7,0	V
Input peaks relative to 50% duty factor	$\pm V_P$	0,2	–	3,5	V
Input leakage current at V_I = 0 to 10 V; T_{amb} = 25 °C	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	12	pF
Stand-alone mode (Fig. 4)					
Series capacitance of crystal	C_1	–	28	–	fF
Parallel capacitance of crystal	C_0	–	7,1	–	pF
Resonance resistance of crystal	R_r	–	–	60	Ω
Gain of circuit	G	–	–	*	V/V
$\overline{\text{BUFEN}}$, $\overline{\text{RE}}$, $\overline{\text{OD}}$					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,5	V
Input current at V_I = 0 to V_{DD}+0,3 V; T_{amb} = 25 °C	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	7	pF
REF (Fig. 5)					
Input voltage	V_{REF}	0	1 to 2	2,7	V
Resistance (pin 21 to pin 20) with REF supply and R, G, B outputs OFF	R_{REF}	–	125	–	Ω

* Value under investigation.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
OUTPUTS					
SAND					
Output voltage high level at I_O = 0 to −10 μA	V_{OH}	4,2	–	V_{DD}	V
Output voltage intermediate level at I_O = −10 to + 10 μA	V_{OI}	1,3	2,0	2,7	V
Output voltage low level at I_O = 0,2 mA	V_{OL}	0	–	0,2	V
Load capacitance	C_L	–	–	130	pF
F1/F6, CLKO, $\overline{\text{DDA}}$/$\overline{\text{FS}}$					
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	50	pF
$\overline{\text{LDS}}$, $\overline{\text{AS}}$					
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	200	pF
$\overline{\text{DTACK}}$, $\overline{\text{BR}}$ (open drain outputs)					
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	150	pF
Capacitance (OFF state)	C_{OFF}	–	–	7	pF
R, G, B (note 2)					
Output voltage HIGH (note 3) at I_{OH} = −100 μA; V_{REF} = 2,7 V	V_{OH}	2,4	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Output resistance during line blanking	R_{OBL}	–	–	150	Ω
Output capacitance (OFF state)	C_{OFF}	–	–	12	pF
Output leakage current (OFF state) at V_I = 0 to V_{DD}+ 0,3 V; T_{amb} = 25 °C	I_{OFF}	−10	–	+ 10	μA

parameter	symbol	min.	typ.	max.	unit
$\overline{VDS}$					
Output voltage HIGH at $I_{OH} = -250\ \mu A$	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at $I_{OL} = 2$ mA	V_{OL}	0	–	0,4	V
Output voltage LOW at $I_{OL} = 1$ mA	V_{OL}	0	–	0,2	V
Output leakage current (OFF state) at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_{OFF}	−10	–	+ 10	μA
INPUT/OUTPUTS					
VCS/OSCO					
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input current (output OFF) at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Load capacitance	C_L	–	–	50	pF
$\overline{TCS}$					
Input voltage HIGH	V_{IH}	3,5	–	10,0	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input current at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at $I_{OH} = -200$ to $100\ \mu A$	V_{OH}	2,4	–	6,0	V
Output voltage LOW at $V_{OL} = 3,2$ mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	50	pF
A1/D0 to A16/D15, $\overline{UDS}$, R/$\overline{W}$					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input current at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at $I_{OH} = -200\ \mu A$	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at $I_{OL} = 3,2$ mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	200	pF

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TIMING (note 4)					
F6 (Fig. 3)					
Rise and fall times	t_r, t_f	10	–	80	ns
Frequency	f_{F6}	5,9	–	6,1	MHz
CLKO, F1/F6, R, G, B, $\overline{VDS}$ $\overline{FS}$/$\overline{DDA}$, $\overline{OD}$ (notes 5, 6 and Fig. 6)					
CLKO HIGH time	t_{CLKH}	25	–	–	ns
CLKO LOW time	t_{CLKL}	15	–	–	ns
CLKO rise and fall times	t_{CLKr} t_{CLKf}	–	–	10	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ change	t_{VCH}	10	–	–	ns
R, G, B, $\overline{VDS}$ valid to CLKO rise	t_{VOC}	10	–	–	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ valid	t_{COV}	–	–	60	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ floating after $\overline{OD}$ fall	t_{FOD}	0	–	30	ns
Skew between outputs R, G, B, $\overline{VDS}$	t_{VS}	–	–	20	ns
R, G, B, $\overline{VDS}$ rise and fall times	t_{Vr}, t_{Vf}	–	–	30	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ active after $\overline{OD}$ rise	t_{UOD}	0	–	60	ns
CLKO HIGH to $\overline{FS}$/$\overline{DDA}$ change	t_{DCH}	10	–	60	ns
$\overline{FS}$/$\overline{DDA}$ valid to CLKO rise	t_{DOC}	5	–	–	ns
F1 HIGH time (note 7)	t_{F1H}	–	500	–	ns
F1 LOW time (note 7)	t_{F1L}	–	500	–	ns
F6 HIGH time	t_{F6H}	–	83	–	ns
F6 LOW time	t_{F6L}	–	83	–	ns
$\overline{OD}$ to CLKO rise set-up	t_{ODS}	–	–	45	ns
$\overline{OD}$ to CLKO HIGH hold	t_{ODH}	–	–	0	ns
MEMORY ACCESS TIMING (notes 8, 9 and Fig. 7)					
$\overline{UDS}$, $\overline{LDS}$, $\overline{AS}$					
Cycle time	t_{cyc}	–	500	–	ns
$\overline{UDS}$ HIGH to bus-active for address output	t_{SAA}	75	–	–	ns
Address valid set-up to $\overline{AS}$ fall	t_{ASU}	20	–	–	ns
Address valid hold from $\overline{AS}$ LOW	t_{ASH}	20	–	–	ns
Address float to $\overline{UDS}$ fall	t_{AFS}	0	–	–	ns

parameter	symbol	min.	typ.	max.	unit
$\overline{AS}$ LOW to $\overline{UDS}$ fall delay	t_{ATD}	50	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ HIGH time	t_{HDS}	220	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ LOW time	t_{LDS}	200	–	–	ns
$\overline{AS}$ HIGH time	t_{HAS}	125	–	–	ns
$\overline{AS}$ LOW time	t_{LAS}	320	–	–	ns
$\overline{AS}$ LOW to $\overline{UDS}$ HIGH	t_{AUH}	305	–	–	ns
Data valid set-up to $\overline{UDS}$ rise	t_{DSU}	30	–	–	ns
Data valid hold from $\overline{UDS}$ HIGH	t_{DSH}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{AS}$ rise delay	t_{UAS}	0	–	15	ns
$\overline{AS}$ LOW to data valid	t_{AFA}	–	–	275	ns
Link-through buffers (notes 8, 9 and Fig. 8)					
$\overline{BUFEN}$ LOW to output valid	t_{BEA}	–	–	100	ns
Link-through delay time	t_{LTD}	–	–	85	ns
Input data float prior to direction change	t_{IFR}	0	–	–	ns
Output float after direction change	t_{OFR}	–	–	60	ns
Output float after $\overline{BUFEN}$ HIGH	t_{BED}	–	–	60	ns
Microprocessor READ from FTFROM (Fig. 9)					
R/$\overline{W}$ HIGH set-up to $\overline{UDS}$ fall	t_{RUD}	0	–	–	ns
$\overline{UDS}$ LOW to returned-data access time	t_{UDA}	–	–	210	ns
$\overline{RE}$ LOW to returned data access time	t_{REA}	–	–	210	ns
Data valid to $\overline{DTACK}$ LOW delay	t_{DTL}	40	–	–	ns
$\overline{DTACK}$ LOW to $\overline{UDS}$ rise	t_{DLU}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	75	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	10	–	–	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ fall	t_{UDR}	0	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DSD}	250	–	350	ns
Address valid to $\overline{UDS}$ fall	t_{AUL}	0	–	–	ns

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
MEMORY ACCESS TIMING (continued)					
Microprocessor WRITE to FTFROM (Fig. 10)					
Write cycle time (note 10)	t_{WCY}	500	–	–	ns
R/$\overline{W}$ LOW set-up to $\overline{UDS}$ fall	t_{WUD}	0	–	–	ns
$\overline{RE}$ LOW to $\overline{UDS}$ fall	t_{RES}	30	–	–	ns
Address valid to $\overline{UDS}$ fall	t_{ASS}	30	–	–	ns
$\overline{UDS}$ LOW time	t_{LUS}	100	–	–	ns
Data valid to $\overline{UDS}$ rise	t_{DSS}	80	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DTA}	0	–	60	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	75	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ rise	t_{UDW}	0	–	–	ns
F1/F6 to memory access cycle (Fig. 11)					
$\overline{UDS}$ HIGH to F6 (component of F1/F6) rise	t_{UF6}	20	–	–	ns
F6 (component of F1/F6) HIGH to $\overline{UDS}$ rise	t_{F6U}	40	–	–	ns
SYNCHRONIZATION and BLANKING					
$\overline{TCS}$, SAND, $\overline{FS}$/$\overline{DDA}$					
See Fig. 12 for timing relationships and Fig. 13 for vertical sync and blanking waveforms.					

Notes to the characteristics

1. Pin 30 must be biased externally.
2. 16-level analogue voltage outputs.
3. Output voltage guaranteed when programmed for top level.
4. All timings are related to a 6,00 MHz clock.
5. CLKO, R, G, B, F1/F6, $\overline{VDS}$: C_L = 25 pF.
   $\overline{FS}$/$\overline{DDA}$: C_L = 50 pF
6. CLKO, F1/F6, $\overline{VDS}$, $\overline{FS}$/$\overline{DDA}$: reference levels = 0,8 to 2,0 V
   R, G, B: reference levels = 0,8 to 2,0 V with V_{REF} = 2,7 V
7. These times may momentarily be reduced to a nominal 83 ns in slave-sync mode at the moment of re-synchronization.
8. C_L = 150 pF.
9. Reference levels = 0,8 to 2,0 V.
10. Microprocessor write cycle times of less than 500 ns are permitted but often result in Wait States being generated, the precise timing of $\overline{DTACK}$ will than depend on the internal synchronization time.

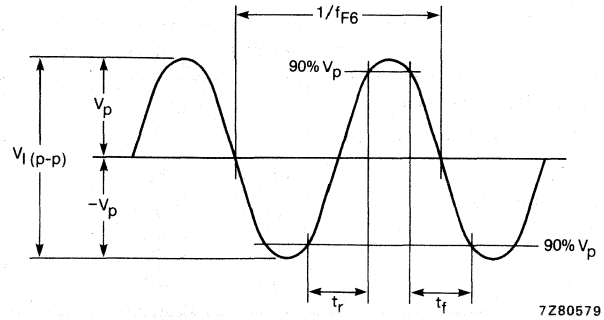
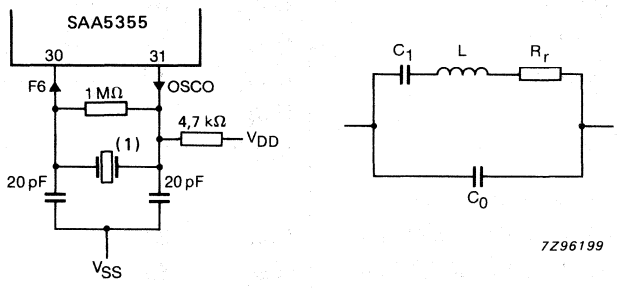


Fig. 3 F6 input waveform.



(1) for 525-line operation, frequency = 6,041957 MHz.

Fig. 4(a) Oscillator circuit for SAA5355 stand-alone sync mode and (b) equivalent circuit of crystal at resonance (see **characteristics** for values).

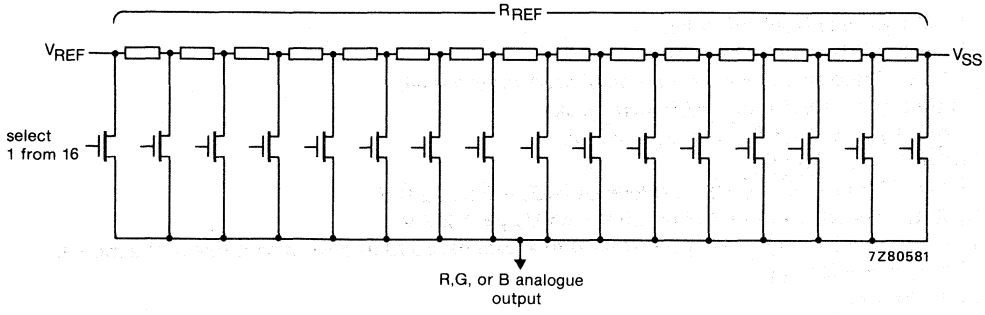


Fig. 5 Circuit arrangement giving one-of-sixteen reference voltage levels for the R, G or B analogue outputs.

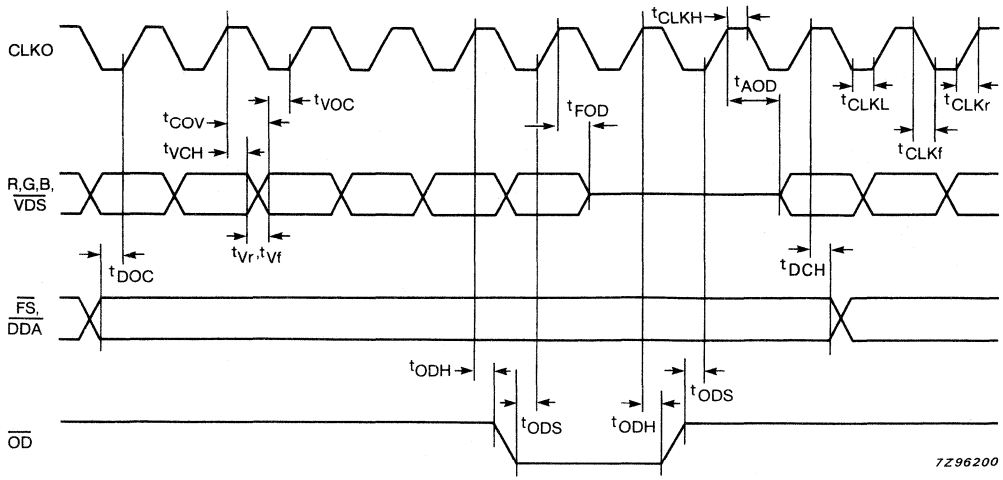


Fig. 6 Video timing.

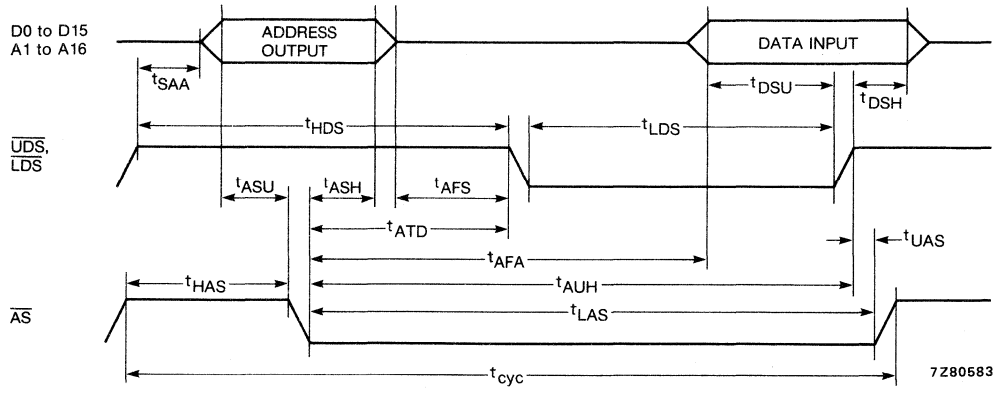


Fig. 7 Memory access timing.

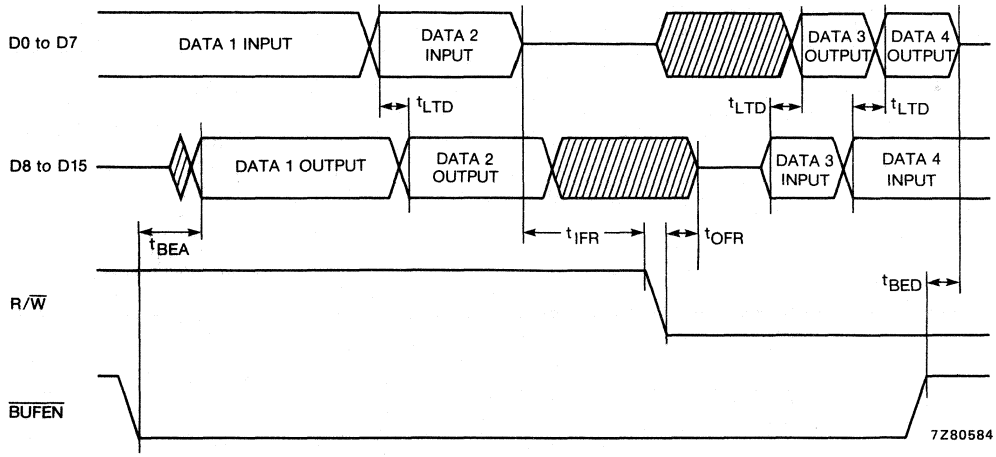


Fig. 8 Timing of link-through buffers.

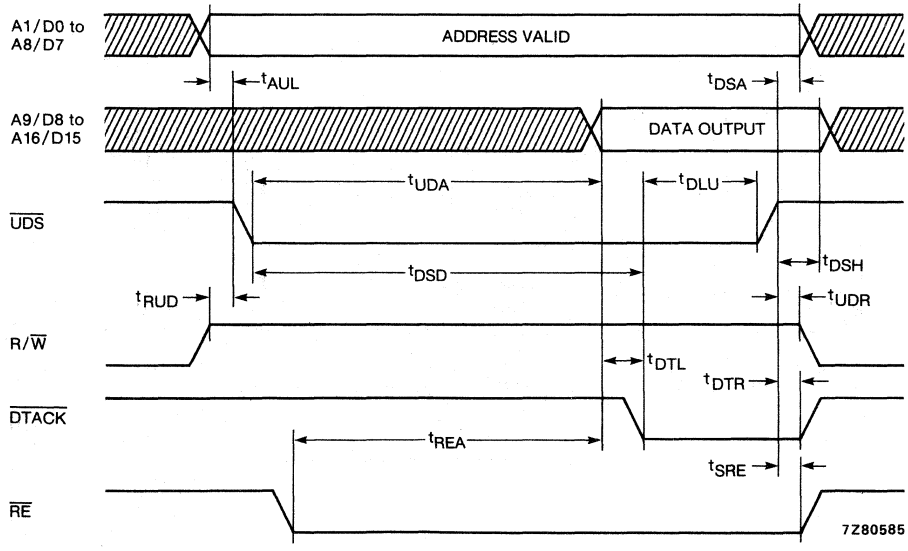


Fig. 9 Timing of microprocessor read from FTFROM.

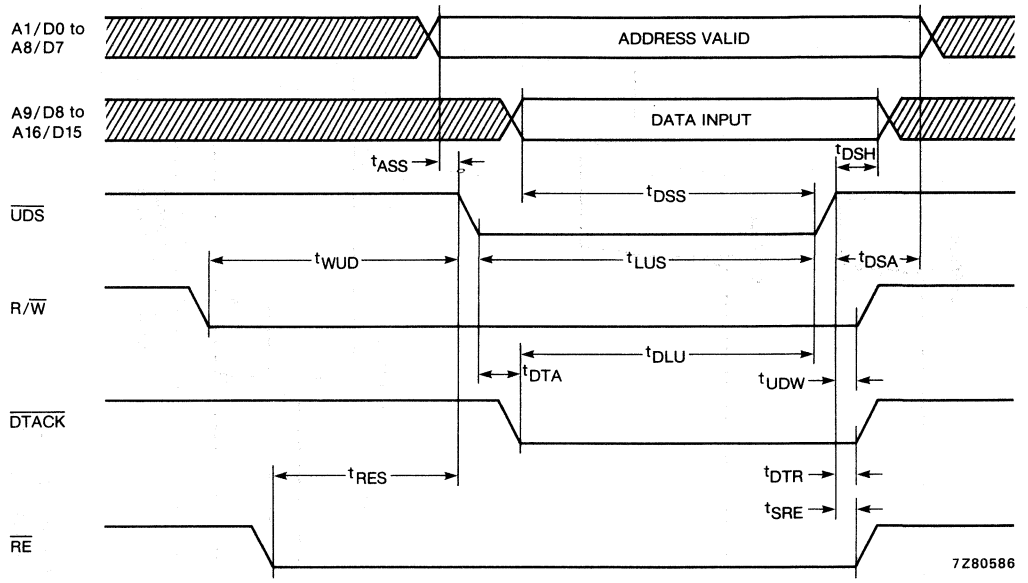


Fig. 10 Timing of microprocessor write to FTFROM.

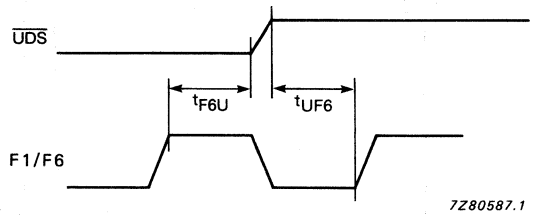


Fig. 11 Timing of F1/F6 to memory access cycle.

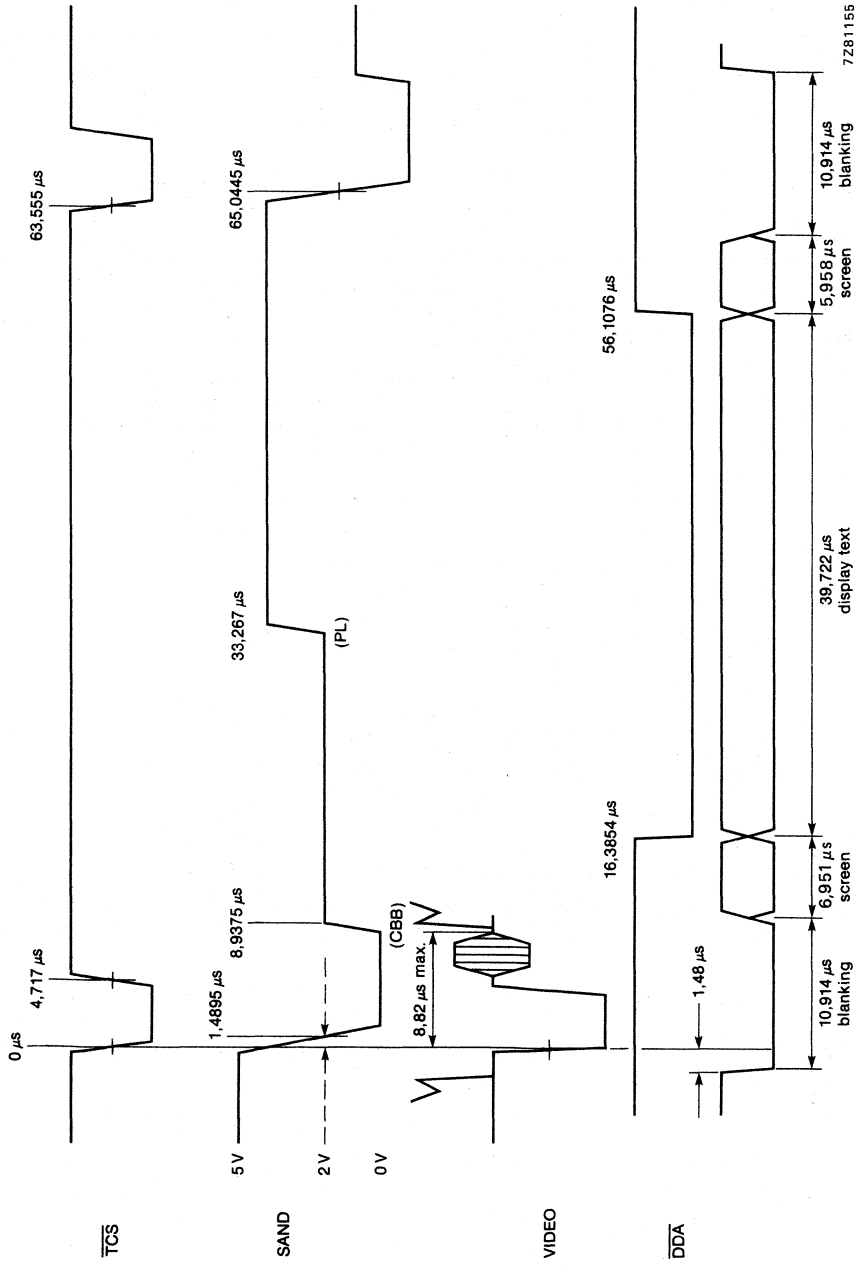


Fig. 12 Timing of synchronization and blanking outputs; all timings are nominal and assume $f_{F6} = 6{,}041957$ MHz.

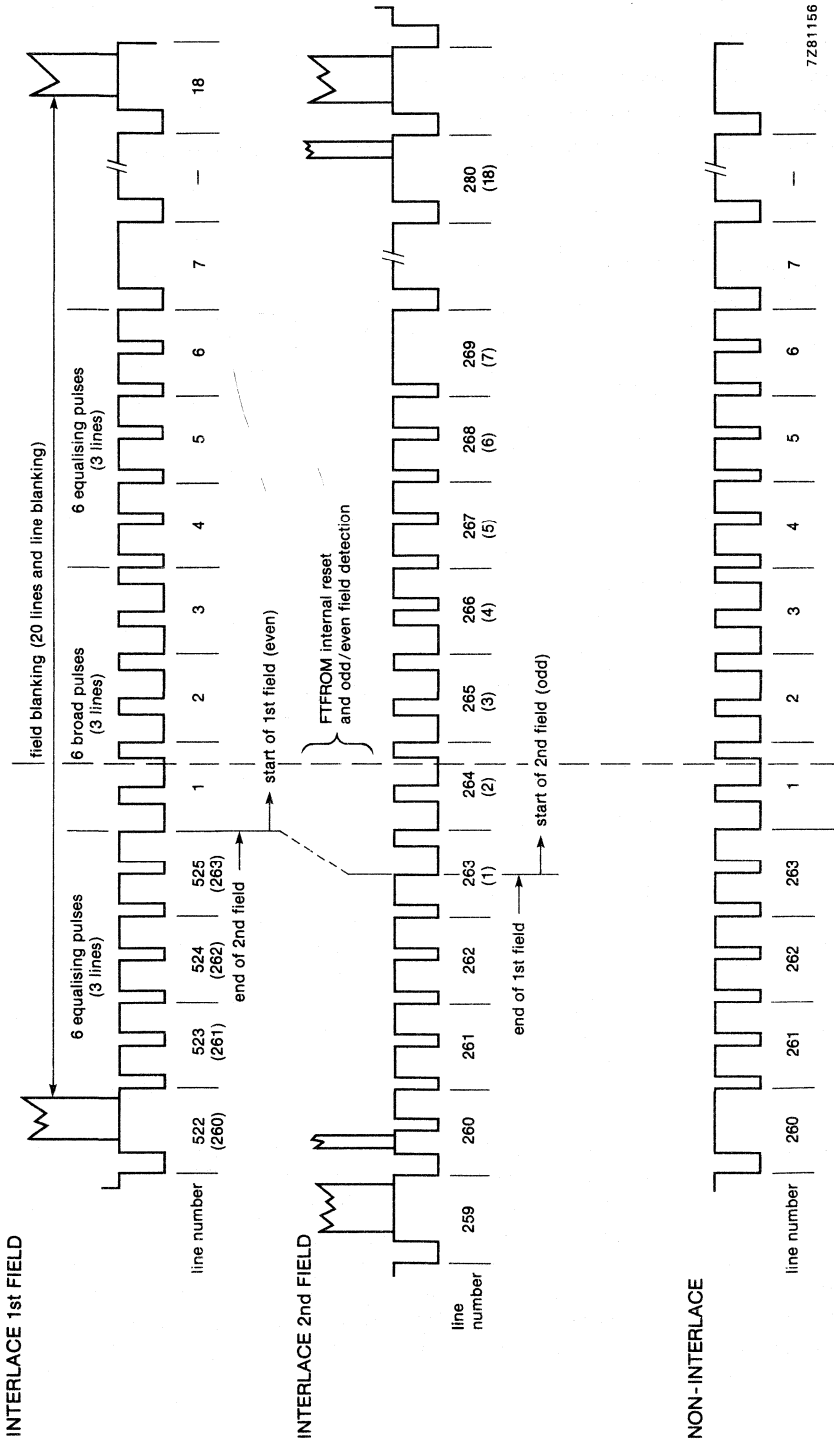


Fig. 13 Vertical synchronization and blanking waveforms; separation of broad pulses = 4,717 μs; equalizing pulse widths = 2,23 μs.

APPLICATION INFORMATION

More detailed application information is available on request

BASIC VIDEOTEX DECODER CONFIGURATION

A basic, practical decoder configuration is shown in Fig. 14, reference should also be made to the block diagram Fig. 1.

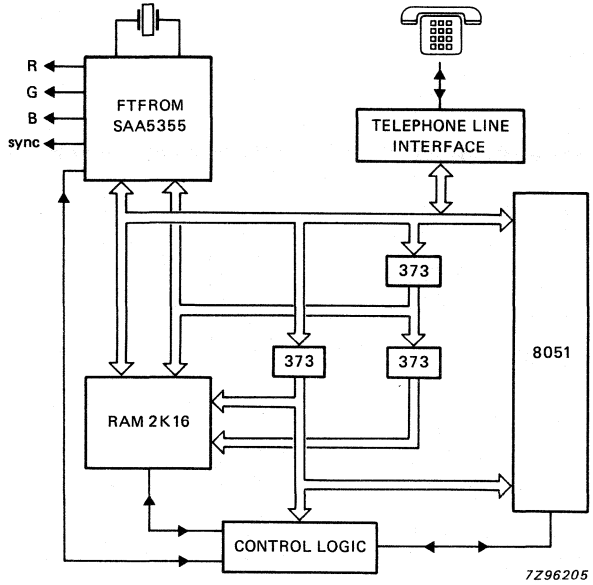


Fig. 14 Basic videotex decoder configuration.

Character and attribute data is fetched from the external memory, processed by the row buffer fill logic according to the stack coding scheme (in stack mode) and then fed into one half of the dual display row buffer. The data fetch process takes place during one line-flyback period (per row) and, since time is required to complete the fill, the other half of the dual row buffer is used for display. The row buffers exchange functions on alternate rows – each holds the 40 columns of 32 bits required to define explicitly every character in a row.

The addresser is used for row buffer filling and for fetching screen colours, and during the display time it is also used for addressing DRCS characters.

Timing

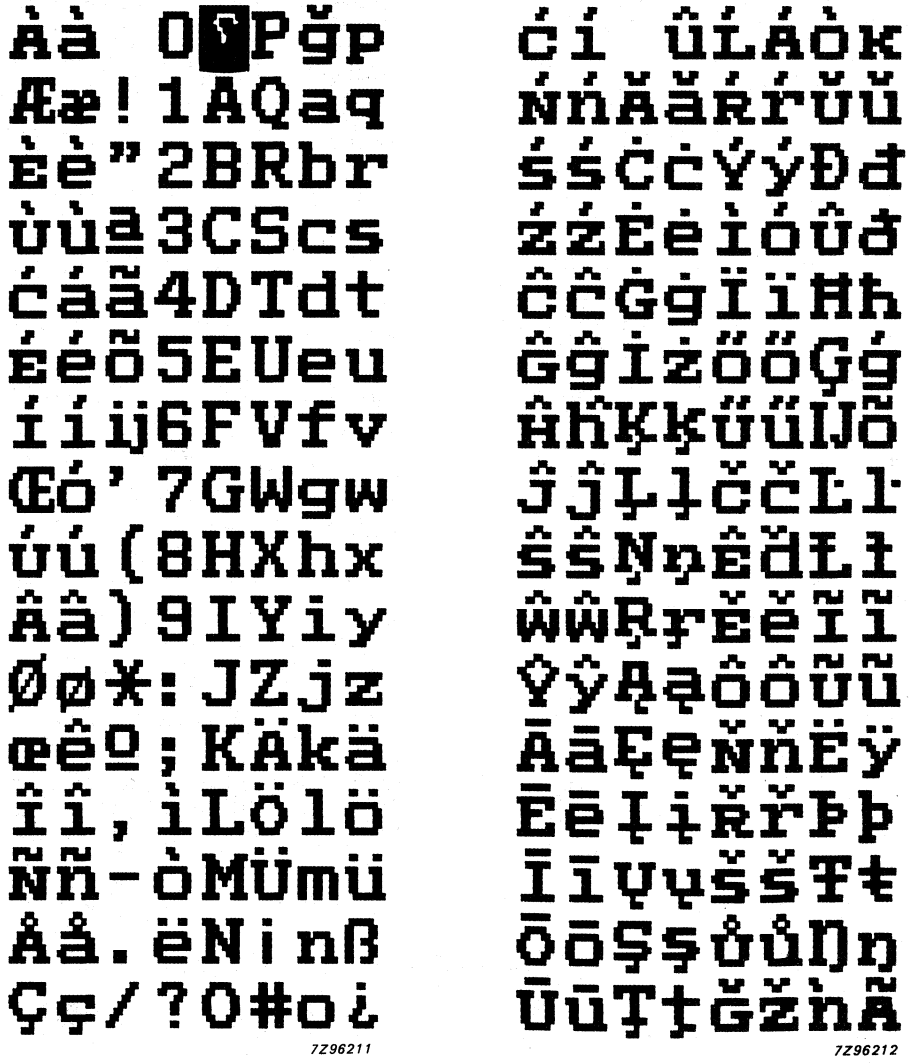
The timing chain operates from an external 6,041957 MHz clock or an on-chip fixed-frequency crystal oscillator. The basic video format is 40 characters per row, 20/21 rows per page and 10 video lines per row. FTFROM will also operate with 25 rows per page and 9 video lines per row.

The display is generated to the normal 525-line/59,94 Hz scanning standard (interlaced or non-interlaced). In addition to composite sync (pin 32) for conventional timebases, a clock output at approximately 1 MHz or 6 MHz (pin 29) is available for driving other devices, and a clock output (pin 27) is available for hard-copy dot synchronization. A defined-display-area timing signal (pin 33) simplifies the application of external peripherals such as a light pen; this signal is nominally coincident with the character dot information.

APPLICATION INFORMATION (continued)

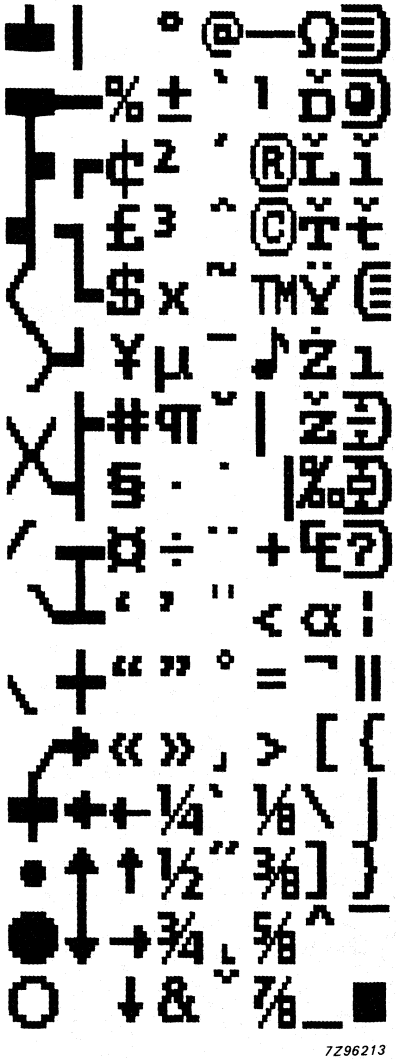
Character generation

FTFROM supports eight character tables, each of (nominally) 128 characters. Four tables are in on-chip ROM and contain fixed characters and four are stored in an external RAM. The fixed character tables (Tables 0 to 3), shown in Figs 15 and 16, are applicable to 10-lines-per-row applications. For 9 lines per row applications, the characters will be as shown but with the last line removed from alpha characters and line 5 (labelling 0 to 9) removed from mosaic and line drawing characters.



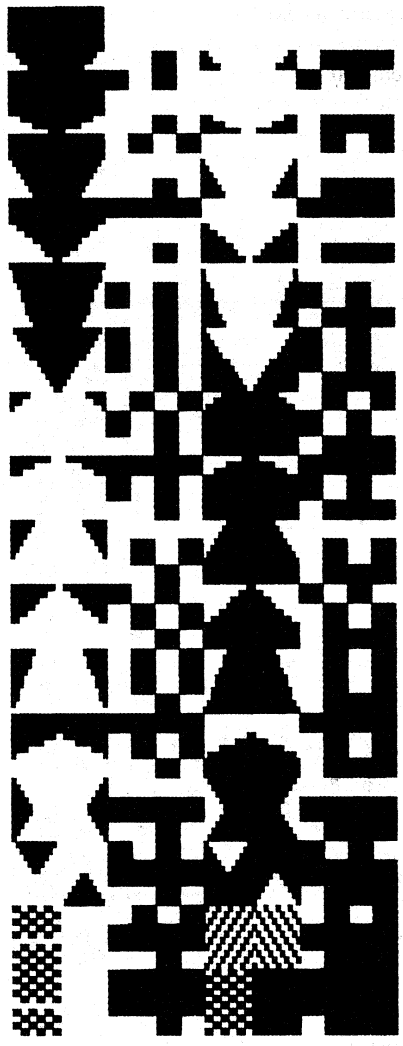
(a) (b)

Fig. 15 On-chip characters: (a) Table 0; (b) Table 1.



7Z96213

(a)



7Z96214

(b)

Fig. 16 On-chip characters: (a) Table 2; (b) Table 3.

APPLICATION INFORMATION (continued)

Character generation (continued)

The 128 most commonly used characters are contained in Table 0, these are the standard upper and lower-case letters of the Roman alphabet, numerals, punctuation and the more common accented characters. In normal text transmission, Table 0 is used most of the time. Table 1 contains other accented characters. Miscellaneous characters, mathematical symbols, the line drawing character set and accents without associated symbols are contained in Table 2. Table 3 contains the block mosaics for the basic alpha-mosaic service and also the new smooth mosaics.

The four tables stored in the external RAM (Tables 4 to 7) are used for DRCS.

Scroll map

The scroll map uses a 26-byte area of on-chip RAM and functions in association with the timing chain. It maps the scan row on to the fetched memory row so allowing the stored page to be displayed in any row order. For each row, a 1-byte pointer to the display memory row is stored in the scroll map. This allows scrolling without the need for data transfer to, or from, side storage.
Additional control bits are stored, allowing 1 to 25 rows to be displayed at any location on the screen.

Colour map and digital-to-analogue converters

The colour map RAM contains thirty-two 12-bit words that are loaded by the microprocessor and read out in three 4-bit groups at pixel rate. Each group is fed to a non-linear (gamma-corrected) D-A converter. The resulting R, G and B outputs are low-impedance with peak-to-peak amplitudes controlled by the reference voltage applied at pin 21.

Cursor

The cursor is available in the stack mode. Its position, character code, character table, foreground colour, background colour, lining and flash attributes are all software programmable via internal register bits.

NON-VIDEOTEX APPLICATIONS

For non-Videotex applications, the device will also support the following operating modes:

Explicit fill mode. An alternative 40 character/rows mode which does not use the memory compression technique of stack coding. More display memory is required but there are no limitations on the number of display attribute changes per row.

80 characters/rows mode. When operating with 80 characters per row, the available display attributes are eight foreground colours, eight (potentially different) background colours (including transparent) as well as underline and blink.

Full field DRCS mode. This mode is not mutually exclusive to the explicit fill and 80 characters/rows modes but rather the available DRCS memory is expanded so that the whole screen can be covered, thus enabling a 'bit map'. All ROM-based characters and all display attributes remain available.

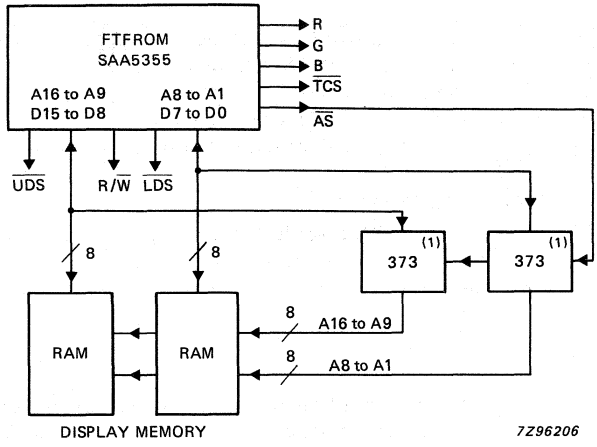
MICROPROCESSOR and RAM BUS INTERFACE

Three types of data transfer take place at the bus interface:

- FTFROM fetches data from the display memory
- The microprocessor reads from, or writes to, FTFROM's internal register map
- The microprocessor accesses the display memory

FTFROM access to display memory (Figs 17 and 18)

FTFROM accesses the external display memory via a 16-bit multiplexed address and data bus with a cycle time of 496,5 ns (F6 = 6,041957 MHz). The address strobe ($\overline{AS}$) signal from FTFROM flags the bus cycle and writes the address into octal latches (74LS373). The display data is stored in bytes of upper (most-significant) and lower (least-significant) display information and is always fetched in pairs of bytes (upper + lower = 16 bits). The upper and lower display RAM sections are enabled simultaneously by the upper and lower data strobes (respectively $\overline{UDS}$ and $\overline{LDS}$) which are always asserted together to fetch a 16-bit word. The read/write control R/$\overline{W}$ is included although FTFROM only reads from the display memory.



(1) 74LS373 octal transparent latch (3-state)

Fig. 17 Simple RAM interface circuit for display memory access.

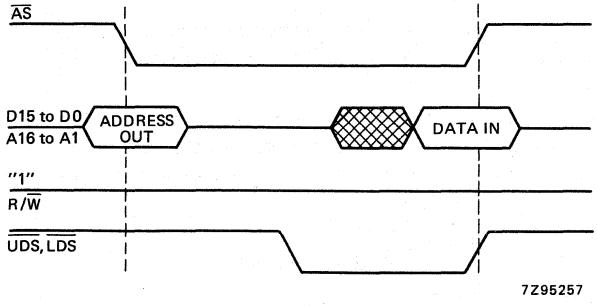


Fig. 18 Bus timing for display memory access.

APPLICATION INFORMATION (continued)

FTFROM access to display memory (continued)

The display memory organization uses the word/byte addressing convention adopted for the SCN68000 microprocessor series. Data fetched on the 16-bit bus is considered in terms of bytes where the even numbered bytes use the upper (most-significant) part of the bus as shown in Fig. 19. The word addresses are numerically the same as the upper byte that they contain — there are no odd-numbered word addresses.

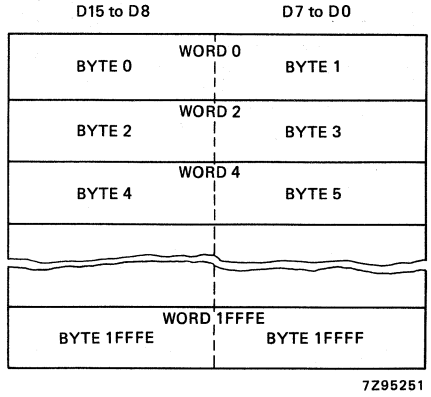


Fig. 19 Display memory word/byte organization.

Warning time

As FTFROM is a real-time display device, it must have direct access to the display memory with priority over the microprocessor and other peripheral devices. This is achieved by FTFROM issuing a bus request ($\overline{BR}$) signal for the duration of the memory access plus a programmable advance warning time which allows the microprocessor to complete its current bus cycle.

In systems where the buses of the microprocessor and FTFROM are intimately connected (connected systems), $\overline{BR}$ may be used to suspend all microprocessor activity so that FTFROM can act as a dedicated DMA controller. In systems where the two buses are separated by buffers (disconnected systems), $\overline{BR}$ may be used either to generate an interrupt or as a direct signal. To these ends, the warning time between the assertion of $\overline{BR}$ and the beginning of FTFROM's bus activity is programmable to be between 0 and 22,84 μs.

Microprocessor access to register map

FTFROM has a set of internal registers which, when memory-mapped, behave as an 8-bit wide RAM connected to the upper part of the data bus (Fig. 20). The control signals $\overline{UDS}$ and R/$\overline{W}$ are reversed to become inputs and the register map is enabled by the signal $\overline{RE}$. Addresses are input via the lower part of the bus. A data transfer acknowledge signal ($\overline{DTACK}$) indicates to the microprocessor that the data transfer is complete.

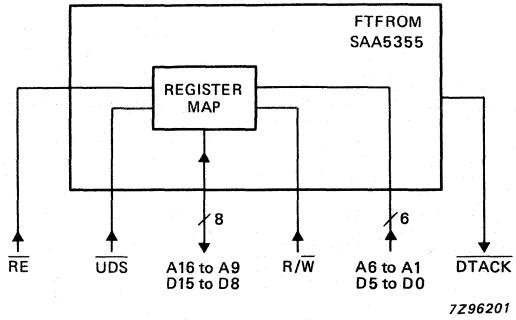


Fig. 20 Microprocessor access to register map.

The main data and address paths used in a connected 68000 interface are shown in Fig. 21. The outputs from the octal latches (74LS373) are enabled only when the 68000 has made the bus available in response to a bus request ($\overline{BR}$). When the register map is accessed data is transferred via the upper part of the bus and the microprocessor's low-order address is passed to FTFROM via the octal buffers (74LS244). At the same time the bidirectional buffers (74LS245) disable the signals from the low order data bus of the 68000.

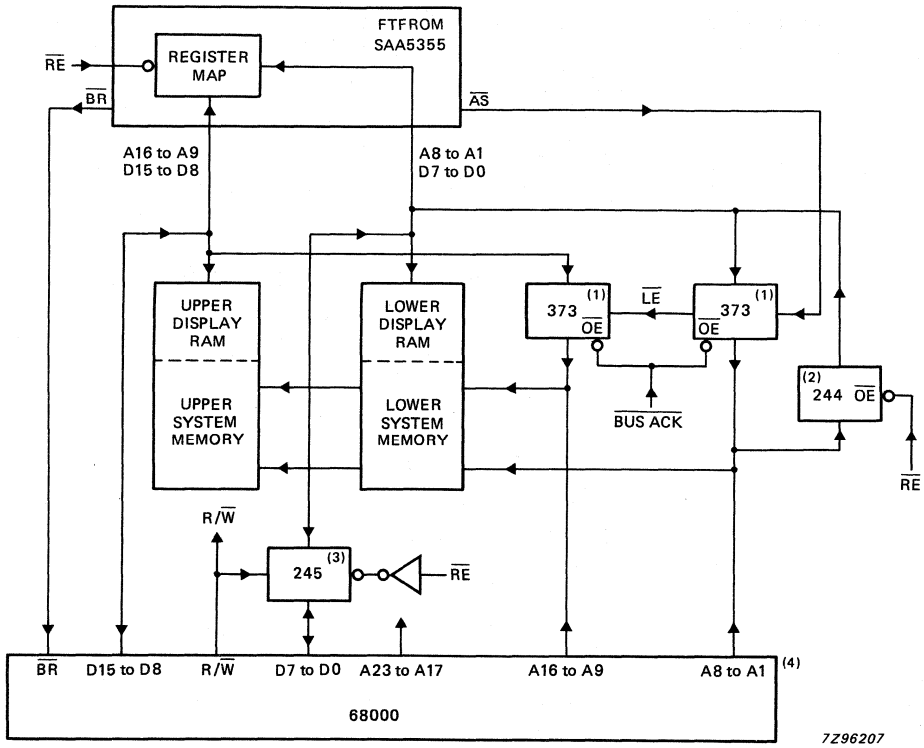
The buffers '244 and '245 may be omitted in a 16-bit write-only configuration where the least-significant data byte is interpreted by FTFROM as an address. Here it will generally be necessary for the microprocessor to hold a (readable) 'master copy' of FTFROM's scroll map contents at a location in its main memory.

8-bit microprocessors

Although the control bus is optimised for the SCN68000 16-bit microprocessor unit, FTFROM will operate with a number of widely differing industry-standard 8, 16 or more-bit microprocessors or microcontrollers (e.g. SCN68008, MAB8051). The interfacing of 8-bit microprocessors to the 16-bit wide display memory is made simple by FTFROM's on-chip link-through buffer which provides the microprocessor with bidirectional access to the lower (odd) half of the memory. The link-through buffer is enabled by the buffer-enable signal $\overline{BUFEN}$, and the send/receive direction is controlled by the signal $\overline{S}$/R.

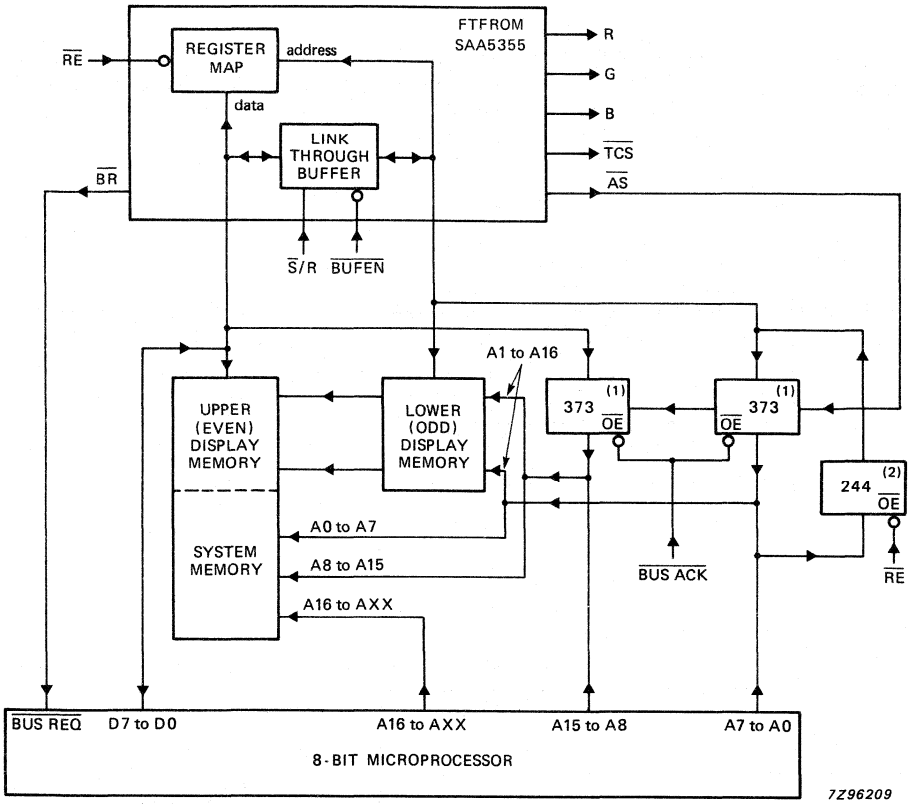
The main data and address paths used in a connected 8-bit microprocessor system are shown in Fig. 22. The interface is similar to that of the 16-bit system but here the display memory does not receive A0 as an address, rather A0 is used as the major enabling signal for $\overline{BUFEN}$ (enables when HIGH).

APPLICATION INFORMATION (continued)



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 74LS245 octal transceiver (3-state)
(4) SCN68000 microprocessor unit

Fig. 21 Connected 16-bit microprocessor system.



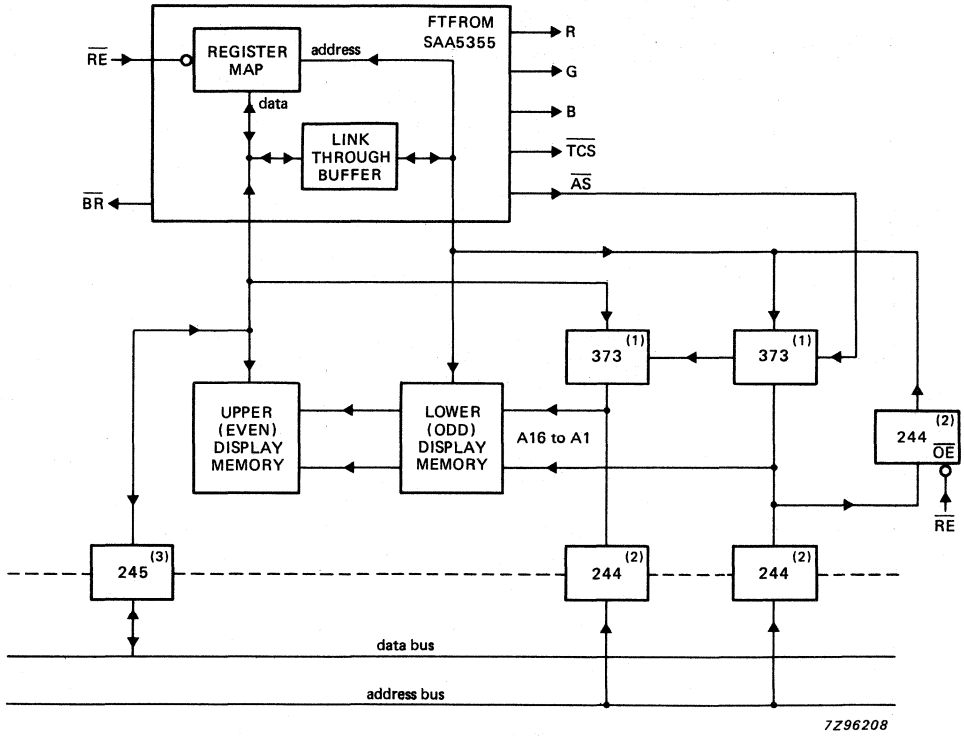
(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)

Fig. 22 Connected 8-bit microprocessor system.

APPLICATION INFORMATION (continued)

Disconnected systems

For many applications it may be desirable to disconnect FTFROM and the display memory from the microprocessor and its ROM, RAM and other peripherals by using isolating buffers as shown in Fig. 23. The two parts of the system then operate independently and communicate only when the microprocessor accesses FTFROM's register map or the display memory.



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 74LS245 octal bus transceiver (3-state)

Fig. 23 Disconnected 8-bit system.

Synchronization

Stand-alone mode

As a stand-alone device (e.g. in terminal applications) FTFROM can output a composite sync signal ($\overline{TCS}$) to the display timebase IC or to a monitor. Timing is obtained from a 6,041957 MHz on-chip oscillator using an external crystal as shown in Fig. 24.

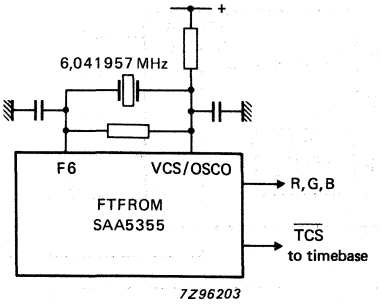


Fig. 24 Stand-alone synchronization mode.

Simple-slave

In the simple-slave mode FTFROM synchronizes directly to another device as shown in Fig. 25. FTFROM's horizontal counter is reset by the falling edge of $\overline{TCS}$. A dead time of 250 ns is built in to avoid resetting the counter at every tv line and so prevents screen jitter.
Field synchronization is made using FTFROM's internal field sync separator.

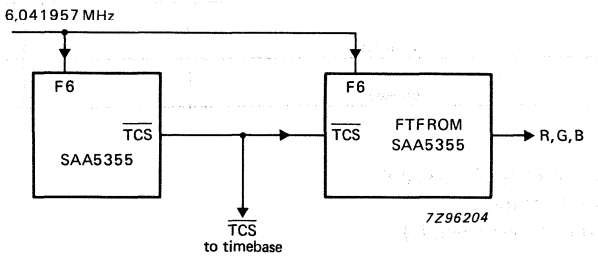


Fig. 25 Simple-slave (direct sync) mode.

APPLICATION INFORMATION (continued)

Synchronization (continued)

Phase-locked slave

The phase-locked slave (indirect sync) mode is shown in Fig. 26. A phase-locked VCO in the SAA5230 teletext video processor provides sync to the timebases. When FTFROM is active, its horizontal counter forms part of the phase control loop – a horizontal reference is fed back to the SAA5230 from the SAND output and a vertical reference is generated by feeding separated composite sync to FTFROM's field sync separator via the VCS input. In the phase-locked slave mode, the display derived from FTFROM can sync with that from a tv source or a local VLP player, thus giving picture-in-text display possibilities.

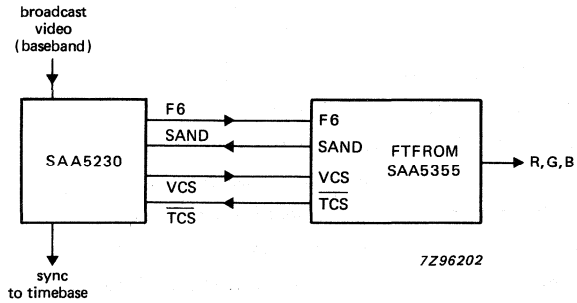


Fig. 26 Phase-locked slave (indirect sync) mode.

EUROM 60 Hz

GENERAL DESCRIPTION

The SAA5361 EUROM is a single-chip VLSI NMOS crt controller capable of handling all display functions required by the CEPT videotex terminal, model A4. Only minimal hardware is required to produce a videotex terminal using EUROM – the simplest configuration needs just a microcontroller and 4 Kbytes of display memory.

Features

- Minimal additional hardware required
- Screen formats of 40/80 character by 1-to-25 row display
- 512 alphanumeric or graphical characters on-chip or extendable off-chip
- Serial attribute storage (STACK) and parallel attribute storage
- Dynamically redefinable character (DRCS) capability over full field
- Interfaces with 8/16-bit microprocessors with optional direct memory access
- On-chip scroll map minimizes data to be transferred when scrolling
- On-chip colour map RAM (4096 locations) and three on-chip digital-to-analogue converters allow 32 colours on-screen
- On-chip digital-to-analogue converters are non-linear to compensate for crt non-linearity
- Memory interface capable of supporting multi-page terminals. EUROM can access up to 128 Kbytes of display memory
- Programmable cursor
- Programmable local status row
- Three synchronization modes:

stand-alone	built-in oscillator operating with an external 7.2 MHz crystal
simple slave	directly synchronized from the source of text composite sync
phase-locked slave	indirect synchronization allows picture-in-text displays (e.g. VCR/VLP video with text overlay)

- On-chip timing composite sync output
- Zoom feature which allows the height of any group of rows to be increased to enhance legibility

PACKAGE OUTLINE

40-lead DIL; plastic (SOT129).

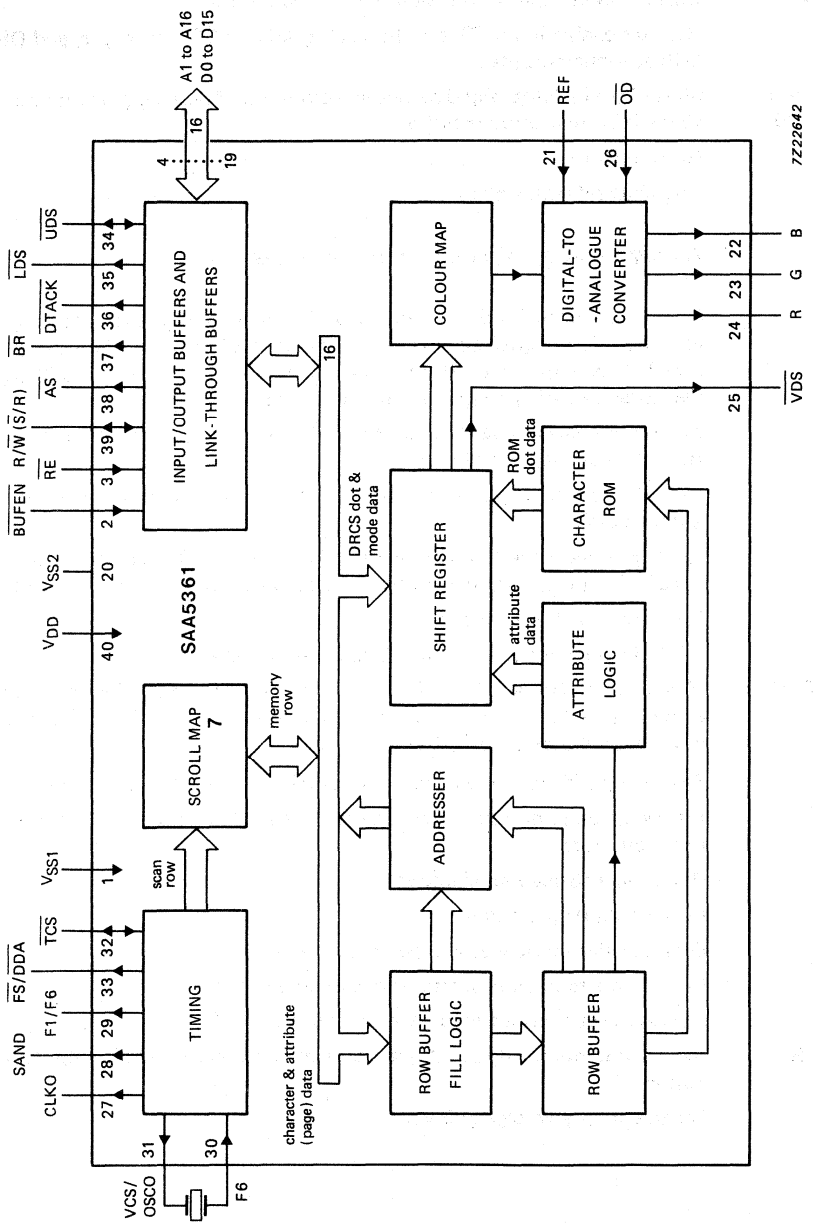


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

1	V_{SS1}	Ground 0 V.
2	$\overline{BUFEN}$	Buffer enable input to the 8-bit link-through buffer.
3	$\overline{RE}$	Register enable input. This enables A1 to A6 and $\overline{UDS}$ as inputs, and D8 to D15 as input/outputs.
4 to 19	A16 to A1/ D15 to D0	Multiplexed address and data bus input/outputs. These pins also function as the 8-bit link-through buffer.
20	V_{SS2}	Ground (0 V).
21	REF	Analogue reference input.
22	B	Analogue outputs (signals are gamma-corrected).
23	G	
24	R	
25	$\overline{VDS}$	Switching output for dot, screen (row), box and window video data; for use when video signal is present (e.g. from tv, VLP, alpha + photographic layer). This output is LOW for tv display and HIGH for text and will interface directly with a number of colour decoder ICs.
26	$\overline{OD}$	Output disable causing R, G, B and $\overline{VDS}$ outputs to go to high-impedance state. Can be used at dot-rate.
27	CLKO	14.4 MHz clock output for hard-copy dot synchronization (referenced to output dots).
28	SAND	Sandcastle feedback to other circuit, when display must be locked to a VLP. The phase-lock part of the sandcastle waveform can be disabled.
29	F1/F6	1.2 MHz or 7.2 MHz output.
30	F6	7.2 MHz clock input. Internal AC coupling is provided.
31	VCS/OSCO	Video composite sync input for phase reference of vertical display timing when locking to a video source or, in stand-alone sync mode, output from internal oscillator circuit (fixed frequency).
32	$\overline{TCS}$	Text composite sync input/output depending on master/slave status.
33	$\overline{FS}/\overline{DDA}$	Field sync pulse output or defined-display-area flag output (both referenced to output dots).
34	$\overline{UDS}$	Upper data strobe input/output.
35	$\overline{LDS}$	Lower data strobe output.
36	$\overline{DTACK}$	Data transfer acknowledge (open drain output).
37	$\overline{BR}$	Bus request to microprocessor (open drain output).
38	$\overline{AS}$	Address strobe output to external address latches.
39	R/$\overline{W}$ ($\overline{S}$/R)	Read/write input/output. Also serves as send/receive for the link-through buffer.
40	V_{DD}	Positive supply voltage (+ 5 V).

PINNING (continued)

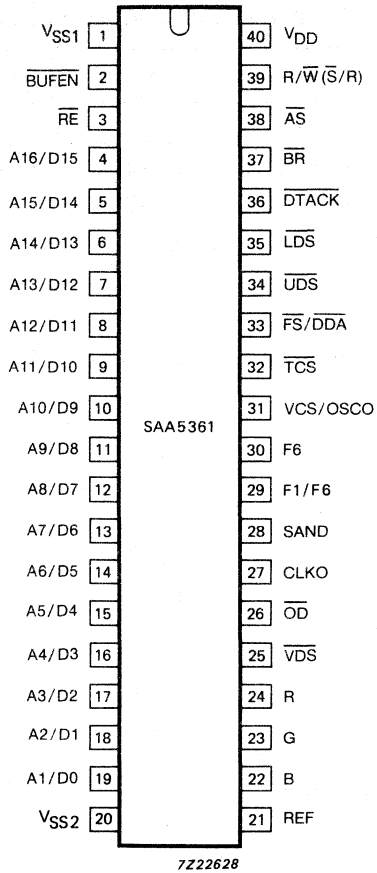


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 40)	V_{DD}	−0.3 to +7.5 V
Maximum input voltage (except F6, $\overline{TCS}$, REF)	V_{Imax}	−0.3 to +7.5 V
Maximum input voltage (F6, $\overline{TCS}$)	V_{Imax}	−0.3 to +10.0 V
Maximum input voltage (REF)	V_{REF}	−0.3 to +3.0 V
Maximum output voltage	V_{Omax}	−0.3 to +7.5 V
Maximum output current	I_{Omax}	10 mA
Operating ambient temperature range	T_{amb}	0 to +60 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

Outputs other than CLKO, OSCO, R, G, B, and $\overline{VDS}$ are short-circuit protected.

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 5 V ± 5%; V_{SS} = 0 V; T_{amb} = 0 to +60 °C, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 40)	V_{DD}	4.75	5.0	5.25	V
Supply current (pin 40)	I_{DD}	–	–	390	mA
INPUTS					
F6					
Slave modes (Fig. 3)					
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	2.5	3.0	7.0	V
Input leakage current at V_I = 0 to $V_{CC\,max}$; T_{amb} = 25 °C	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	12	pF
Stand-alone mode (Fig. 4)					
Series capacitance of crystal	C_1	–	28	–	fF
Parallel capacitance of crystal	C_0	–	7.1	–	pF
Resonance resistance of crystal	R_r	–	–	60	Ω
$\overline{\text{BUFEN}}$, $\overline{\text{RE}}$, $\overline{\text{OD}}$					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	6.5	V
Input leakage current at V_I = 0 to V_{DD}+ 0.3 V; T_{amb} = 25 °C	I_{IL}	−10	–	+ 10	μA
Input capacitance	C_I	–	–	7	pF
REF (Fig. 5)					
Input voltage	V_{REF}	0	1 to 2	2.7	V
Resistance (pin 21 to pin 20) with REF supply and R, G, B outputs OFF	R_{REF}	–	125	–	Ω

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
OUTPUTS					
SAND					
Output voltage high level at I_O = 0 to −10 μA	V_{OH}	4.2	–	V_{DD}	V
Output voltage intermediate level at I_O = −10 to + 10 μA	V_{OI}	1.3	–	2.7	V
Output voltage low level at I_O = 0.2 mA	V_{OL}	0	–	0.2	V
Load capacitance (note 1)	C_L	–	–	130	pF
F1/F6, $\overline{DDA}$/$\overline{FS}$					
Output voltage HIGH	V_{OH}	2.4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3.2 mA	V_{OL}	0	–	0.4	V
Load capacitance (note 1)	C_L	–	–	50	pF
$\overline{LDS}$, $\overline{AS}$					
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2.0	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3.2 mA	V_{OL}	0	–	0.8	V
Load capacitance (note 1)	C_L	–	–	200	pF
$\overline{DTACK}$, $\overline{BR}$ (open drain outputs)					
Output voltage LOW at I_{OL} = 3.2 mA	V_{OL}	0	–	0.4	V
Load capacitance (note 1)	C_L	–	–	150	pF
Capacitance (OFF state)	C_{OFF}	–	–	7	pF
R, G, B (note 2)					
Output voltage HIGH (note 3) at I_{OH} = −100 μA; V_{REF} = 2.7 V	V_{OH}	2.4	–	–	V
Output voltage LOW at I_{OL} = 2 mA (note 10)	V_{OL}	–	–	0.4	V
Output resistance during line blanking	R_{OBL}	–	–	150	Ω
Output capacitance (OFF state)	C_{OFF}	–	–	12	pF
Output leakage current (OFF state) at V_I = 0 to V_{DD}+ 0.3 V; T_{amb} = 25 °C	I_{OFF}	−10	–	+ 10	μA
CLOCKO					
Output voltage HIGH	V_{OH}	2.0		V_{DD}	V
Output voltage LOW	V_{OL}	0		0.8	V
Load capacitance (note 1)	C_L	–		50	pF

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
$\overline{VDS}$					
Output voltage HIGH	V_{OH}	2.0	–	V_{DD}	V
Output voltage LOW	V_{OL}	0	–	0.8	V
Output leakage current (OFF state) at V_I = 0 to V_{DD} + 0.3 V; T_{amb} = 25 °C	I_{LO}	−10	–	+ 10	μA
INPUTS/OUTPUTS					
VCS/OSCO					
Input voltage HIGH	V_{IH}	2.0	–	6.0	V
Input voltage LOW	V_{IL}	0	–	0.8	V
Output leakage current (output OFF) at V_I = 0 to V_{DD} + 0.3 V; T_{amb} = 25 °C	I_{LO}	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Load capacitance (note 1)	C_L	–	–	50	pF
$\overline{TCS}$					
Input voltage HIGH	V_{IH}	3.5	–	10.0	V
Input voltage LOW	V_{IL}	0	–	1.5	V
Output leakage current at V_I = 0 to V_{DD} + 0.3 V; T_{amb} = 25 °C	I_{LO}	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at I_{OH} = −200 to 100 μA	V_{OH}	2.0	–	6.0	V
Output voltage LOW at V_{OL} = 3.2 mA	V_{OL}	0	–	0.8	V
Load capacitance (note 1)	C_L	–	–	50	pF
A1/D0 to A16/D15					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	6.0	V
Output leakage current V_I = 0 to V_{DD} + 0.3 V; T_{amb} = 25 °C	I_{LO}	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2.4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3.2 mA	V_{OL}	0	–	0.4	V
Load capacitance (note 1)	C_L	–	–	200	pF
$\overline{UDS}$; R/$\overline{W}$					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	6.0	V
Output leakage current at V_I = 0 to V_{DD} + 0.3 V; T_{amb} = 25 °C	I_{LO}	−10	–	+ 10	μA
Input capacitance	C_{IN}	–	–	10	pF
Output voltage HIGH (I_{OH} = −200 μA)	V_{OH}	2.0	–	V_{DD}	V
Output voltage LOW (I_{OH} = 3.2 mA)	V_{OL}	0	–	0.8	V
Load capacitance (note 1)	C_L	–	–	200	pF

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TIMING					
Values guaranteed at 0.8 V and 2.0 V levels F6 input frequency at 7.2 MHz					
F6 (Fig. 3)					
Rise and fall times	t_r, t_f	10	–	69	ns
Frequency	f_{F6}	–	72	–	MHz
CLKO, F1/F6, R, G, B, $\overline{\text{VDS}}$, $\overline{\text{FS/DDA}}$, $\overline{\text{OD}}$ (notes 4, 5 and Fig. 6)					
CLKO HIGH time	t_{CLKH}	20	–	–	ns
CLKO LOW time	t_{CLKL}	12	–	–	ns
CLKO rise and fall times	t_{CLKr} t_{CLKf}	– –	– –	10 10	ns ns
CLKO HIGH to R, G, B, $\overline{\text{VDS}}$ floating after $\overline{\text{OD}}$ fall	t_{FOD}	0	–	30	ns
Skew between outputs R, G, B, $\overline{\text{VDS}}$	t_{VS}	–	–	20	ns
R, G, B, $\overline{\text{VDS}}$ rise and fall times	t_{Vr}, t_{Vf}	–	–	30	ns
CLKO HIGH to R, G, B, $\overline{\text{VDS}}$ active after $\overline{\text{OD}}$ rise	t_{AOD}	0	–	60	ns
F1 HIGH time (note 5)	t_{F1H}	333	417	500	ns
F1 LOW time (note 5)	t_{F1L}	333	417	500	ns
F6 HIGH time	t_{F6H}	33	69	100	ns
F6 LOW time	t_{F6L}	33	69	100	ns
$\overline{\text{OD}}$ to CLKO rise set-up	t_{ODS}	–	–	45	ns
$\overline{\text{OD}}$ to CLKO HIGH hold	t_{ODH}	–	–	0	ns
MEMORY ACCESS TIMING					
(notes 1, 6, 7 and Fig. 7)					
$\overline{\text{UDS}}$, $\overline{\text{LDS}}$, $\overline{\text{AS}}$					
Cycle time	t_{cyc}	–	417	–	ns
$\overline{\text{UDS}}$ HIGH to bus-active for address output	t_{SAA}	65	–	–	ns
Address valid set-up to $\overline{\text{AS}}$ fall	t_{ASU}	16	–	–	ns
Address valid hold from $\overline{\text{AS}}$ LOW	t_{ASH}	16	–	–	ns
Address float to $\overline{\text{UDS}}$ fall	t_{AFS}	0	–	–	ns

parameter	symbol	min.	typ.	max.	unit
$\overline{AS}$ LOW to $\overline{UDS}$ fall delay	t_{ATD}	42	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ HIGH time	t_{HDS}	180	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ LOW time (note 9)	t_{LDS}	160	–	–	ns
$\overline{AS}$ HIGH time	t_{HAS}	100	–	–	ns
$\overline{AS}$ LOW time	t_{LAS}	240	–	–	ns
Data valid set-up to $\overline{UDS}$ rise	t_{DSU}	25	–	–	ns
Data valid hold from $\overline{UDS}$ HIGH	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{AS}$ rise delay	t_{UAS}	0	–	15	ns
$\overline{AS}$ LOW to data valid	t_{AFA}	–	–	225	ns
Link-through buffers (notes 6, 7 and Fig. 8)					
$\overline{BUFEN}$ LOW to output valid	t_{BEA}	–	–	85	ns
Link-through delay time	t_{LTD}	–	–	70	ns
Input data float prior to direction change	t_{IFR}	0	–	–	ns
Output float after direction change	t_{OFR}	–	–	50	ns
Output float after $\overline{BUFEN}$ HIGH	t_{BED}	–	–	50	ns
Microprocessor READ from EUROM (Fig. 9)					
R/$\overline{W}$ HIGH set-up to $\overline{UDS}$ fall	t_{RUD}	0	–	–	ns
$\overline{UDS}$ LOW to returned-data access time	t_{UDA}	–	–	210	ns
$\overline{RE}$ LOW to returned data access time	t_{REA}	–	–	210	ns
Data valid to $\overline{DTACK}$ LOW delay	t_{DTL}	0	–	–	ns
$\overline{DTACK}$ LOW to $\overline{UDS}$ rise	t_{DLU}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	50	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	10	–	–	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	8	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ fall	t_{UDR}	0	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DSD}	–	–	260	ns
Address valid to $\overline{UDS}$ fall	t_{AUL}	0	–	–	ns

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
MEMORY ACCESS TIMING (continued)					
Microprocessor WRITE to EUROM (Fig. 10)					
Write cycle time (note 8)	t_{WCY}	500	–	–	ns
R/$\overline{W}$ LOW set-up to $\overline{UDS}$ fall	t_{WUD}	0	–	–	ns
$\overline{RE}$ LOW to $\overline{UDS}$ fall	t_{RES}	30	–	–	ns
Address valid to $\overline{UDS}$ fall	t_{ASS}	30	–	–	ns
$\overline{UDS}$ LOW time	t_{LUS}	100	–	–	ns
Data valid to $\overline{UDS}$ rise	t_{DSS}	80	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DTA}	0	–	60	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	50	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ rise	t_{UDW}	0	–	–	ns
F1/F6 to memory access cycle (Fig. 11)					
$\overline{UDS}$ HIGH to F6 (component of F1/F6) rise (notes 1, 6 and 7)	t_{UF6}	20	–	–	ns
F6 (component of F1/F6) HIGH to $\overline{UDS}$ rise	t_{F6U}	40	–	–	ns
SYNCHRONIZATION and BLANKING					
$\overline{TCS}$, SAND, $\overline{FS}$/$\overline{DDA}$					
See Fig. 12 for timing relationships and Fig. 13 for vertical sync and blanking waveforms.					

Notes to the characteristics

1. All pins are tested with a 150 pF load capacitor.
2. 16-level analogue voltage outputs.
3. Output voltage guaranteed when programmed for top level.
4. CLKO, F1/F6, $\overline{VDS}$, $\overline{FS}$/$\overline{DDA}$: reference levels = 0.8 to 2.0 V.
   R, G, B: reference levels = 0,8 to 2,0 V with V_{REF} = 2.7 V.
5. These times may momentarily be reduced to a nominal 69 ns in slave-sync mode at the moment of re-synchronization.
6. Reference levels = 0.8 to 2.0 V.
7. F6 input at 6 MHz.
8. Microprocessor write cycle times of less than 500 ns are permitted but often result in Wait States being generated, the precise timing of $\overline{DTACK}$ will then depend on the internal synchronization time
9. This timing may be infringed at the beginning and end of the memory access window.
10. Output voltage guaranteed when programmed for bottom level.

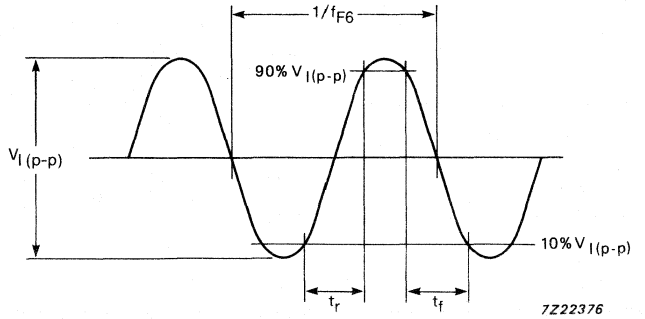


Fig. 3 F6 input waveform.

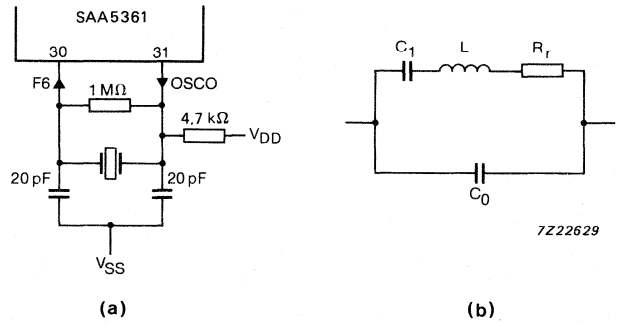


Fig. 4(a) Oscillator circuit for SAA5361 stand-alone sync mode and (b) equivalent circuit of crystal at resonance (see **characteristics** for values).

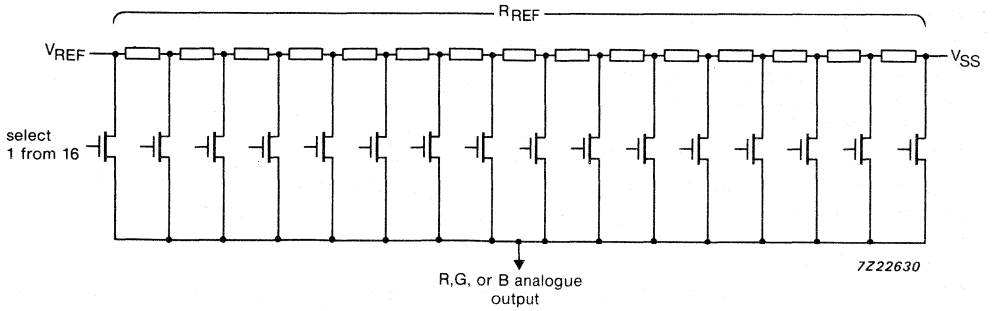


Fig. 5 Circuit arrangement giving one-of-sixteen reference voltage levels for the R, G or B analogue outputs.

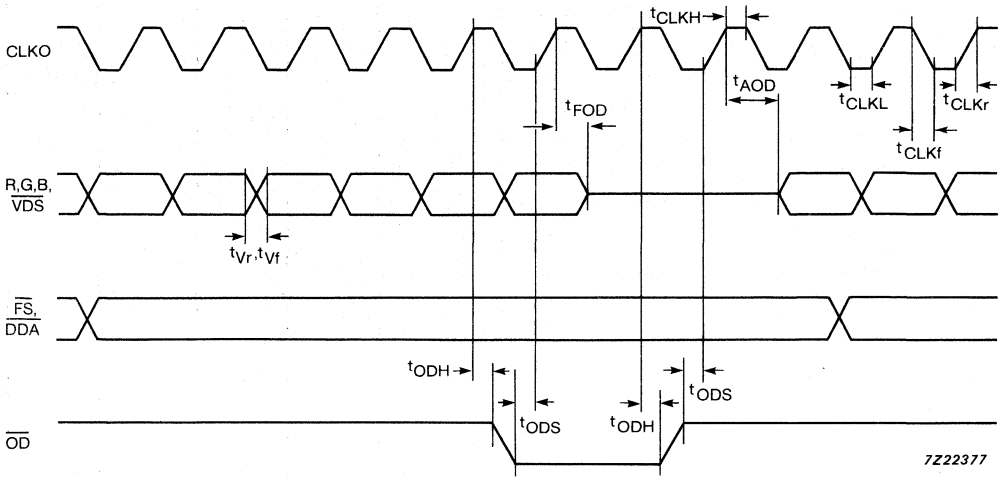


Fig. 6 Video timing.

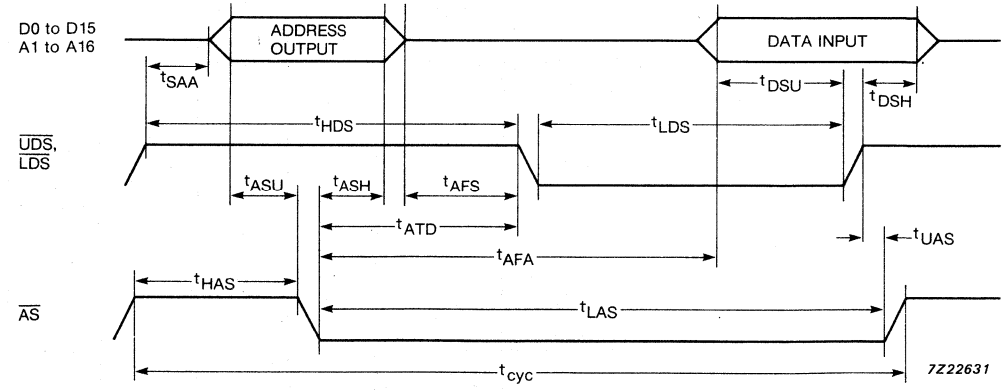


Fig. 7 Memory access timing.

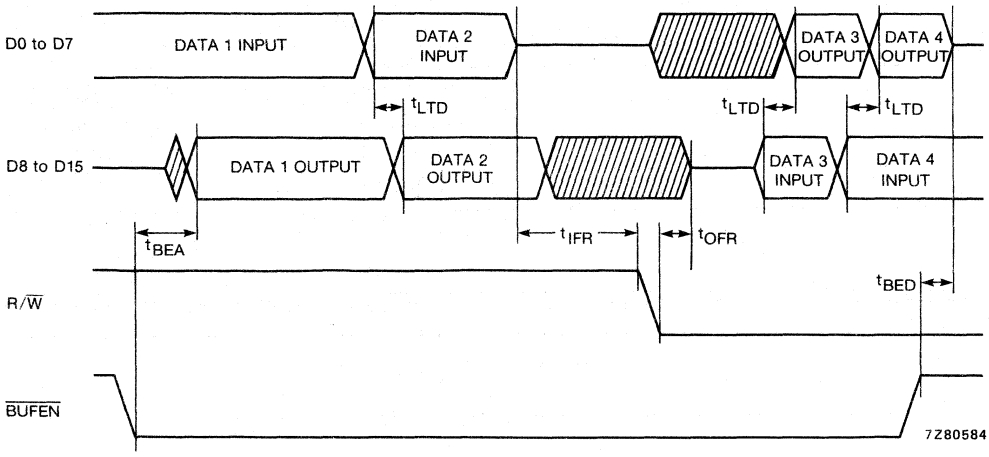


Fig. 8 Timing of link-through buffers.

DEVELOPMENT DATA

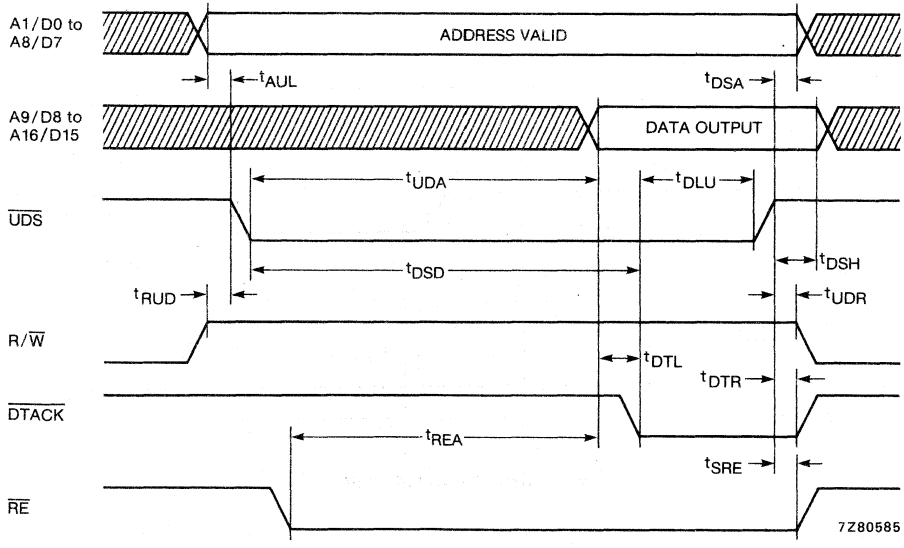


Fig. 9 Timing of microprocessor read from EUROM.

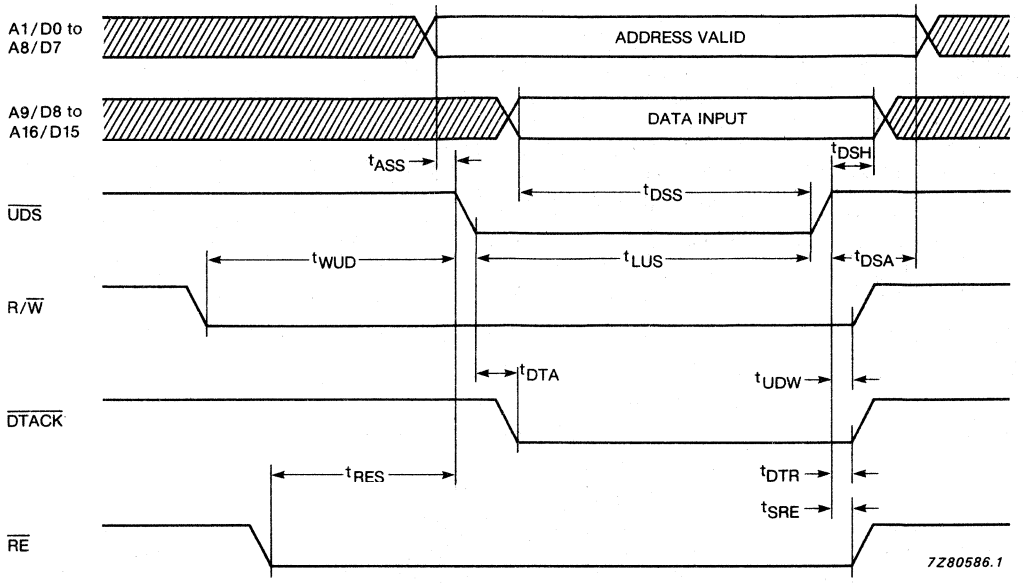


Fig. 10 Timing of microprocessor write to EUROM.

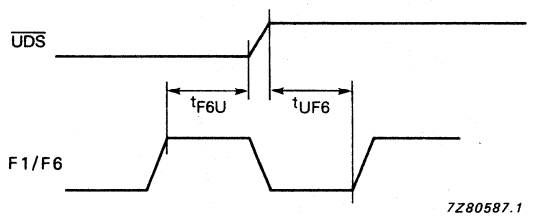


Fig. 11 Timing of F1/F6 to memory access cycle.

DEVELOPMENT DATA

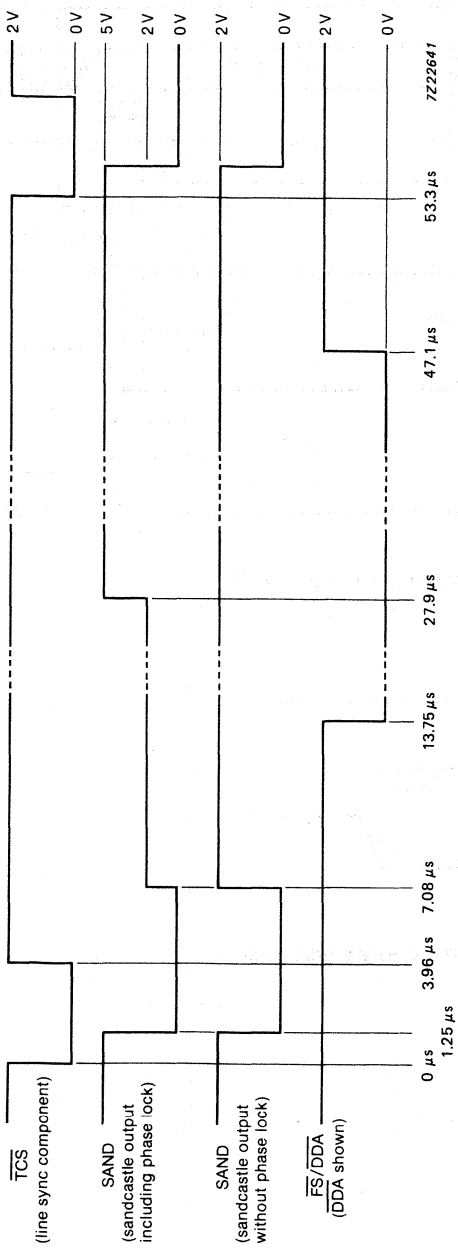


Fig. 12 Timing of synchronization and blanking outputs; all timings are nominal and assume f_{F6} = 7.2 MHz.

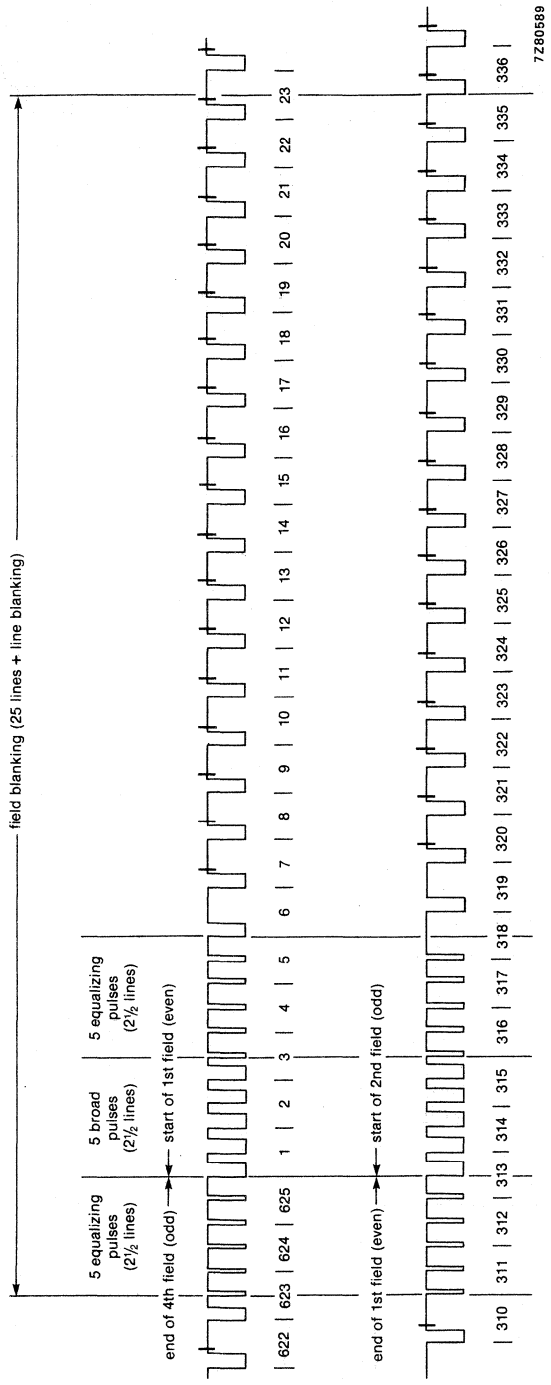


Fig. 13 Vertical synchronization and blanking waveforms; separation of broad pulses = 3.96 μs; equalizing pulse widths = 7.88 μs.

APPLICATION INFORMATION

More detailed application information is available on request

BASIC VIDEOTEX DECODER CONFIGURATION

A basic, practical decoder configuration is shown in Fig. 14, reference should also be made to the block diagram Fig. 1.

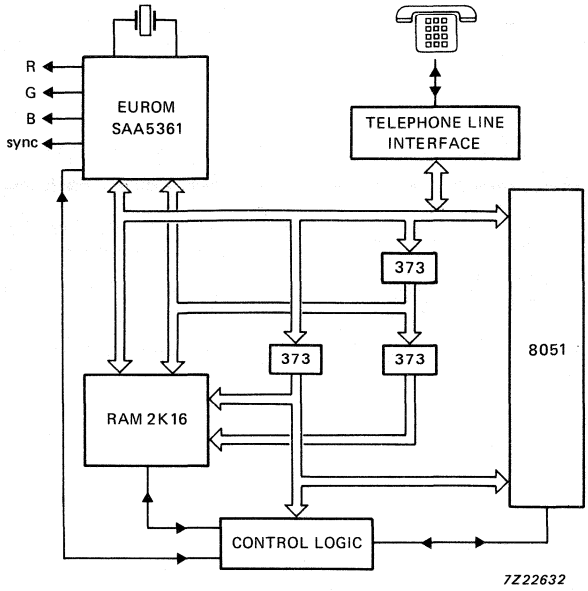


Fig. 14 Basic videotex decoder configuration.

Character and attribute data is fetched from the external memory, processed by the row buffer fill logic according to the stack coding scheme (in stack mode) and then fed into one half of the dual display row buffer. The data fetch process takes place during one line-flyback period (per row) and, since time is required to complete the fill, the other half of the dual row buffer is used for display. The row buffers exchange functions on alternate rows – each holds the 40 columns of 32 bits required to define explicitly every character in a row.

The addresser is used for row buffer filling and for fetching screen colours, and during the display time it is also used for addressing DRCS characters.

Timing

The timing chain operates from an external 7.2 MHz clock or an on-chip fixed-frequency crystal oscillator. The basic video format is 40 characters per row, 24/25 rows per page and 10 video lines per row. EUROM will also operate with 20/21 rows per page and 12 video lines per row. The two extra lines per row are added symmetrically and contain background colour only for ROM-based alpha-numeric characters. DRCS characters, block and smooth mosaics and line drawing characters occupy all 12 lines.

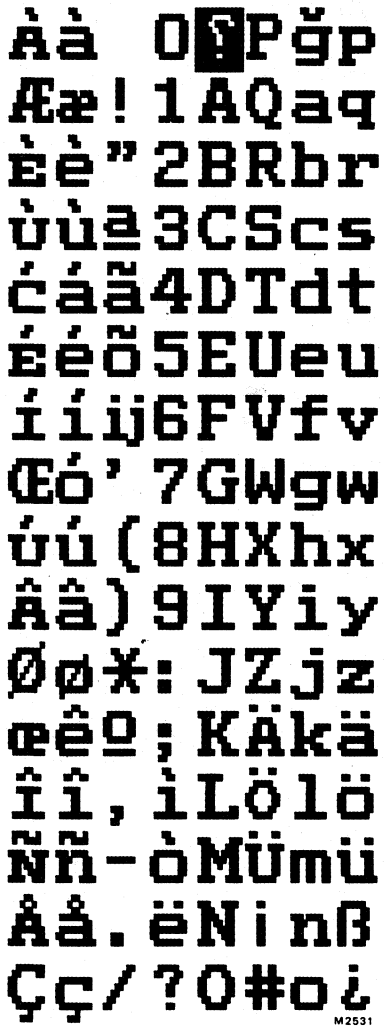
The display is generated to 625-line/60 Hz scanning (interlaced or non-interlaced).
In addition to composite sync (pin 32) for conventional timebases, a clock output at 1.2 MHz or 7.2 MHz (pin 29) is available for driving other videotex devices, and a 14.4 MHz clock (pin 27) is available for hard-copy dot synchronization. A defined-display-area timing signal (pin 33) simplifies the application of external peripherals such as a light pen; this signal is nominally coincident with the character dot information.

DEVELOPMENT DATA

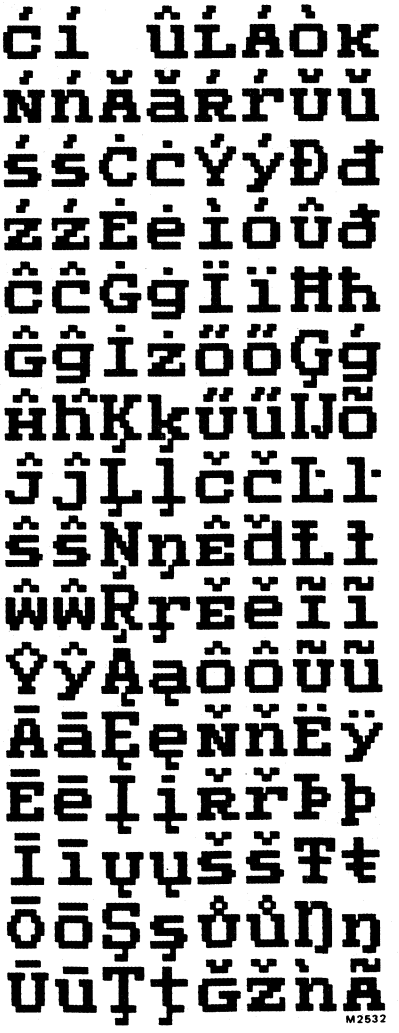
APPLICATION INFORMATION (continued)

Character generation

EUROM supports eight character tables, each of (nominally) 128 characters. Four tables are in on-chip ROM and contain fixed characters and four are stored in an external RAM. The contents of the fixed character tables (Tables 0 to 3) are shown in Figs 15 and 16.

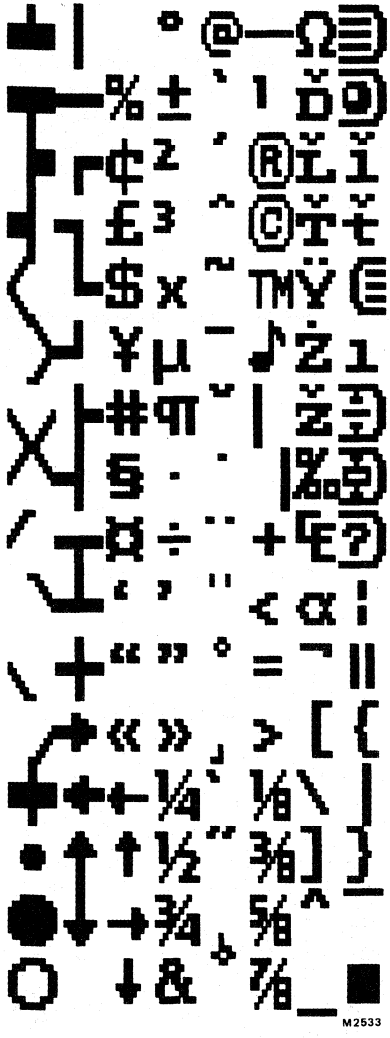


(a)

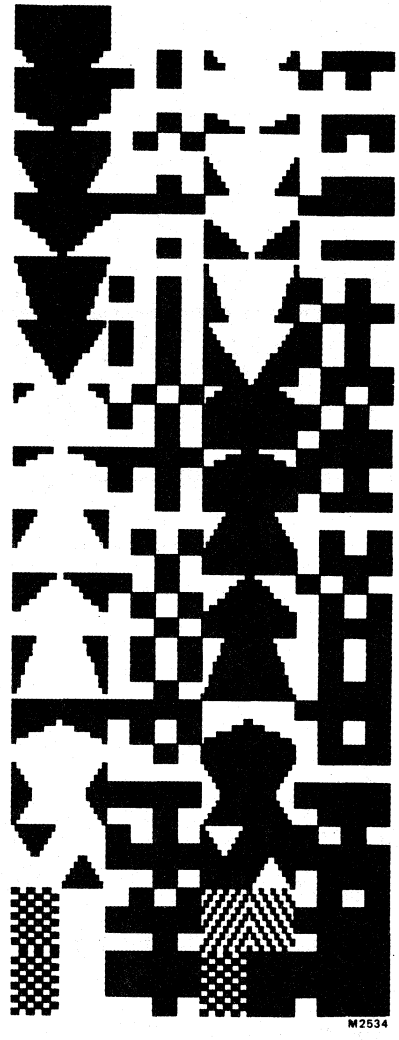


(b)

Fig. 15 On-chip characters: (a) Table 0; (b) Table 1.



(a)



(b)

Fig. 16 On-chip characters: (a) Table 2; (b) Table 3.

APPLICATION INFORMATION (continued)

Character generation (continued)

The 128 most commonly used characters are contained in Table 0, these are the standard upper and lower-case letters of the Roman alphabet, numerals, punctuation and the more common accented characters. In normal text transmission, Table 0 is used most of the time. Table 1 contains other accented characters. Miscellaneous characters, mathematical symbols, the line drawing character set and accents without associated symbols are contained in Table 2. Table 3 contains the block mosaics for the basic alpha-mosaic service and also the new smooth mosaics.

The four tables stored in the external RAM (Tables 4 to 7) are used for DRCS.

Scroll map

The scroll map uses a 26-byte area of on-chip RAM and functions in association with the timing chain. It maps the scan row on to the fetched memory row so allowing the stored page to be displayed in any row order. For each row, a 1-byte pointer to the display memory row is stored in the scroll map. This allows scrolling without the need for data transfer to, or from, side storage.
Additional control bits are stored, allowing 1 to 25 rows to be displayed at any location on the screen.

Colour map and digital-to-analogue converters

The colour map RAM contains thirty-two 12-bit words that are loaded by the microprocessor and read out in three 4-bit groups at pixel rate. Each group is fed to a non-linear (gamma-corrected) D-A converter. The resulting R, G and B outputs are low-impedance with peak-to-peak amplitudes controlled by the reference voltage applied at pin 21.

Cursor

The cursor is available in the stack mode. Its position, character code, character table, foreground colour, background colour, lining and flash attributes are all software programmable via internal register bits.

NON-VIDEOTEX APPLICATIONS

For non-Videotex applications, the device will also support the following operating modes:

Explicit fill mode. An alternative 40 character/rows mode which does not use the memory compression technique of stack coding. More display memory is required but there are no limitations on the number of display attribute changes per row.

80 characters/rows mode. When operating with 80 characters per row, the available display attributes are eight foreground colours, eight (potentially different) background colours (including transparent) as well as underline and blink.

Full field DRCS mode. This mode is not mutually exclusive to the explicit fill and 80 characters/rows modes but rather the available DRCS memory is expanded so that the whole screen can be covered, thus enabling a 'bit map'. All ROM-based characters and all display attributes remain available.

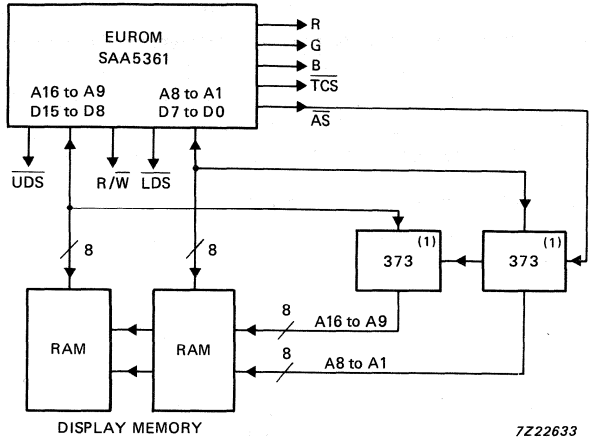
MICROPROCESSOR and RAM BUS INTERFACE

Three types of data transfer take place at the bus interface:

- EUROM fetches data from the display memory
- The microprocessor reads from, or writes to, EUROM's internal register map
- The microprocessor accesses the display memory

EUROM access to display memory (Figs 17 and 18)

EUROM accesses the external display memory via a 16-bit multiplexed address and data bus with a cycle time of 417 ns. The address strobe ($\overline{AS}$) signal from EUROM flags the bus cycle and writes the address into octal latches (74LS373). The display data is stored in bytes of upper (most-significant) and lower (least-significant) display information and is always fetched in pairs of bytes (upper + lower = 16 bits). The upper and lower display RAM sections are enabled simultaneously by the upper and lower data strobes (respectively $\overline{UDS}$ and $\overline{LDS}$) which are always asserted together to fetch a 16-bit word. The read/write control R/$\overline{W}$ is included although EUROM only reads from the display memory.



(1) 74LS373 octal transparent latch (3-state)

Fig. 17 Simple RAM interface circuit for display memory access.

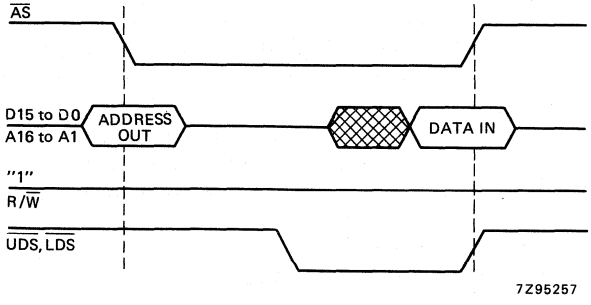


Fig. 18 Bus timing for display memory access.

APPLICATION INFORMATION (continued)

EUROM access to display memory (continued)

The display memory organization uses the word/byte addressing convention adopted for the SCN68000 microprocessor series. Data fetched on the 16-bit bus is considered in terms of bytes where the even numbered bytes use the upper (most-significant) part of the bus as shown in Fig. 19. The word addresses are numerically the same as the upper byte that they contain — there are no odd-numbered word addresses.

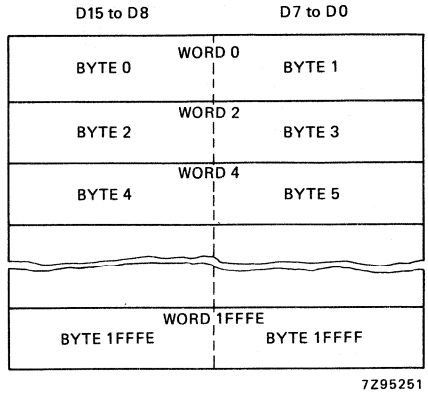


Fig. 19 Display memory word/byte organization.

Warning time

As EUROM is a real-time display device, it must have direct access to the display memory with priority over the microprocessor and other peripheral devices. This is achieved by EUROM issuing a bus request ($\overline{BR}$) signal for the duration of the memory access plus a programmable advance warning time which allows the microprocessor to complete its current bus cycle.

In systems where the buses of the microprocessor and EUROM are intimately connected (connected systems), $\overline{BR}$ may be used to suspend all microprocessor activity so that EUROM can act as a dedicated DMA controller. In systems where the two buses are separated by buffers (disconnected systems), $\overline{BR}$ may be used either to generate an interrupt or as a direct signal. To these ends, the warning time between the assertion of $\overline{BR}$ and the beginning of EUROM's bus activity is programmable to be between 0 and 19.2 μs.

Microprocessor access to register map

EUROM has a set of internal registers which, when memory-mapped, behave as an 8-bit wide RAM connected to the upper part of the data bus (Fig. 20). The control signals $\overline{UDS}$ and R/$\overline{W}$ are reversed to become inputs and the register map is enabled by the signal $\overline{RE}$. Addresses are input via the lower part of the bus. A data transfer acknowledge signal ($\overline{DTACK}$) indicates to the microprocessor that the data transfer is complete.

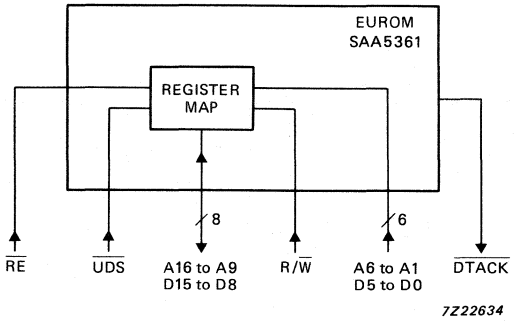


Fig. 20 Microprocessor access to register map.

The main data and address paths used in a connected 68000 interface are shown in Fig. 21. The outputs from the octal latches (74LS373) are enabled only when the 68000 has made the bus available in response to a bus request ($\overline{BR}$). When the register map is accessed data is transferred via the upper part of the bus and the microprocessor's low-order address is passed to EUROM via the octal buffers (74LS244). At the same time the bidirectional buffers (74LS245) disable the signals from the low order data bus of the 68000.

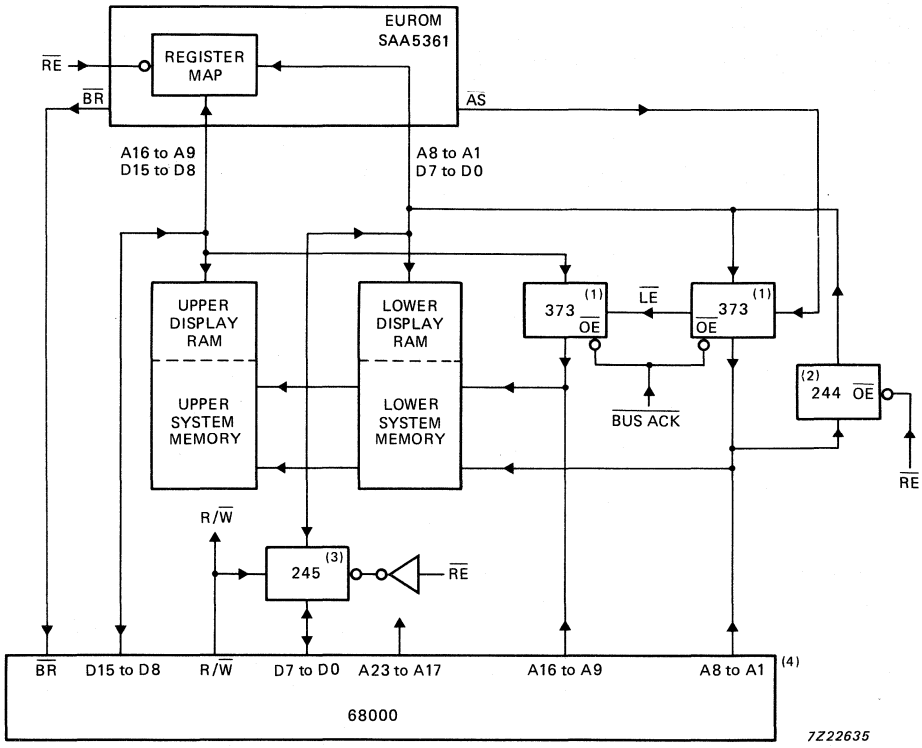
The buffers '244 and '245 may be omitted in a 16-bit write-only configuration where the least-significant data byte is interpreted by EUROM as an address. Here it will generally be necessary for the microprocessor to hold a (readable) 'master copy' of EUROM's scroll map contents at a location in its main memory.

8-bit microprocessors

Although the control bus is optimised for the SCN68000 16-bit microprocessor unit, EUROM will operate with a number of widely differing industry-standard 8, 16 or more-bit microprocessors or microcontrollers (e.g. SCN68008, MAB8051). The interfacing of 8-bit microprocessors to the 16-bit wide display memory is made simple by EUROM's on-chip link-through buffer which provides the microprocessor with bidirectional access to the lower (odd) half of the memory. The link-through buffer is enabled by the buffer-enable signal $\overline{BUFEN}$, and the send/receive direction is controlled by the signal $\overline{S}$/R.

The main data and address paths used in a connected 8-bit microprocessor system are shown in Fig. 22. The interface is similar to that of the 16-bit system but here the display memory does not receive A0 as an address, rather A0 is used as the major enabling signal for $\overline{BUFEN}$ (enables when HIGH).

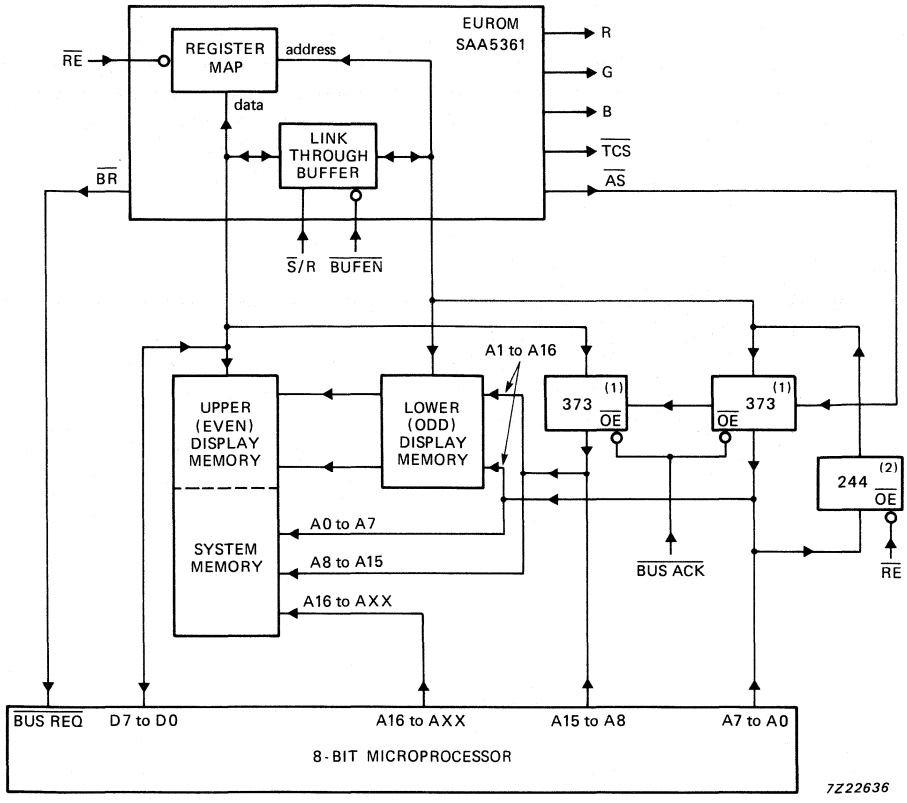
APPLICATION INFORMATION (continued)



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 74LS245 octal bus transceiver (3-state)
(4) SCN68000 microprocessor unit

Fig. 21 Connected 16-bit microprocessor system.

DEVELOPMENT DATA



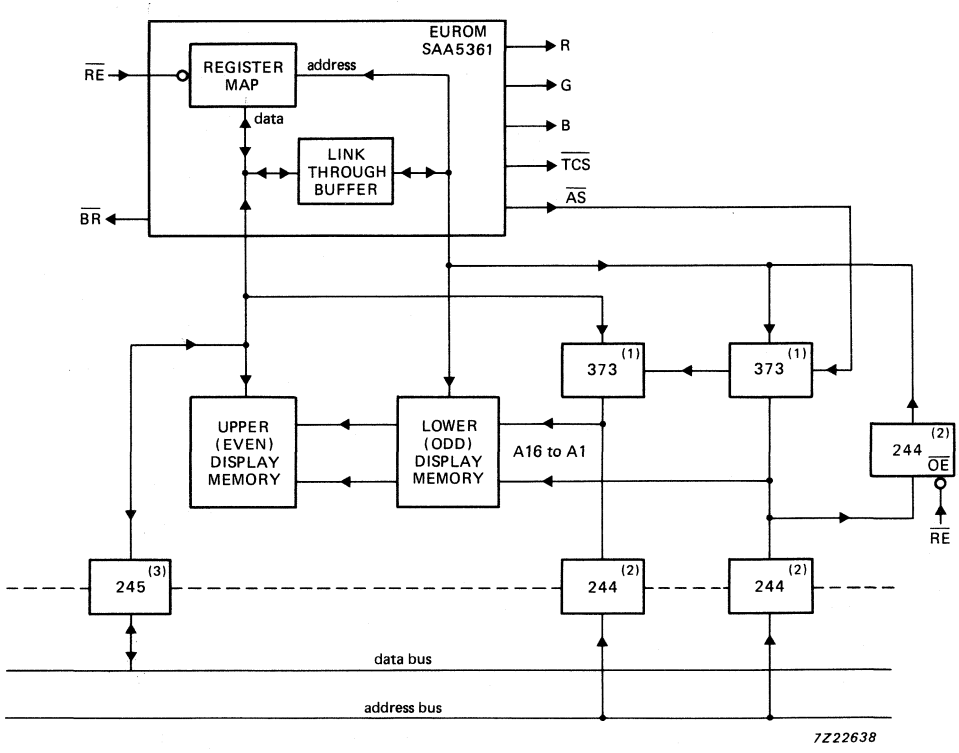
(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)

Fig. 22 Connected 8-bit microprocessor system.

APPLICATION INFORMATION (continued)

Disconnected systems

For many applications it may be desirable to disconnect EUROM and the display memory from the microprocessor and its ROM, RAM and other peripherals by using isolating buffers as shown in Fig. 23. The two parts of the system then operate independently and communicate only when the microprocessor accesses EUROM's register map or the display memory.



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 75LS245 octal bus transceiver (3-state)

Fig. 23 Disconnected 8-bit system.

DEVELOPMENT DATA

Synchronization

Stand-alone mode

As a stand-alone device (e.g. in terminal applications) EUROM can output a composite sync signal ($\overline{TCS}$) to the display timebase IC or to a monitor. Timing is obtained from a 7.2 MHz on-chip oscillator using an external crystal as shown in Fig. 24.

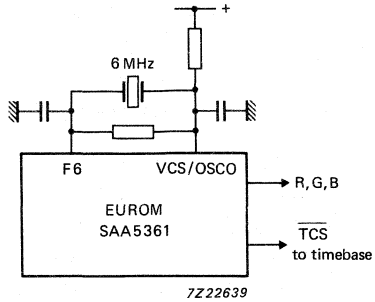


Fig. 24 Stand-alone synchronization mode.

Simple-slave

In the simple-slave mode EUROM synchronizes directly to another device, such as to the $\overline{TCS}$ signal from another EUROM as shown in Fig. 25. EUROM's horizontal counter is reset by the falling edge of $\overline{TCS}$. A dead time of 208 ns is built in to avoid resetting the counter at every tv line and so prevents screen jitter.
Field synchronization is made using EUROM's internal field sync separator.

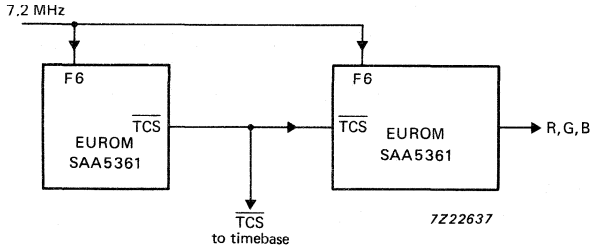


Fig. 25 Simple-slave (direct sync) mode.

APPLICATION INFORMATION (continued)

Synchronization (continued)

Phase-locked slave

The phase-locked slave (indirect sync) mode is shown in Fig. 26. Part of a VIP2 forms alu. When EUROM is active, its horizontal counter forms part of the phase control loop — a horizontal reference is fed back to the VIP2 from the SAND output and a vertical reference is generated by feeding separated composite sync to EUROM's field sync separator via the VCS input. In the phase-locked slave mode, the display derived from EUROM can sync with that from a tv source or a local VLP player, thus giving picture-in-text display possibilities.

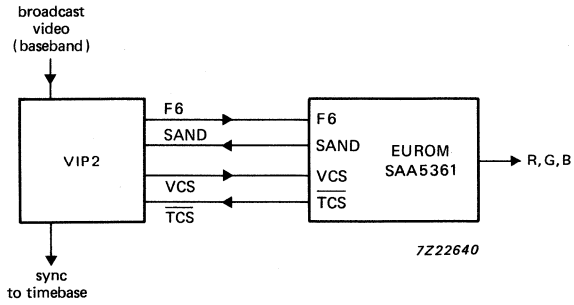


Fig. 26 Phase-locked slave (indirect sync) mode.

Data sheet	
status	Preliminary specification
date of issue	January 1992

SAA5370
Dual port controller for EUROM, with two UARTs (EASI)

FEATURES

- The CMOS circuit SAA5370 connects EUROM, display RAM, microprocessor, keyboard, modem and scratch pad RAM
- Optional EUROM mode or dual port mode
- Maximum 128 kbyte display RAM
- Suitable for 16-bit or 8-bit microcomputers
- Microprocessor interface handles the multiplexed 16-bit address/ 8-bit data bus
- Demultiplexer for address/data bus
- Various controls to extend EPROM and display RAM address ranges
- Internal generation of microprocessor clock and EUROM clock
- Two separate UARTs with baud rates up to 19200 1/s
- Various port outputs to support external switching dependent on read and write controls
- Interrupt controller for six interrupt sources with different priority levels
- 16-bit timer/counter for general use
- Internal control register with address range from FF00 to FFFF
- No external components, small power consumption.

GENERAL DESCRIPTION

Economic microprocessor interface, suitable for EUROM and display RAM applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage (pins 10, 39, 81)	4.75	5	5.25	V
I_{DD}	total supply current	-	-	120	mA
V_{IL}	data, address and control input voltage LOW	0	-	0.8	V
	reset input voltage LOW	0	-	0.6	V
V_{IH}	data, address and control input voltage HIGH	2	-	V_{DD}	V
	reset input voltage HIGH	2.4	-	V_{DD}	V
V_{OL}	data, address and control output voltage LOW	-	-	0.4	V
V_{OH}	data, address and control output voltage HIGH	2.4	-	-	V
f_{OSCI}	maximum input clock frequency	-	24.0	28.8	MHz
T_{amb}	operating ambient temperature range	0	-	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5370	120	QFP	plastic	SOT220B

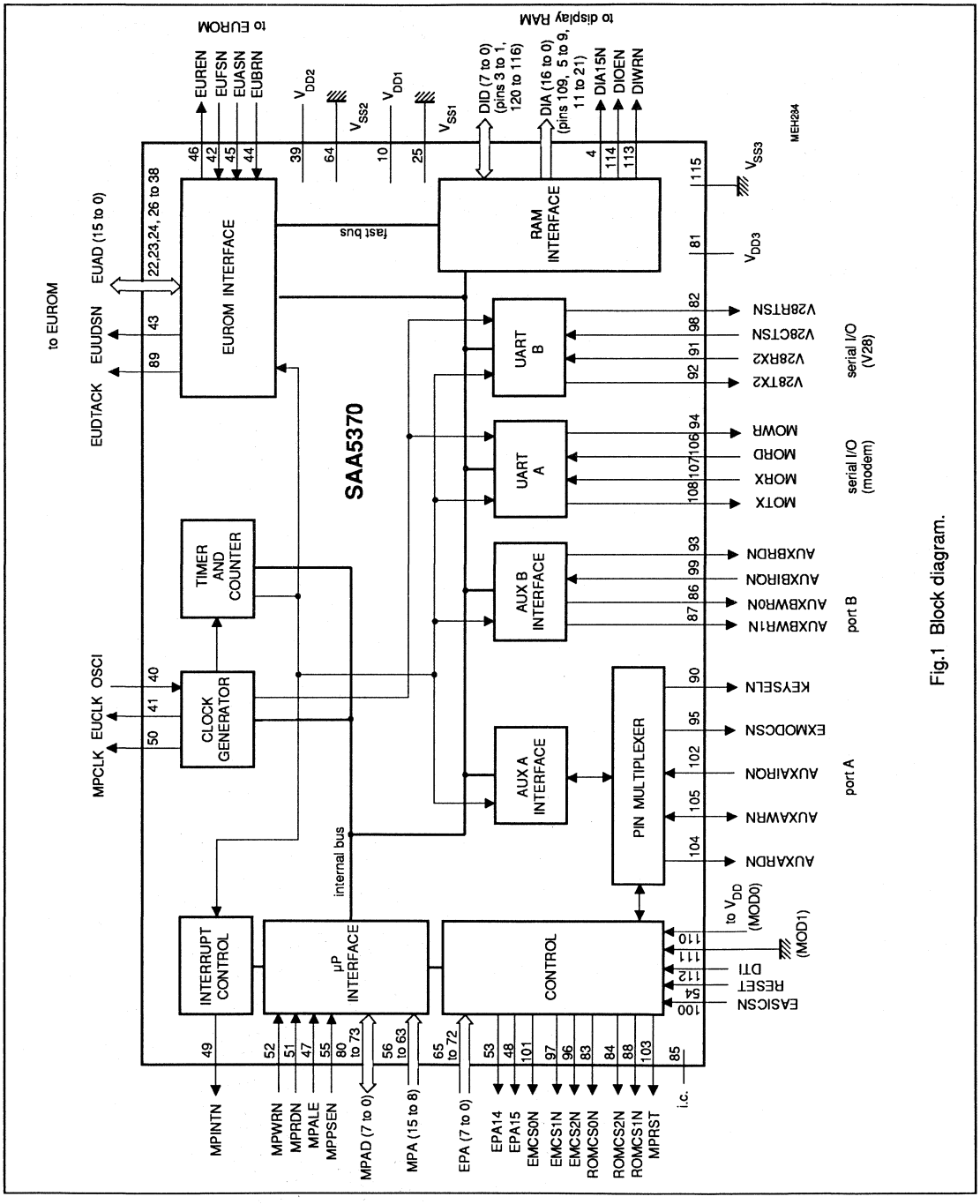


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	STATUS	DESCRIPTION
DID5	1	I/O	8-bit display RAM data input/output (bits 7 to 5)
DID6	2	I/O	
DID7	3	I/O	
DIA15N	4	O	inverted display RAM address output (bit 15); Fig.4
DIA15	5	O	16-bit display RAM address output (bits 15 to 11)
DIA14	6	O	
DIA13	7	O	
DIA12	8	O	
DIA11	9	O	
V_{DD1}	10	-	+5 V supply voltage 1
DIA10	11	O	16-bit display RAM address output (bits 10 to 0)
DIA9	12	O	
DIA8	13	O	
DIA7	14	O	
DIA6	15	O	
DIA5	16	O	
DIA4	17	O	
DIA3	18	O	
DIA2	19	O	
DIA1	20	O	
DIA0	21	O	
EUAD15	22	I/O	16-bit address and 8-bit data bus to EUROM output (bits 15 to 13)
EUAD14	23	I/O	
EUAD13	24	I/O	
V_{SS1}	25	-	GND1 (0 V)
EUAD12	26	I/O	16-bit address and 8-bit data bus to EUROM output (bits 12 to 8)
EUAD11	27	I/O	
EUAD10	28	I/O	
EUAD9	29	I/O	
EUAD8	30	I/O	

SYMBOL	PIN	STATUS	DESCRIPTION
EUAD7	31	I/O	16-bit address and 8-bit data bus to EUROM output (bits 7 to 0)
EUAD6	32	I/O	
EUAD5	33	I/O	
EUAD4	34	I/O	
EUAD3	35	I/O	
EUAD2	36	I/O	
EUAD1	37	I/O	
EUAD0	38	I/O	
V_{DD2}	39	-	+5 V supply voltage 2
OSCI	40	I	system clock signal input (24 MHz for 50 Hz system; 28.8 MHz for 60 Hz system)
EUCLK	41	O	clock output to EUROM (6 MHz for 50 Hz system; 7.2 MHz for 60 Hz system)
EUFSN	42	I	field sync signal from EUROM (active-LOW)
EUUDSN	43	I/O	upper data strobe signal to/from EUROM
EUBRN	44	I	bus request signal from EUROM (active-LOW)
EUASN	45	I	address strobe signal from EUROM (active-LOW)
EUREN	46	O	register enable signal to EUROM (active-LOW)
MPALE	47	I	microprocessor address latch enable input (active-HIGH)
EPA15	48	O	EPROM mapping address output to extend ROM (bit 15)
MPINTN	49	O	interrupt to microprocessor
MPCLK	50	O	clock output signal to microprocessor (Table 3; register ..FF)
MPRDN	51	I	read data bus control from microprocessor (active-LOW)
MPWRN	52	I	write data bus control from microprocessor (active-LOW)
EPA14	53	O	EPROM mapping address output to extend ROM (bit 14)
RESET	54	I	reset input (active-HIGH)
MPPSEN	55	I	program store enable input from microprocessor
MPA15	56	I/O	16-bit microprocessor address bus (bits 15 to 11)
MPA14	57	I/O	
MPA13	58	I/O	
MPA12	59	I/O	
MPA11	60	I/O	

SYMBOL	PIN	STATUS	DESCRIPTION
MPA10	61	I/O	16-bit microprocessor address bus (bits 10 to 8)
MPA9	62	I/O	
MPA8	63	I/O	
V_{SS2}	64	-	GND2 (0 V)
EPA7	65	I/O	8-bit latched lower address bus (bits 7 to 0)
EPA6	66	I/O	
EPA5	67	I/O	
EPA4	68	I/O	
EPA3	69	I/O	
EPA2	70	I/O	
EPA1	71	I/O	
EPA0	72	I/O	
MPAD0	73	I/O	multiplexed data/address bus from/to microprocessor
MPAD1	74	I/O	
MPAD2	75	I/O	
MPAD3	76	I/O	
MPAD4	77	I/O	
MPAD5	78	I/O	
MPAD6	79	I/O	
MPAD7	80	I/O	
V_{DD3}	81	-	+5 V supply voltage 3
V28RTSN	82	O	UART-B output ready to send for V28 (active-LOW)
ROMCS0N	83	I/O	EPROM chip select default output (active-LOW); Fig.5
ROMCS2N	84	I/O	EPROM chip select mapped output (active-LOW); Fig.5
i.c.	85	-	internally connected
AUXBWR0N	86	O	port output active-LOW at write; ports AUX-B
AUXBWR1N	87	O	
ROMCS1N	88	I/O	EPROM chip select mapped output (active-LOW); Fig.5
EUDTACK	89	O	data acknowledge signal to EUROM
KEYSELN	90	O	keybord select control output (port output active-LOW at read and write)

SYMBOL	PIN	STATUS	DESCRIPTION
V28RX	91	I	serial data input from V28
V28TX	92	O	serial data output to V28
AUXBRDN	93	O	port output active-LOW at read ; port AUX-B
MOWR	94	O	UART-A ready to send output for modem (active-HIGH)
EXMODCSN	95	O	AUX-A output to select modem chip (port output active-LOW at read and write)
EMCS2N	96	O	extended memory chip select output (bit 2); Fig.4
EMCS1N	97	O	extended memory chip select output (bit 1); Fig.4
V28CTSN	98	I	control input clear to send V28 (active-LOW)
AUXBIRQN	99	I	AUX-B port interrupt request (active-LOW); AUXB-bit in registers ..FB and ..FA
EASICSN	100	I	device chip select input (active-LOW)
EMCS0N	101	O	extended memory chip select output (bit 0); Fig.4
AUXAIRQN	102	I	AUX-A port interrupt request input (active-LOW); AUXA-bit in registers ..FB and ..FA
MPRST	103	O	microprocessor reset output
AUXARDN	104	O	AUX-A read strobe output; port output active-LOW at read
AUXAWRN	105	O	AUX-A write strobe output; port output active-LOW at write
MORD	106	I	control input modem clear to send (UART-A)
MORX	107	I	serial data input from modem (UART-A)
MOTX	108	O	serial data output to modem (UART-A)
DIA16	109	O	17-bit display RAM address; Fig.4
MOD0	110	I	mode pin connected to V_{DD}
MOD1	111	I	mode pin connected to GND
DTI	112	I	data test input connected to ground
DIWRN	113	O	write control to display RAM ; active-LOW for write/read HIGH
DIOEN	114	O	enable control to display RAM (enable = LOW)
V_{SS3}	115	-	GND3 (0 V)
DID0	116	I/O	8-bit display RAM data input/output (bits 4 to 0)
DID1	117	I/O	
DID2	118	I/O	
DID3	119	I/O	
DID4	120	I/O	

PIN CONFIGURATION

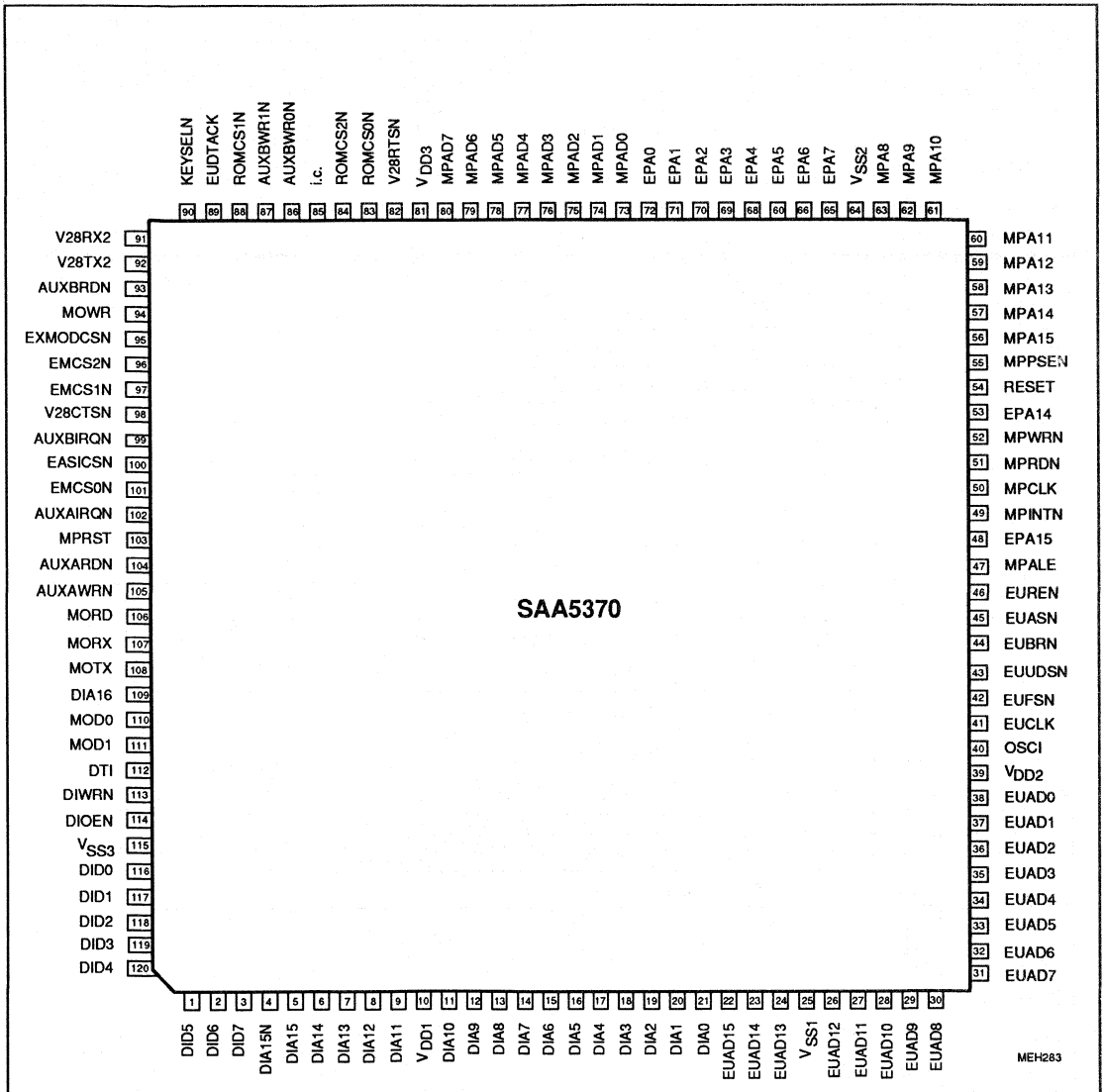


Fig.2 Pin configuration.

Dual port controller for EUROM with two UARTs (EASI)

SAA5370

FUNCTIONAL DESCRIPTION

The SAA5370 connects EUROM (optionally a second microprocessor in dual processor mode), display RAM with maximum 128 kbyte, microprocessor, keyboard, modem and scratch pad RAM. Chip select outputs are provided to enable extended memories, printer, RAM, modem and keyboard. The processor writes, after each hardware reset, data to 8-bit internal control registers (Tables 2 and 3) to select the different functions. The processor can read the status bytes. The registers are connected to the lower 8-bit data bus of the host processor. The SAA5370 supports the 8031 software.

Microprocessor interface

The microprocessor interface connects 8-bit or 16-bit processors to the circuit, and it provides all relevant signals due to processor memory operations. The strobed 8-bit address of the multiplexed address/data bus is demultiplexed and transferred to the EPROM interface.
The 16-bit address of the microprocessor is catched with the falling edge of MPALE.The lower Byte of the 16-bit address is fed via the internal address bus to the EUROM port . Data is latched in an 8-bit/16-bit data register (read/write). All signals are synchronized by the master clock, that achieves different timings dependent on the applied microprocessor type. Signals are switched according to the operation modes.

Control unit

Programmable registers control the functions (Tables 2 and 3). The registers are written or read by the host microprocessor as described previously. Programmable are: the UARTs A and B, the timer and counter and the interrupt vectors. The system command bytes ..FF and ..FE have to be programmed after reset. The initial start address is then FF00. In this stand-by mode all 3-state outputs are in the high-ohmic state. The initial state of the registers is zero. Programming selects the interfaces, sets the clock signal dividers and configures the pins.

The SAA5370 starts its operation after MRRST = HIGH.

Clock generation

An external crystal oscillator signal provides the SAA5370 on pin 40 (OSCI) with a 24 MHz clock signal in 50 Hz mode (28.8 MHz in 60 Hz mode). The EUROM clock frequency is EUCLK = OSCI/4; the microprocessor clock MPCLK is programmable by the bits PCK2 to PCK0 and FSR of the register ..FF (Table 3). The FRS-bit sets 50/60 Hz mode and switches the baud rate prescaler (after reset: FRS, CLK2 and CLK 1 = 0; CLK0 = 1).
A third clock signal supplies the serial interfaces UART-A and UART-B. The baud rate clock BRCLK = OSCI/50 (respectively OSCI/60) is generated to achieve 480 kHz. The reset sets a default value of MPCLK = EUCLK/2. The host processor then initialises the system by writing the command register bytes ..FF and ..FE.
The baud generator sample rate is f_S = 25 x baud rate.

The allowable dual phase shift keying DPSK due to 50/60 Hz refers to the bit period and achieves the accuracy of locating the middle of the bit A. With A = 2% the resulting maximum bit distortion is E_{dist} = 48% (the "Bundespost" allows maximum A = 10%).

UARTs

Serial data transmission with baud rates of Table 1 can be obtained by means of UART-A and UART-B. The UART-A is pre-determined for an external modem. The data format is: start bit, 8-bit data word and stop bit. The command and status register Byte ..EE sets the baud rate, enables the interrupts and controls the second hand-shake. The status bits indicate a full receiver, an empty transmitter or a received error condition. The logical status on the receiver and hand-shake pins is reflected in the status byte.

Auxiliary port controls AUXA and AUXB

These output signals support external system switching dependent on read and write control and the addressing of the host microcomputer. The outputs are active-LOW at write

output	pin	at address
AUXBWR1N	87	DF to D8
AUXBWR0N	86	D7 to D0
AUXAWRN	105	CF to C8

The outputs are active-LOW at read

output	pin	at address
AUXBRDN	93	DF to D0
AUXARDN	104	CF to C8

The outputs are active-LOW at write and read:

output	pin	at address
EXMODCSN	95	C7 to C0
KEYSELN	104	BF to B8

Table 1 Generated baud rates

BAUD RATE	SAMPLE RATE	SAMPLE PERIOD	DPSK
19200	BRCLK	2.1 µs	1 µs
9600	BRCLK/2	4.2 µs	2 µs
4800	BRCLK/4	8.3 µs	4 µs
2400	BRCLK/8	16.6 µs	8 µs
1200	BRCLK/16	33.3 µs	16 µs
300	BRCLK/64	133.3 µs	64 µs
75	BRCLK/256	533.3 µs	256 µs

Interrupt request inputs (active-LOW) for ports B and A:

AUXBIRQN, pin 99

AUXAIRQN, pin 102

Interrupt controller

The interrupt controller handles six sources (Table 3) with different priority levels. The operation is determined by programmable registers. Interrupt status bits are reflected in the interrupt request register ..FA; these bits are also available in each of the individual on chip facility status registers. The individual interrupt enable bits are combined with the main interrupt enable bit (ENINT) to disable all interrupts by means of one bit only (ENINT-bit = 0; interrupts enabled).

Internal masks are provided for all input/output facilities. The host processor finds out by reading the status byte (..FB) which of the interrupts are active. The processor can also write an interrupt acknowledge, then an interrupt vector is provided. The interrupt command register(..F9) determines the upper four bits of the interrupt vector to disable all interrupts and to reset the interrupt bits. The two bytes (two byte step) of the interrupt vector are apart . The register content is divided into a read-only part (RINT-bits) and a read/write part (OVEC-bits). The RINT-bits flag which of the interrupts has issued a request.

The general operation of the interrupt control depends on the selected mode and control bit (PX2 in ..FE register).
An acknowledge cycle is performed by reading the interrupt vector register ..F9. This register is updated with the current vector for highest priority interrupt (provided by the host processor) when a real cycle starts. The interrupt request output MPINTN is set HIGH (inactive) by a L/H transition of the read signal. The next pending or incoming interrupt is issued if "acknowledge-only" mode is set (PX2-bit = 0). An interrupt has to be terminated by writing into the service register ..FB, if the "end of interrupt" mode is set (PX2-bit = 1). A new or a pending interrupt issues only after writing the service register ..FB (the data written is irrelevant).

Timer/counter

A 16-bit timer is provided for general use. Interrupts are generated at program intervals in the timer mode. Clock period measurements are done in the counter mode. The 4-bit prescaler can be programmed to achieve a larger timer/counter frequency range. The timer/counter is controlled by the command Byte ..F0.

Timer mode:
The timer input is connected to one of the basic clocks of the clock generator. The timer is preset to any value. A maskable interrupt can be initiated at timer underflow state. Then, the preset value is automatically reloaded, and the timer continues.

Counter mode:
This mode is selected by the TCC-bit of the Byte ..FO. TTCC = 1 converts the timer into an 8-bit period counter. The preset-LOW byte ..F1 is used as a programmable prescaler. The counter measures the programmed period of the signal on pin 107 (MORX) with 8-bit disbandment by sampling it with the pre-scaled clock. The result is latched into the result register (RES7 to RES0) and an interrupt is generated. The counter can be programmed to measure the total input signal period on pin 107 (C–D in Fig.3), the HIGH period A or the LOW period B. The measurement of C–D is continuous, the LOW and HIGH are measured only once more. The measurement mode is pre-determined by the PN and FCL bits of the command Byte ..F0.

The timer/counter preset register can be set to values betwee 0000 and FFFF. In timer mode the values of the preset registers are complemented and then loaded into the counter. The timer starts to count down within the next clock cycle. Thus, the preset value is equal to the number of clock cycles (after prescaler) between each interrupt. An interrupt is generated, if the counter value is zero, and the counter is set to the preset value starting to count down again. One interrupt only is generated, even if several interrupts have not been served. In counter mode, only the preset LOW-byte ..F1 is used as described previously to provide an 8-bit prescaler. No interrupts are caused by an underflow.

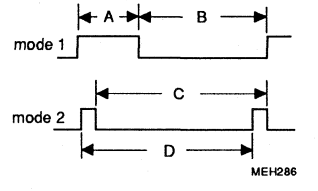


Fig.3 Counter configuration.

Internal control register

Various internal controllable registers control the functions. The register address range for an 8031 host processor is FF00 to FFFF. These registers have to be written or read by the host processor. The initial start address offset after reset is FF00 (8051 type family).

Internal registers and EUROM registers are all mapped in 256 bytes of a memory. Random data will be put on the microcomputer data bus if a write-only register is read.

Table 2 Internal register mapping (addresses FFFF to FF00)

REGISTER FUNCTION	ADDRESS	R/W	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
System command 0	.. FF	RW	EURM	PCK2	PCK1	PCK0	FRS	MOD2	MOD1	MOD0
System command 1	.. FE	RW	0	0	0	0	0	PX2	PX1	0
Reserved	..FD to ..FC	-								
Interrupt INSERV (service)	.. FB	RW	AUXB	AUXB	AUXB	AUXA	UARTB	TMRB	UARTA	EUROM
INTREQ (request)	.. FA	R	AUXB	AUXB	AUXB	AUXA	UARTB	TMRB	UARTA	EUROM
INTVEC (vector)	.. F9	W	OVEC7	OVEC6	OVEC5	OVEC4	0	0	0	ENINTN
		R	0	0	0	0	RINT3	RINT2	RINT1	0
INTMASK (mask)	.. F8	RW	AUXB	AUXB	AUXB	AUXA	UARTB	TMRB	UARTA	EUROM
Reserved	..F7 to ..F4	-								
Timer/counter pre-set	.. F3	R	RES7	RES6	RES5	RES4	RES3	RES2	RES1	MORX
HIGH-byte	.. F2	W	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0
		R	RES7	RES6	RES5	RES4	RES3	RES2	RES1	RES0
LOW-byte	.. F1	W	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0
		R	RES7	RES6	RES5	RES4	RES3	RES2	RES1	RES0
Timer/counter commands	.. F0	W	0	0	PN	FCL	TCC	TPC1	TPC0	TON
		R	RES7	RES6	RES5	RES4	RES3	RES2	RES1	RES0
UART-B control	.. EF	W	TBD7	TBD6	TBD5	TBD4	TBD3	TBD2	TBD1	TBD0
		R	RBD7	RBD6	RBD5	RBD4	RBD3	RBD2	RBD1	RBD0
command and status	.. EE	W	RTSBN	TBR2B	TBR1B	TBR0B	RBR2B	RBR1B	RBR0B	BRKB
		R	CTSBN	CTSBN	RPSB	FRMB	BRKB	OVRB	TXEB	RXFB
UART-A control	.. ED	W	TAD7	TAD6	TAD5	TAD4	TAD3	TAD2	TAD1	TAD0
		R	RAD7	RAD6	RAD5	RAD4	RAD3	RAD2	RAD1	RAD0
command and status	.. EC	W	RTSAN	TBR2A	TBR1A	TBR0A	RBR2A	RBR1A	RBR0A	BRKA
		R	CTSAN	CTSAN	RPSA	FRMA	BRKA	OVRA	TXEA	RXFA
Reserved	..EB to ..E7	-								
Display RAM end address	.. E6	W	DRE15	DRE14	DRE13	DRE12	DRE11	DRE10	DRE9	DRE8
8031 ROM mapping	.. E5	W	0	0	0	R4	R3	R2	R1	R0
Extended RAM mapping	.. E4	W	0	0	0	0	EXT3	EXT2	EXT1	EXT0

Table 3 Function of the register bits of Table 2

<table>
<tr><td>"..FF"
EURM</td><td>Mode selection: 0 = EUROM mode; 1 = dual processor mode</td></tr>
<tr><td>PCK2 to PCK0</td><td>Processor clock selection in 50/60 Hz systems
<table>
<tr><th>PCK2</th><th>PCK1</th><th>PCK0</th><th>50Hz</th><th>60 Hz</th><th>internally devided by</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>2 kHz</td><td>2.4 kHz</td><td>12</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>3 kHz</td><td>3.6 kHz</td><td>8</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>4 kHz</td><td>4.8 kHz</td><td>6</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>6 kHz</td><td>7.2 kHz</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>8 kHz</td><td>9.6 kHz</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>12 kHz</td><td>14.4 kHz</td><td>2</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>12 kHz</td><td>14.4 kHz</td><td>2</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>12 kHz</td><td>14.4 kHz</td><td>2</td></tr>
</table></td></tr>
<tr><td>FRS</td><td>Field select bit: 0 = 50 Hz mode; 1 = 60 Hz mode</td></tr>
<tr><td>MOD2 to MODE0</td><td>Intializing indication
<table>
<tr><th>MOD2</th><th>MOD1</th><th>MOD0</th><th></th><th></th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>=</td><td>not initialized</td></tr>
<tr><td>X</td><td>X</td><td>X</td><td>=</td><td>operational</td></tr>
</table></td></tr>
<tr><td>"..FE"
PX2
PX1</td><td>
Interrupt /acknowledge: 0 = acknowledge-only mode; 1 = end of interrupt
Processor selection: 0 = 16-bit; 1 = 8-bit</td></tr>
<tr><td>"..FB" and "..FA"
AUXB
AUXA
UARTB
TMRB
UARTA
EUROM</td><td>Interrupt request (read and write): 1 = interrupt requested
requested flag reflects pin 99 (AUXBIRQN)
requested flag reflects pin 102 (AUXAIRQN)
requested flag UART-B
requested flag timer/counter
requested flag UART-A
Field sync interrupt from EUROM reflects L/H rising edge of TV sync signal</td></tr>
<tr><td>"..F9"
OVEC7 to OVEC0
RINT3 to RINT1</td><td>
Upper bits of programmable interrupt vector offset address
Internal interrupt vector address bits
<table>
<tr><th>RINT3</th><th>RINT2</th><th>RINT1</th><th>vector</th><th>priority</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>EUROM</td><td>0 (high)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>UART-A</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>TIMER</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>UART-B</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>AUXA</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>AUXB</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>not used</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>not used</td><td>7 (low)</td></tr>
</table></td></tr>
</table>

"..F9" continued ENINTN	Total enable interrupt bit: 0 = enabled; 1 = disabled
"..F8" AUXB AUXA UARTB TMRB UARTA EUROM	Interrupt mask: 0 = enabled; 1 = masked flag AUXB flag AUXA flag UART-B flag timer/counter flag UART-A Field sync flag from EUROM
"..F3" RES7 to RES1 MORX	Result bits, not used MORX signal from UART-A, state of input pin107
"..F2" DH7 to DH0	High value byte of timer preset register
"..F1" DL7 to DL0	Low value byte of timer preset register
"..F0" PN	Measurement polarity: 0 = LOW period measured; for full period measurement H/L transition starts and stops the counter 1 = HIGH period measured; for full period measurement L/H transition starts and stops the counter
FCL	Period counter control: 0 = full period continously measured; interrupt is generated at each full period and the counter value is loaded into the result register 1 = single measurement of either the LOW or HIGH period; the counter value is loaded into the result register
TCC	Timer/counter mode setting: 0 = timer mode; 4-bit prescaler and 16-bit counter from preset value 1 = counter mode; 8-bit counter and 4+8 bit pre-scaler (the counter is gated by the state MORX on pin 107)
TPC1 to TPC0	Prescaler setting: TPC1 TPC0 value 0 0 0 0 1 4 1 0 8 1 1 16
TON	Timer on: 0 = counter disabled; counter set to preset value; 1 = counter enabled

"..EF" RBD7 to RBD0 TBD7 to TBD0	UART-B Read 8-bit serial data input V28RX2 (pin 91) Write 8-bit serial data buffer output V28TX2 (pin 92)
"..EE" RTSBN	UART-B Ready to send bit, active-LOW output signal on pin 82 (V28RTSN)
RBR2B to RBR0B TBR2B to TBR0B	Set baud rate for receive (read) Set baud rate for transmission (write)
BRKB CTSBN RPSB FRMB OVLB TXEB RXFB	Break condition bit: 0 = received data correctly formatted; 1 = no stop bit detected Clear to send byte, active-LOW input signal on pin 98 (V28CTSN) Read input state for status from pin 91 (V28RX2) Frame error bit: 0 = no framing error detected; 1 = framing error detected Overrun of receiver buffer: 0 = no overrun; 1 = overwritten by new data before read out of previous data Transmit buffer empty bit: 0 = not ready to receive new data; 1 = ready Receiver buffer full bit: 0 = no new data; 1 = data clear to be read (new data)
"..ED" RAD7 to RAD0 TAD7 to TAD0	UART-A Read 8-bit serial data input MORX (pin 107) Write 8-bit serial data buffer output MOTX (pin 108)
"..EC" RTSAN	UART-A Ready to send bit, active-LOW output signal on pin 94 (MOWR)
RBR2A to RBR0A TBR2A to TBR0A	Set baud rate for receive (write) Set baud rate for transmission (write) see bit table of UART-B as previously described
BRKA CTSAN RPSA FRMA	Break condition bit: 0 = data correctly formatted; 1 = no stop bit detected Clear to send byte, active-LOW input signal on pin 106 (MORD) Read input state from pin 107 (MORX) Frame error bit: 0 = no framing error detected; 1 = framing error detected

RBR2B TBR2B	RBR1B TBR1B	RBR0B TBR0B	baud rate (1/s)
0	0	0	off
0	0	1	19200
0	1	0	9600
0	1	1	4800
1	0	0	2400
1	0	1	1200
1	1	0	300
1	1	1	75

UART-A	
OVLA	Overrun of receiver buffer: 0 = no overrun; 1 = overwritten by new data before read out of previous data
TXEA	Transmit buffer empty bit: 0 = not ready to receive new data; 1 = ready
RXFA	Receiver buffer full bit: 0 = no new data; 1 = data clear to be read (new data)
"..E6"	
DRE15 to DRE8	Display RAM end address DIA15 to DIA8 and DIA15N (write)
"..E5"	
R5 to R4	Extention of ROM addresses, sets outputs EPA15 and EPA14; Table 5
R2 to R1	Extention of ROM addresses; Table 4
"..E4"	
EXT2 to EXT1	External chip select control to de-activate the display RAM access from the processor and to determine the active chip select (EUROM always has access to the display RAM)

EXT2	EXT1	pins	EMCS2N	EMCS1N	EMCS0N	
0	0		1	1	1	(1)
0	1		1	0	1	(2)
1	0		1	1	0	(2)
1	1		0	1	1	(2)

(1) processor has access to the display RAM (output DIA15 = 0)
(2) processor has access to the extended RAM (Fig.4)

EXT0	Display RAM extention bit to set address output DIA16: 0 = DIA16 is LOW; the lower 64kbyte are addressed (Fig.4) 1 = DIA16 is HIGH; the upper 64kbyte are addressed

Display RAM interface

The display RAM can be extended up to 128 KByte by means of the 17-bit address bus. A bidirectional 8-bit data bus is provided in the RAM interface. The inverted address bit DIA15N is also available, this ensures an economical handling of two 32K8 RAMs (Fig.4). Two RAM accesses are necessary to read/write a 16-bit word from/to memory. Modes are:

- EUROM reads data from RAM
- µP reads/writes data from/to RAM.

The EURAM data fetch has always priority over the RAM access of the controller. The latched address from EUROM is transferred to the RAM output without any delay of full clock cycles (switch of multiplexer only), if the address strobe EUASN (Fig.7) indicates a RAM access of the EUROM. The RAM access for one data byte takes about two clock cycles. A data multiplexer transfers the first data byte to a latch and shift register of the EUROM interface stage. The second data byte, fetched in a further RAM access, completes the word format of EUROM data. This operation takes about five cycles for one RAM access of EUROM. The data word to EUROM is latched out within an additional cycle.

RAM chip select

The external memory chip select is mapped in the address range 0000 to 7FFF. The RAM sections are mapped in 32K8 blocks (Fig.4), enabled by EMCS2N, EMCS1N and EMCS0N (Fig.1 and Table 3).

ROM chip select

The EPROM map register contains the bits R4 to R0 (Byte ..E5) to map the EPROM range directly in 3 x 4 blocks of 16K8 Byte (Fig.5) overlaying the block "0". This action is controlled by ROMCS1N and ROMCS2N outputs. The lower 48K8 Byte ROM can be always accessed. A total of 5 x 64K8 byte ROMs may be mapped.

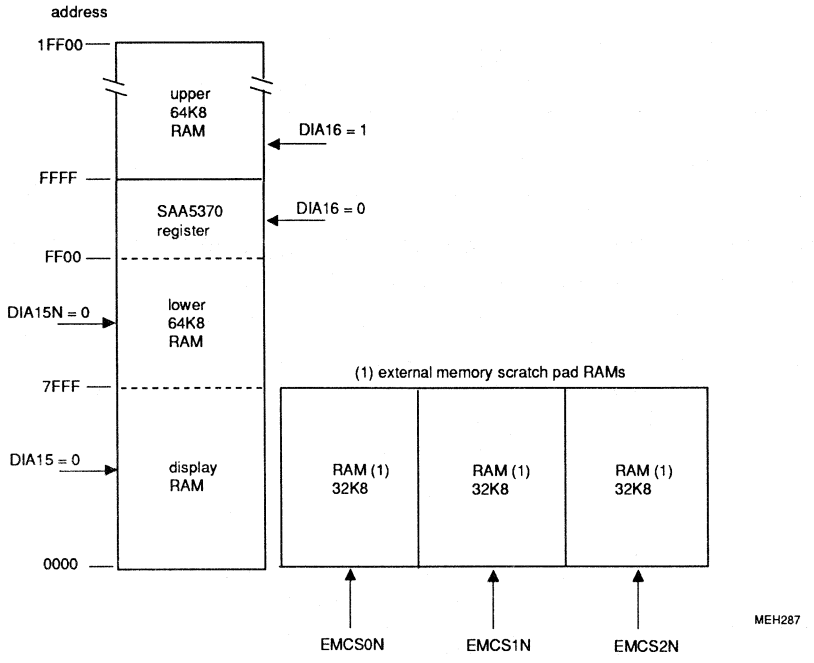


Fig.4 External RAM access.

Table 4 8031 ROM mapping.

outputs MPA15	MPA14	bits of byte ..E5 R2	R1	R0	outputs EPA15	EPA14	ROM CS2N	ROM CS1N	ROM CS0N	address range (kbyte) real RAM	mapped
0	X	X	X	X	0	A14	1	1	0	0 to 32	0 to 32
1	0	X	X	X	1	0	1	1	0	32 to 48	32 to 48
1	1	0	0	0	1	1	1	1	0	48 to 64	48 to 64
1	1	0	0	1	0	0	R4	R3	1	0 to 16	48 to 64
1	1	0	1	0	0	1	R4	R3	1	16 to 32	48 to 64
1	1	0	1	1	1	0	R4	R3	1	32 to 48	48 to 64
1	1	1	X	X	1	1	R4	R3	1	48 to 64	48 to 64

X = 0 or 1
ROMCS0N = normal EPROM chip select

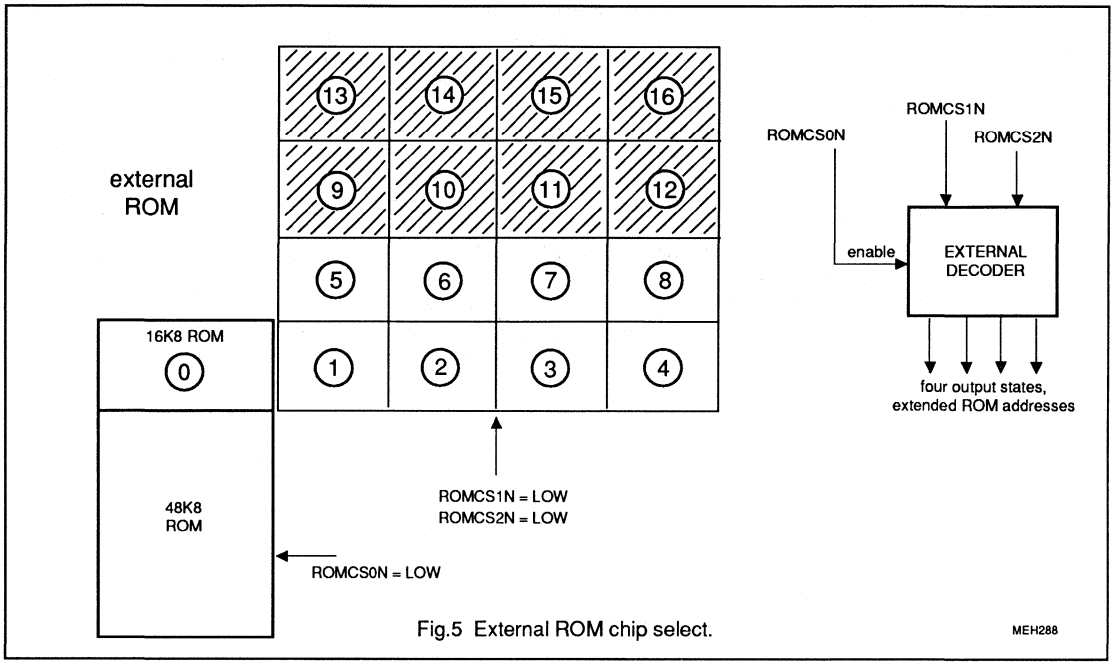


Fig.5 External ROM chip select.

Table 5 8031 ROM control register (ROMCS0N = normal EPROM chip select).

outputs EPA15 (R5-bit))	EPA14 (R4-bit)	ROM CS2N	ROM CS1N	ROM CS0N	ROM block CS direct	ROM block CS decoded
X	X	1	1	0	64 k	64 k
1	1	1	1	0	0	0
0	0	1	0	1	1	5
1	0	1	0	1	2	6
0	1	1	0	1	3	7
1	1	1	0	1	4	8
0	0	0	1	1	5	9
1	0	0	1	1	6	10
0	1	0	1	1	7	11
1	1	0	1	1	8	12
0	0	0	0	1		1
1	0	0	0	1		2
0	1	0	0	1		3
1	1	0	0	1		4
0	0	1	1	1		13
1	0	1	1	1		14
0	1	1	1	1		15
1	1	1	1	1		16

EUROM interface

Operation modes:

- EUROM fetches data from external display RAM (EURM-bit = 0)
- two microcontrollers access a common 64 kbyte RAM. The circuit is a Dual Port RAM Manager (dual processor mode; EURM-bit = 1)

Dual processor mode:
The 16-bit EUROM address/data bus (EUAD15 to EUAD0) is demultiplexed to 16-bit address bus and 8-bit data bus.

The dual processor mode enables two microprocessors to access a common RAM quasi-simultaneously. Then, the EUROM port is used for a second processor with 8- or 16-bit multiplexed address/data bus (PX1-bit = 0 for 16-bit and PX1-bit = 1 for 8-bit processor). Data is automatically multiplexed to and from the 8-bit data bus in case of 16 bit data words.

EUROM registers:
The registers refer to "EUROM User Manual, December 1987".

The registers are directly written by the microcomputer via the registers ..7F to ..40. A range of 64 Bytes is mapped for this purpose (display end address).

An interrupt is generated by the LOW-to-HIGH edge of the EUFSN signal. The interrupt flag for the EUROM is set in the interrupt controller, and the microprocessor has a free access to the EUROM for the pre-display period (register address range 7F to 40).

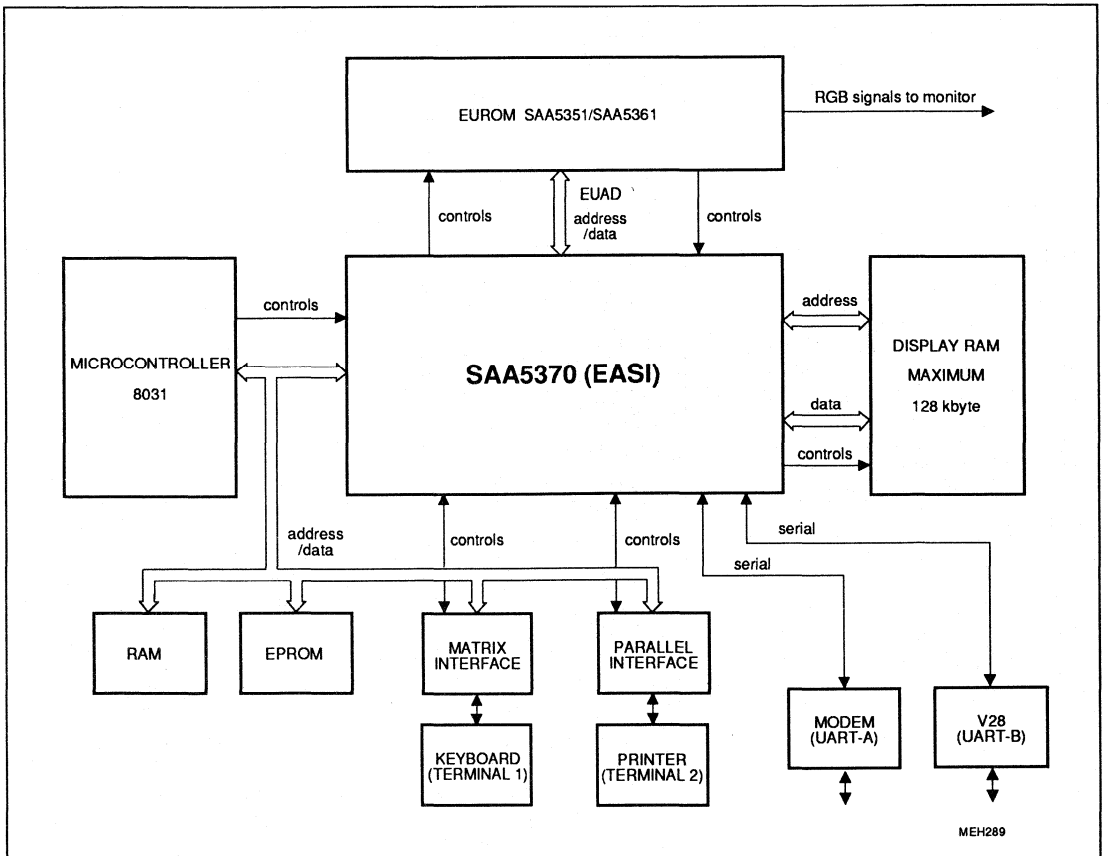


Fig.6 EUROM application with SAA5370.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD1}	supply voltage 1 (pin 10)	−0.5	6.5	V
V_{DD2}	supply voltage 2 (pin 39)	−0.5	6.5	V
V_{DD3}	supply voltage 3 (pin 81)	−0.5	6.5	V
V_I	DC input voltage on all pins	−0.5	V_{DD}	V
I_{DD1}	supply current 1 (pin 10)	-	70	mA
I_{DD2}	supply current 2 (pin 39)	-	70	mA
I_{DD3}	supply current 3 (pin 81)	-	70	mA
P_{tot}	total power dissipation	0	tbf	mW
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	-	±2000	V

DC CHARACTERISTICS

$V_{DD1} = V_{DD2} = V_{DD3} = 4.75$ to 5.25 V; $T_{amb} = 0$ to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range (pins 10, 39 and 81)		4.75	5	5.25	V
I_{DD}	total supply current ($I_{DD1} + I_{DD2} + I_{DD3}$)		-	-	120	mA
Data, address and control inputs (except reset)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DD}	V
V_I	input current		-	-	±1	μA
Reset input						
V_{IL}	input voltage LOW		0	-	0.6	V
V_{IH}	input voltage HIGH		2.4	-	V_{DD}	V
V_I	input current		-	-	±1	μA
Data, address and control outputs						
V_{OL}	output voltage LOW	$I_{OL} = 3.2$ mA	-	-	0.4	V
V_{OH}	outputt voltage HIGH	$I_{OH} = -0.4$ mA	2.4	-	-	V
3-state outputs						
$I_{O\,off}$	output current	high-impedance state	-	-	±5	μA

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

AC CHARACTERISTICS

$V_{DD1} = V_{DD2} = V_{DD3} = 4.75$ to 5.25 V; $T_{amb} = 0$ to 70 °C; output transition time measured with $C_L = 100$ pF unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input signal OSCI from oscillator (pin 40)						
f_{OSCI}	input clock signal frequency		tbf	24.0	28.8	MHz
t_{pL}	LOW time of OSCI		tbf	tbf	tbf	ns
t_{pH}	HIGH time of OSCI		tbf	tbf	tbf	ns
t_r, t_f	rise and fall time		tbf	tbf	tbf	ns
50 Hz and 60 Hz RAM timing		Fig.7				
t_{OSCI}	period time of OSCI	50 Hz timing	-	41.16	-	ns
		60 Hz timing	-	34.72	-	ns
t_{EAD}	EUROM address feed-through delay		-	-	28	ns
t_{CA2}	RAM address feed-through delay	2nd access	-	-	14	ns
t_{RA}	RAM access time	50 Hz timing	-	-	80	ns
		60 Hz timing	-	-	60	ns
t_{DH}	RAM data hold time after address change		-	tbf	-	ns
t_{CD1}	data feed-through delay	1st access	-	tbf	28	ns
t_{CD2}		2nd access	-	tbf	28	ns
t_{EDH}	data hold time on EUROM interface pins		10	tbf	-	ns

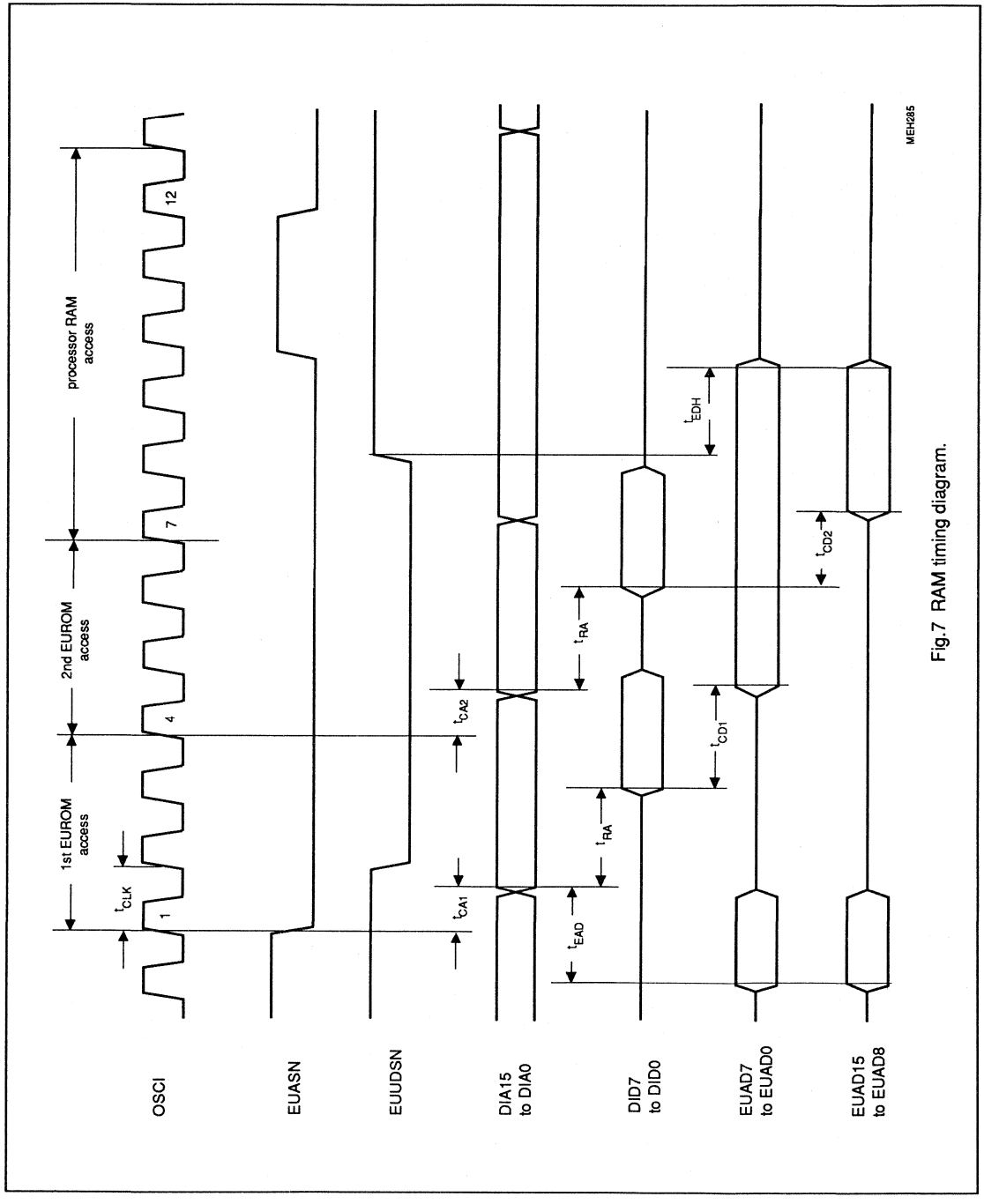


Fig.7 RAM timing diagram.

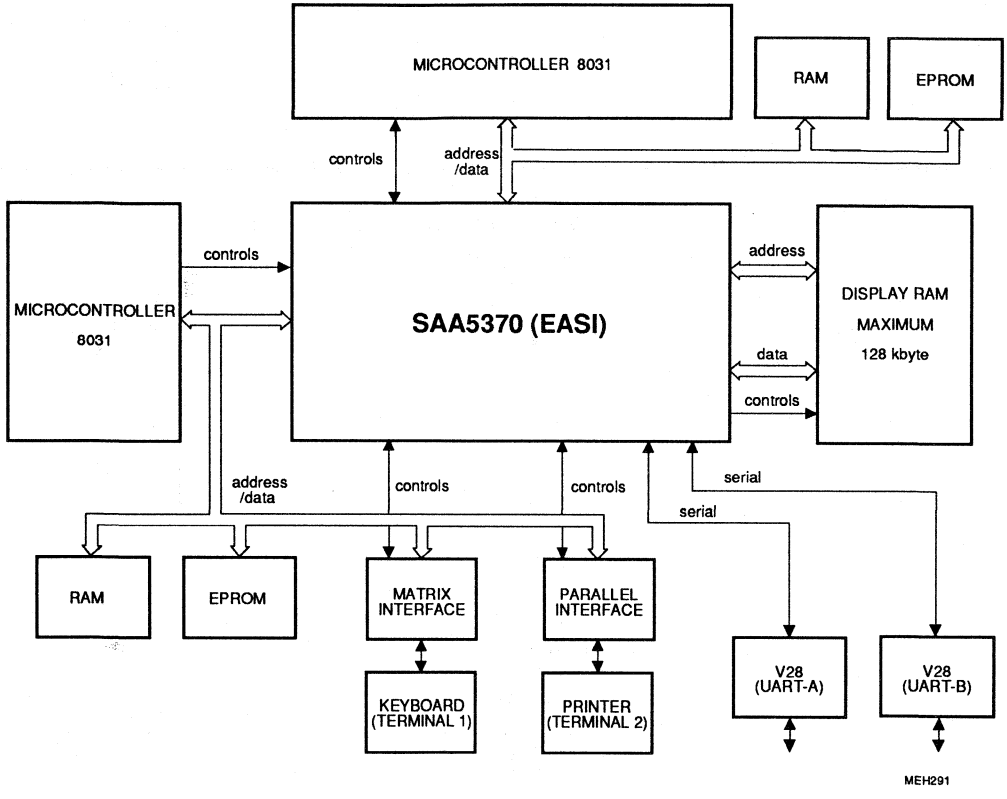


Fig.8 Dual processor application with SAA5370.

Data sheet	
status	Preliminary specification
date of issue	May 1992

SAA7151B

Digital multistandard colour decoder with SCART interface (DMSD2-SCART)

FEATURES

- 8-bit performance on chip for luminance and chrominance signal processing for PAL, NTSC and SECAM standards
- Separate 8-bit luminance and 8-bit chrominance input signals from Y/C, CVBS, S-Video (S-VHS or Hi8) sources
- SCART signal insertion by means of RGB/YUV convertion; fast switch handling
- Horizontal and vertical sync detection for all standards
- Real time control output RTCO
- Fast sync recovery of vertical blanking for VCR signals (bottom flutter compensation)
- Controls via the I^2C-bus
- User programmable aperture correction (horizontal peaking)
- Cross-colour reduction by chrominance comb-filtering (NTSC) or by special cross-colour cancellation (SECAM)
- 8-bit quantization of output signals in 4:1:1 or 4:2:2 formats
- 720 active samples per line
- The YUV bus supports a data rate of 13.5 MHz (CCIR 601).
  - (864 x f_H) for 50 Hz
  - (858 x f_H) for 60 Hz
- Compatible with memory-based features (line-locked clock)
- One 24.576 MHz crystal oscillator for all standards

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage (pins 5, 18, 28, 37 and 52)	4.5	5	5.5	V
I_{DD}	total supply current (pins 5, 18, 28, 37 and 52)	-	100	250	mA
V_I	input levels	TTL-compatible			
V_O	output levels	TTL-compatible			
T_{amb}	operating ambient temperature	0	-	70	°C

GENERAL DESCRIPTION

The SAA7151B is a digital multistandard colour-decoder having two 8-bit input channels, one for CVBS or Y, the other for chrominance or time-multiplexed colour-difference signals.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7151B	68	PLCC	plastic	SOT188CG

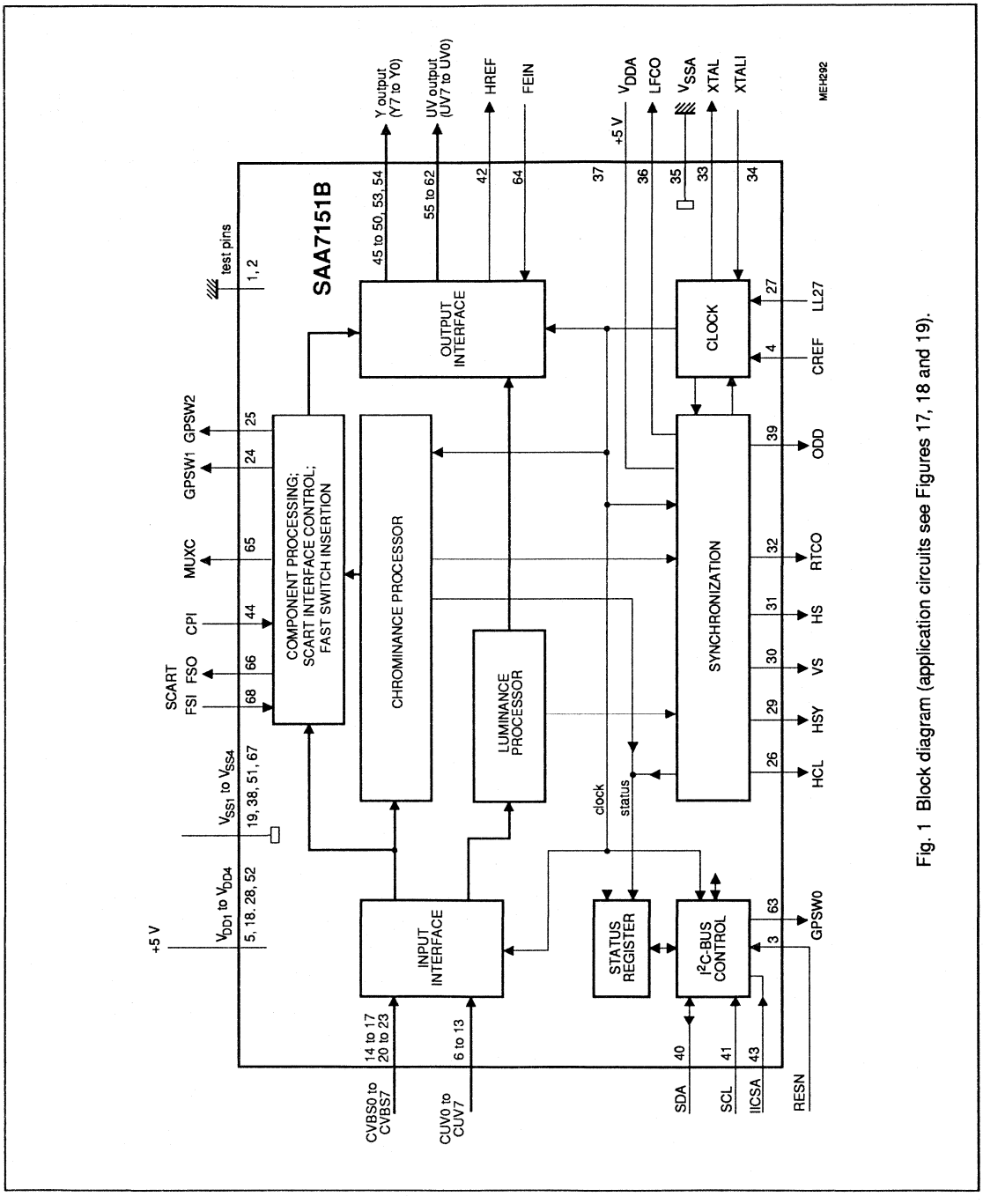


Fig. 1 Block diagram (application circuits see Figures 17, 18 and 19).

PINNING

SYMBOL	PIN	DESCRIPTION
SP	1	connected to ground (shift pin for testing)
AP	2	connected to ground (action pin for testing)
RESN	3	reset, active-LOW
CREF	4	clock reference, sync from external to ensure in-phase signals on the Y-, CUV- and YUV-bus
V_{DD1}	5	+5 V supply input 1
CUV0	6	chrominance input data bits CUV7 to CUV0 (digitalized time-multiplexed signals in two's complement format from a S-Video source (VHS, Hi8) or a chrominance /colour-difference source
CUV1	7	
CUV2	8	
CUV3	9	
CUV4	10	
CUV5	11	
CUV6	12	
CUV7	13	
CVBS0	14	CVBS lower input data bits CVBS3 to CVBS0 (CVBS with luminance, chrominance and all sync information in two's complement format)
CVBS1	15	
CVBS2	16	
CVBS3	17	
V_{DD2}	18	+5 V supply input 2
V_{SS1}	19	ground 1 (0 V)
CVBS4	20	CVBS upper input data bits CVBS7 to CVBS4 (CVBS with luminance, chrominance and all sync information in two's complement format)
CVBS5	21	
CVBS6	22	
CVBS7	23	
GPSW1	24	status bit output FSST0 or port 1 output for general purpose (programmable by subaddress 0C)
GPSW2	25	status bit output FSST1 or port 2 output for general purpose (programmable by subaddress 0C)
HCL	26	black level clamp pulse output (begin and stop programmable), e.g. for TDA8708 (ADC)
LL27	27	line-locked system clock input signal (27 MHz)
V_{DD3}	28	+5 V supply input 3
HSY	29	horizontal sync pulse output (begin and stop programmable), e.g. for TDA8708 (ADC)
VS	30	vertical sync output signal (Fig.10)
HS	31	horizontal sync output signal (Fig.14; start point programmable)
RTCO	32	real time control output; serial increments of HPLL and FSCPLL and status PAL or SECAM sequence (Fig.9)
XTAL	33	24.576 MHz clock output (open-circuit for use with external oscillator)
XTALI	34	24.576 MHz connection for crystal or external oscillator (TTL compatible squarewave)

SYMBOL	PIN	DESCRIPTION
V_{SSA}	35	analog ground
LFCO	36	line frequency control output signal, multiple of horizontal frequency (nominal 6.75 MHz)
V_{DDA}	37	+5 V supply input for analog part
V_{SS2}	38	ground 2 (0 V)
ODD	39	odd/even field identification output (odd = HIGH)
SDA	40	I^2C-bus data line
SCL	41	I^2C-bus clock line
HREF	42	horizontal reference for YUV data outputs (for active line 720Y samples long)
IICSA	43	set module address input of I^2C-bus (LOW = 1000 101X; HIGH = 1000 111X)
CPI	44	clamping pulse input (digital clamping of external UV signals)
Y7	45	Y signal output bits Y7 to Y2 (luminance), part of the digital YUV-bus
Y6	46	
Y5	47	
Y4	48	
Y3	49	
Y2	50	
V_{SS3}	51	ground 3 (0 V)
V_{DD4}	52	+5 V supply input 4
Y1	53	Y signal output bits Y1 to Y0 (luminance), part of the digital YUV-bus
Y0	54	
UV7	55	UV signal output bits UV7 to UV0, part of the digital YUV-bus
UV6	56	
UV5	57	
UV4	58	
UV3	59	
UV2	60	
UV1	61	
UV0	62	
GPSW0	63	port output for general purpose (programmable by subaddress 0D)
FEIN	64	fast enable input (active-LOW to control fast switching due to YUV data; HIGH = YUV high-Z
MUXC	65	multiplexer control output; source select signal for external ADC (UV signal multiplexing)
FSO	66	fast switch and sync insertion output; gated FS signal from FSI or sync insertion pulse in full screen RGB mode
V_{SS4}	67	ground 4 (0 V)
FSI	68	fast switch input signal fed from SCART/peri-TV connector (indicates fast insertion of RGB signals)

Digital multistandard colour decoder with SCART interface (DMSD2-SCART)

SAA7151B

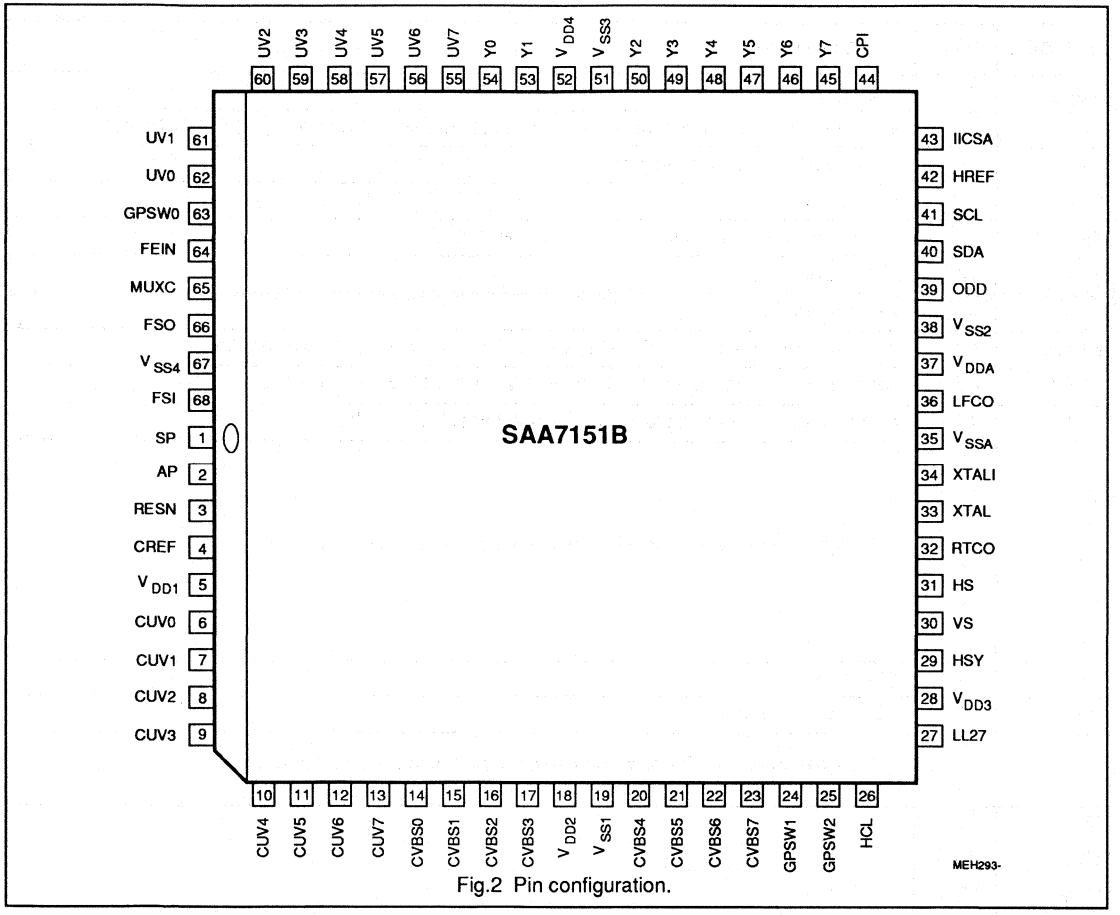


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

System configuration

The SAA7151B decodes digital TV signals with line-locked clock in PAL, SECAM and NTSC standards (CVBS or S-Video) as well as RGB signals coming from a SCART/peri-TV connector. The different source signals are switched, if necessary matrixed and converted (Fig.3 and Table 1).

8-bit CVBS data (digitized composite video) and 8-bit UV data (digitized chrominance and/or time-multiplexed colour-difference signals) are fed to the SAA7151B. The data rate is 27 MHz.

Chrominance processing

The 8-bit chrominance input signal (signal "C" out of CVBS or Y/C in Fig.4a) is fed via the input interface to a bandpass filter for eliminating the DC component, then to the quadrature demodulator. Subcarrier signals from the local oscillator (DTO1) with 90 degree phase shift are applied to its multiplier inputs. The frequency depends on set TV standard.

The multipliers operate as a quadrature demodulator for all PAL and NTSC signals; it operates as a frequency down-mixer for SECAM signals.

The two multiplier output signals are converted to a serial UV data stream and applied to two low-pass filter stages, then to a gain controlled amplifier. A final multiplexed low-pass filter achieves, together with the preceding stages, the required bandwidth performance.

The from PAL and NTSC originated signals are applied to a comb-filter. The signals, originated from SECAM, are fed through a cloche filter (0 Hz centre frequency), a phase demodulator and a differentiator to obtain frequency-demodulated colour-difference signals.

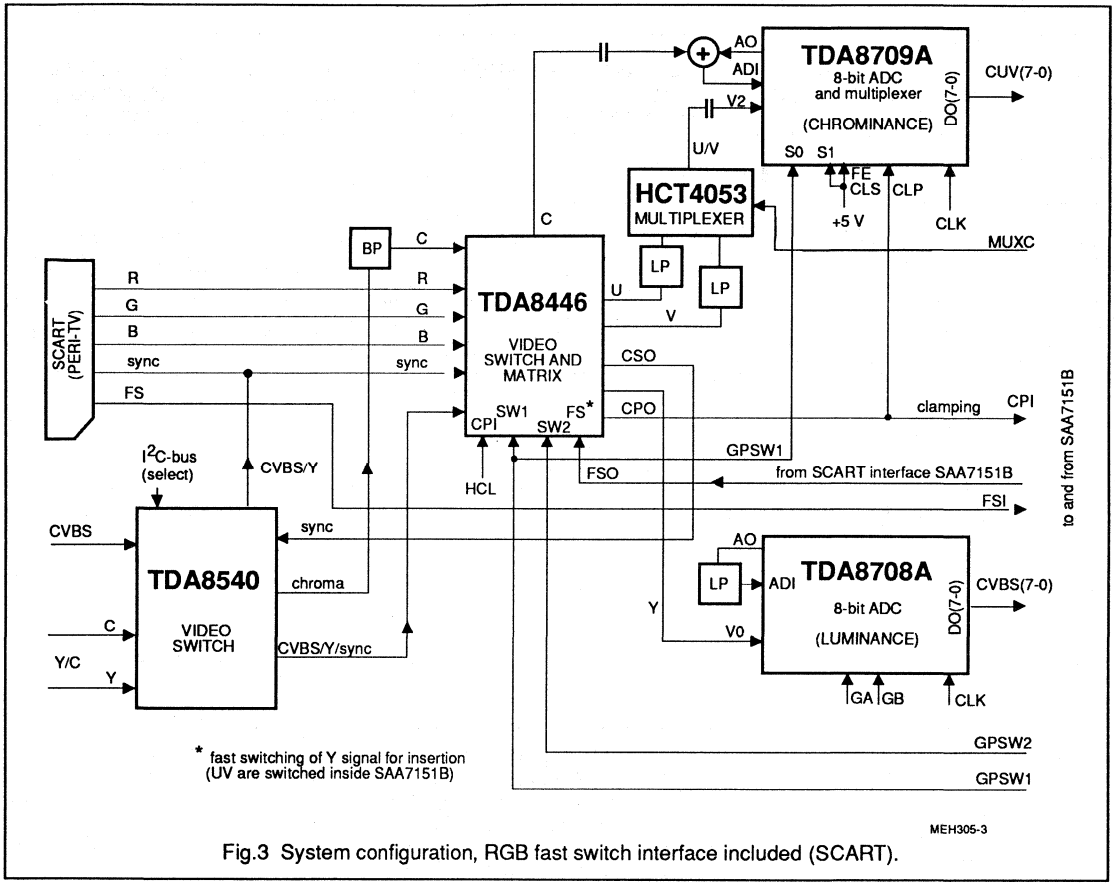


Fig.3 System configuration, RGB fast switch interface included (SCART).

The SECAM signals are fed after de-emphasis to a cross-over switch, to provide the both serial-transmitted colour-difference signals. These signals are finally fed via the fast switch to the output formatter stages and to the output interface. Chrominance signals are output in parallel (4:2:2) on the YUV-bus. The data rate of Y signal (pixel rate) is 13.5 MHz. UV signals have a data rate of 13.5 MHz/2 for the 4:2.2 format (Table 2) respectively 13.5 MHz/4 for the 4:1.1 format (Table 3)

Component processing and SCART interface control

The 8-bit multiplexed colour-difference input signal (signal CUV, Fig.1, out of matrixed RGB in Fig.3) is fed via the input interface to a chrominance stop filter (UV signal only can pass through; Figures 20 to 22). Here it is clamped and fed to the offset compensation which can be enabled or disabled via the I²C-bus.

For matrixed RGB signals – the full screen SCART mode and the fast insertion mode (blanking/switching) are selectable. The chrominance stop filter is automatically bypassed in full screen SCART mode.

Full screen RGB mode (SCART):

The CUV digital input signal (7-0) consists of time-multiplexed samples for U and V. An offset correction for both signals is applied to correct external clamping errors. An internal timing correction compensates for slight differences in timing during sampling. The U and V signals are delay-compensated and fed to the output formatter. The format 4:2:2 or 4:1:1 is generated by a switchable filter.
The control signals for the front end (Figures 3 and 18) MUXC, status bits FSST1, FSST0 (outputs GPSW2, GPSW1) and FSO are generated by the SAA7151B.

Table 1 SCART interface control (Fig.3)

mode	connection FSO	GPSW 2	GPSW 1	MUXC	chroma output of TDA8446 to TDA8709A	TDA8709A selected input	CUV (7-0)	luminance fast switch TDA8446	input selector (via I²C-bus) TDA8540
RGB only	0	0	0	0	high-Z	VIN2	U/V	sync (RGB)	sync (RGB)
	0	0	0	1					
Y/C or CVBS only	0	0	1	0	C	VIN1	C	Y (Y/C) or CVBS	Y (Y/C) or CVBS
	0	0	1	1					
Fast switch	0	1	0	0	C	VIN2	0.5(C+U)/ 0.5(C+V)	Y (Y/C) or CVBS	Y (Y/C) or CVBS
	0	1	0	1					
	0	1	1	0	not used				
	0	1	1	1					
RGB only	1	0	0	0	high-Z	VIN2	U/V	Y (RGB)	sync (RGB)
	1	0	0	1					
	1	0	1	0	not used				
	1	0	1	1					
Fast switch	1	1	0	0	C	VIN2	0.5(C+U)/ 0.5(C+V)	Y (RGB)	Y (Y/C) or CVBS
	1	1	0	1					
	1	1	1	0	not used				
	1	1	1	1					

Fast insertion mode:

Fast insertion is applied by FSI pulse to ensure correct timing. The RGB source signal is matrixed into UV and inserted into the CVBS or Y/C source signal after two field periods if FSI pulses are received. The output FSO is set to HIGH during a determined insertion window (screen plain minus 6 % of horizontal and vertical deflection). Switch over depends on the phase of FSI in relation to the valid pixel sequence depending on the phase-different weighting factors. They are applied to the original and the inserted UV data (Figures 5 and 6)
The control signals for the front end (Table 1) MUXC, FSO, status bits FSST1 and FSST0 (outputs GPSW2 and GPSW1) are generated by the SAA7151B .

The amplitude of chrominance and colour-difference signals are scaled down by factor 2 to avoid overloading of the chrominance analog-to-digital converter. The amplitudes are reduced in the TDA8446 by signals on lines GPSW2 and GPSW1.

Luminance processing

The luminance input signal, a digital CVBS format or an 8-bit luminance format (S-Video), is fed through a sample rate converter to reduce the data rate to 13.5 MHz (Fig.4b).

Sample rate is converted by means of a switchable pre-filter. High frequency components are emphasized to compensate for loss in the following chrominance trap filter. This chrominance trap filter (f_o = 4.43 MHz or f_o = 3.58 MHz centre frequency selectable) eliminates the most of the colour carrier signal, therefore, it must be bypassed for S-Video signals.

The high frequency components of the luminance signal can be "peaked" in two bandpass filters with selectable transfer characteristic. A coring circuit (±1 LSB) can improve the signal , this signal is then added to the original signal. A switchable amplifier achieves a common DC amplification, because the DC gains are different in both chrominance trap modes. Additionally, a cut-off sync pulse is generated for the original signal in both modes.

Synchronization

The luminance output signal is fed to the synchronization stage. Its bandwidth is reduced to 1 MHz in a low-pass filter (sync pre-filter). The sync pulses are sliced and fed to the phase detectors to be compared with the sub-divided clock frequency. The resulting output signal is applied to the loop filter to

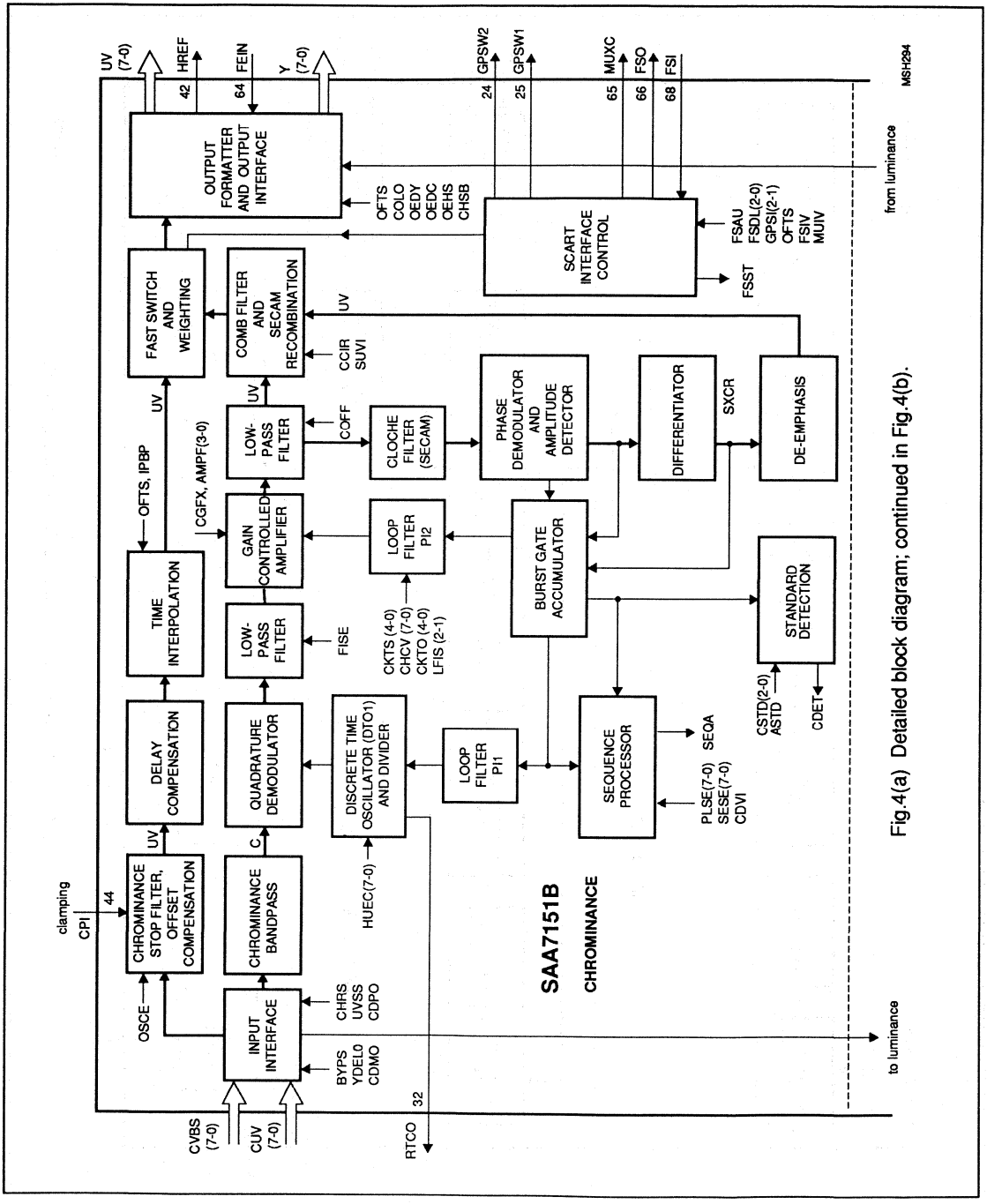


Fig.4(a) Detailed block diagram; continued in Fig.4(b).

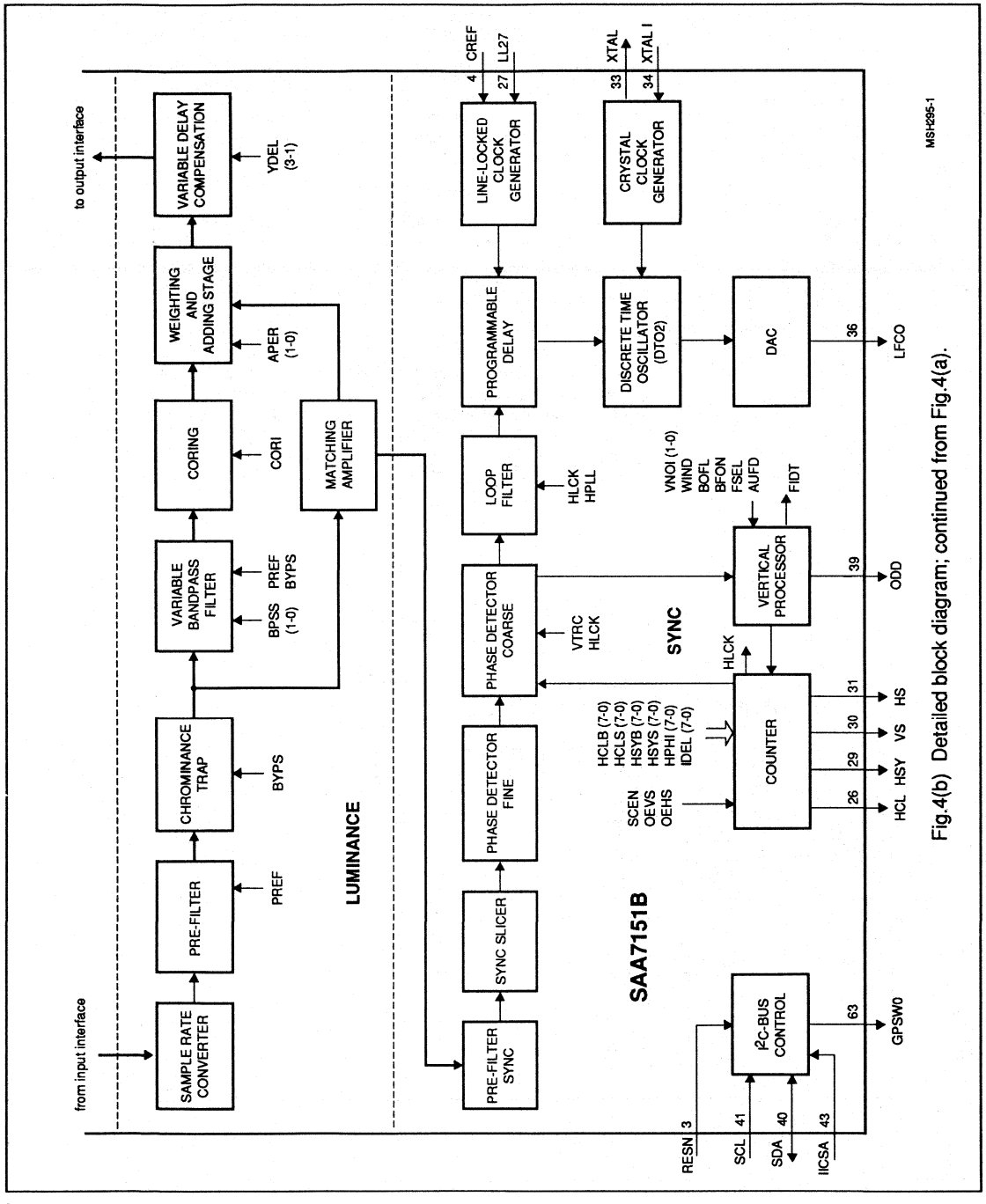


Fig.4(b) Detailed block diagram; continued from Fig.4(a).

accumulate all phase deviations. There are three groups of output timing signals:

a. signals related to data output signals (HREF)
b. signals related to the input signals (HSY, and HCL)
c. signals related to the internal sync phase

All horizontal timings are derived from the main counter, which represents the internal sync phase. The HREF signal only with its critical timing is phase-compensated in relationship to the data output signal. Future circuit improvements could slightly influence the processing delays of some internal stages to achieve a changed timing due to the timing groups b and c.
The HREF signal only controls the data multiplexer phase and the data output signals.

All timings of the following diagrams are measured with nominal input signals, for example coming from a pattern generator. Processing delay times are taken between input and data output, respectively between internal sync reference (main counter = 0) and the rising edge of HREF.

Line locked clock frequency

LFCO is required in an external PLL (SAA7157) to generate the line-locked clock frequency LL27 and CREF.

YUV-bus, digital outputs

The 16-bit YUV-bus transfers digital data from the output interfaces to a feature box, or to the digital-to-analog converter (DAC). Outputs are controlled via the I²C-bus in normal selections, or they are controlled by output enable chain (FEIN, pin 64). The YUV-bus data rate 13.5 MHz. Timing is achieved by marking each second positive rising edge of the clock LL27 synchronized by CREF.

YUV-bus formats
4 : 2 : 2 and 4 : 1 : 1

The output signals Y7 to Y0 are the bits of the digital luminance signal. The output signals UV7 to UV0 are the bits of the digital colour-difference signal. The frames in the Tables 2 and 3 are the time to transfer a full set of samples. In case of 4 : 2 : 2 format two luminance samples are transmitted in comparision to one U and one V sample within one frame. The time frames are controlled by the HREF signal, which determines the correct UV data phase. The YUV data outputs can be enabled or set to 3-state position by means of the FEIN signal. FEIN = LOW enables the output; HIGH on this pin forces the Y and U/V outputs after 2 x LL27 clock cycles to a high-impedance state.

Table 2 for the 4 : 2 : 2 format (720 pixels per line). The quoted frequencies are valid on the YUV-bus. The time frames are controlled by the HREF signal.

output /pin	pixel byte sequence					
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7(MSB)	U7	V7	U7	V7	U7	V7
Y frame	0	1	2	3	4	5
UV frame	0		2		4	

Table 3 for the 4 : 1 : 1 format (720 pixels per line). The quoted frequencies are valid on the YUV-bus. The time frames are controlled by the HREF signal.

output/pin	pixel byte sequence							
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	0	0	0	0	0	0	0	0
UV1	0	0	0	0	0	0	0	0
UV2	0	0	0	0	0	0	0	0
UV3	0	0	0	0	0	0	0	0
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7 (MSB)	U7	U5	U3	U1	U7	U5	U3	U1
Y frame	0	1	2	3	4	5	6	7
UV frame	0				4			

Signal levels (Figures 11 and 12)

The nominal input and output signal levels are defined by a colour bar signal with 75 % colour, 100 % saturation and 100 % luminance amplitude (EBU colour bar).

CUV-bus input format

The CUV-bus transfers the digital chrominance/colour-difference signals from the ADC to the SAA7151B (Fig.5; Table 1):

- normal mode for digital chrominance transmission.
- UV colour-difference mode for colour-difference signals UV (out of matrixed RGB signals)
- FS mode (fast switch mode; UV inserted into chrominance signal C with addition of the two signal spectra).

RTCO output

The RTCO output signal (Fig.9) contains serialized information about actual clock frequency, subcarrier frequency and PAL/SECAM sequence. This signal may preferably be used with the frequency-locked digital video encoder SAA7199B.

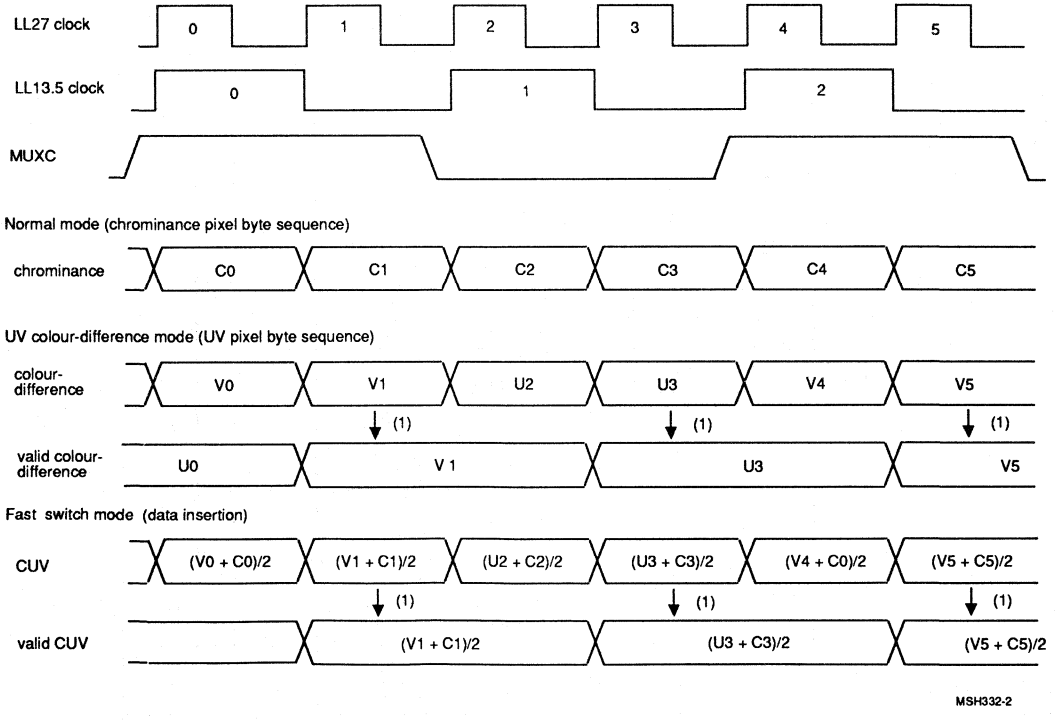


Fig.5 CUV input formats.
(1) each second sample only after a MUXC change is taken for down-sampling to 13.5 MHz to reduce cross-talk components between U and V signals.

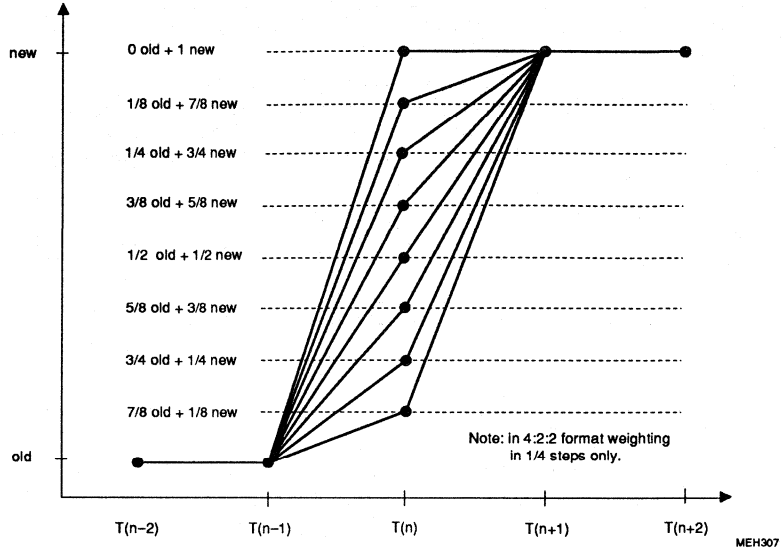


Fig.6 Addition of weighted components.

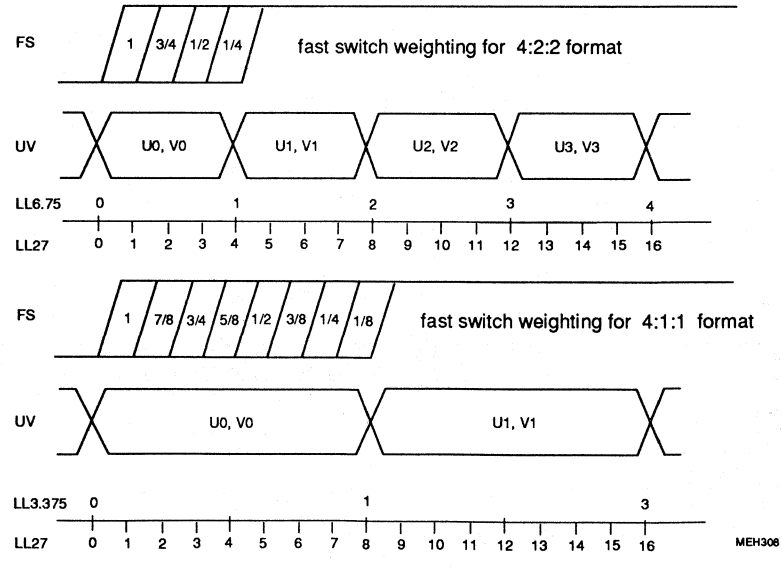


Fig.7 Weighting factors of fast switching for 4:2:2 and 4:1:1 formats.

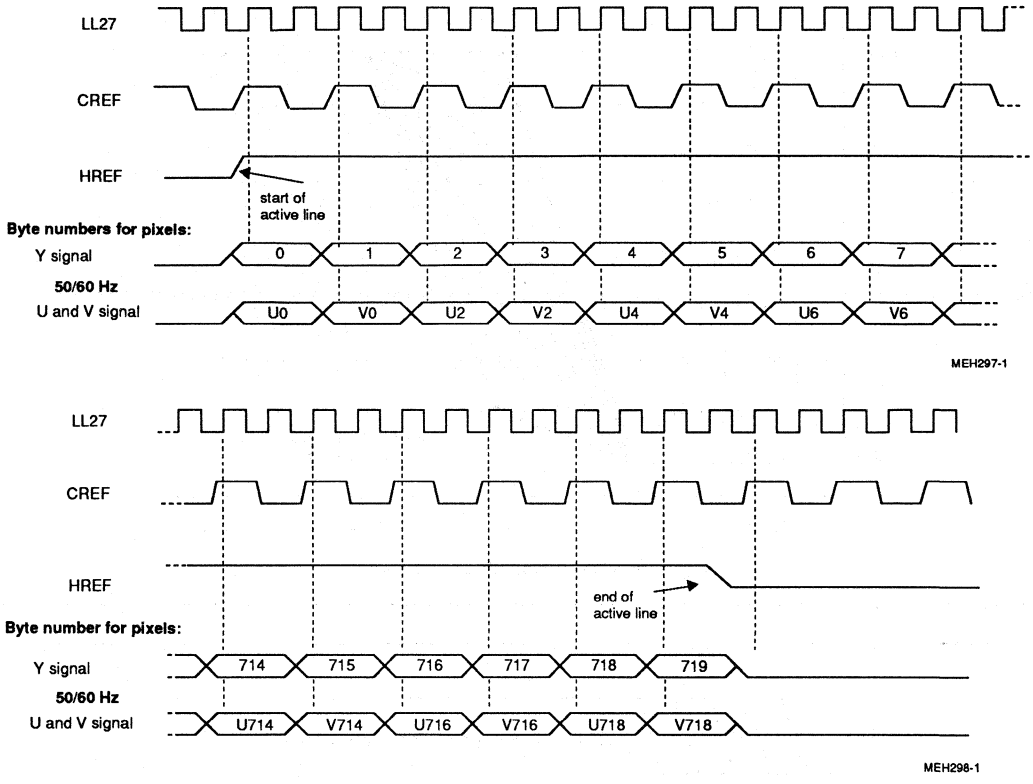
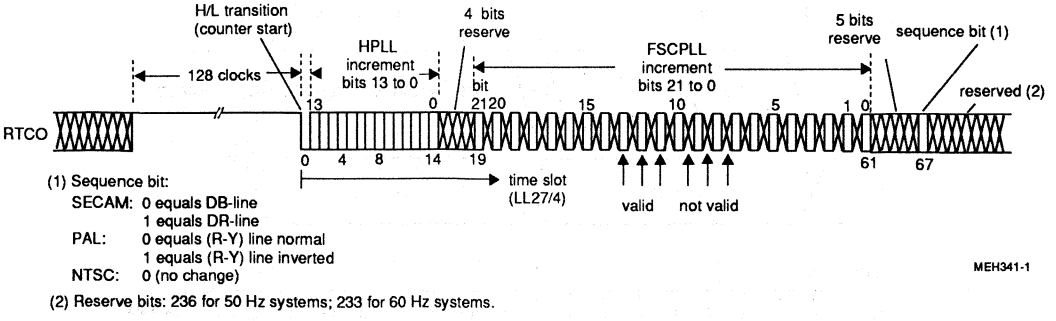


Fig.8 Line control by HREF in 4:2:2 format for 50 Hz and 60 Hz systems.



(2) Reserve bits: 236 for 50 Hz systems; 233 for 60 Hz systems.

Fig.9 RTCO timing.

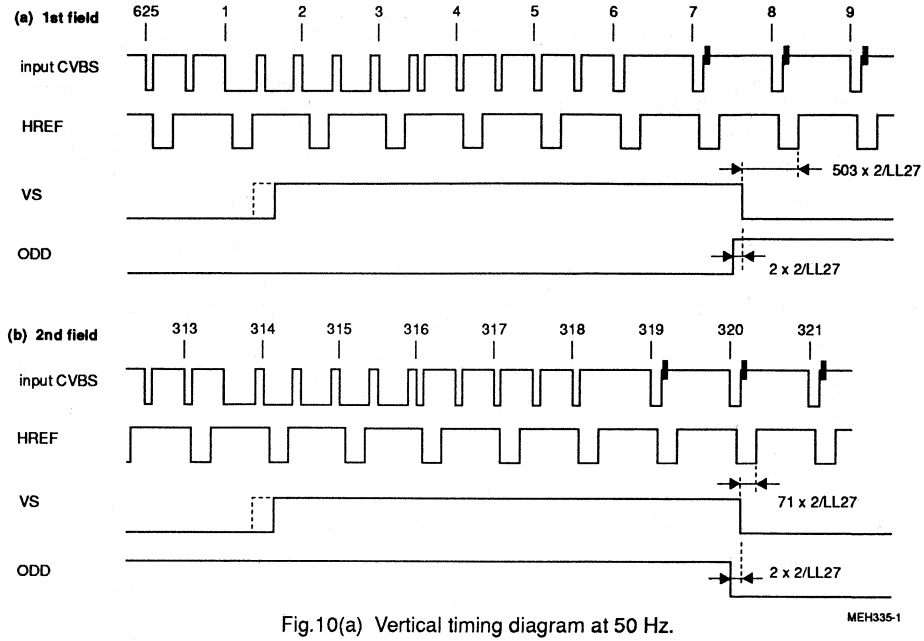


Fig.10(a) Vertical timing diagram at 50 Hz.

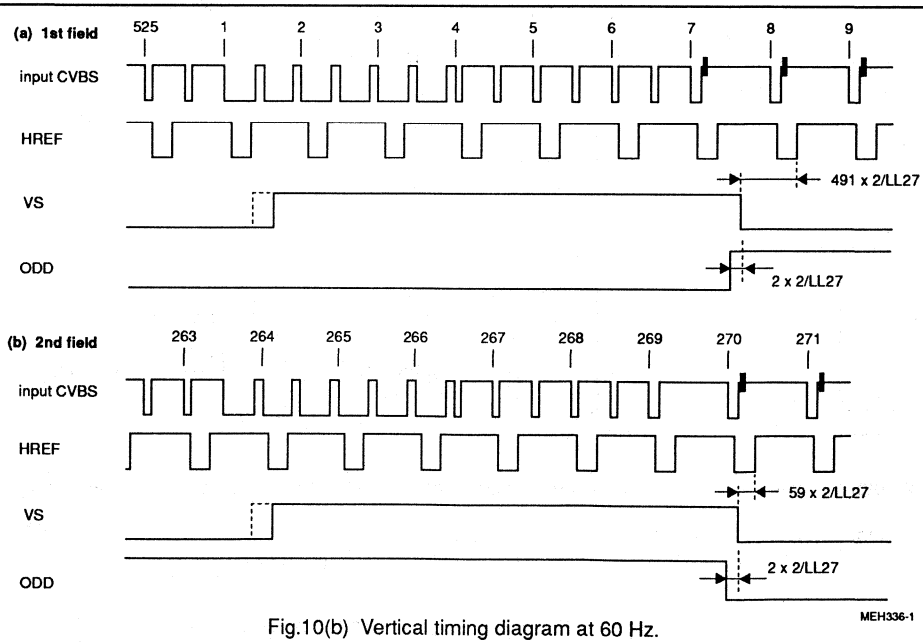
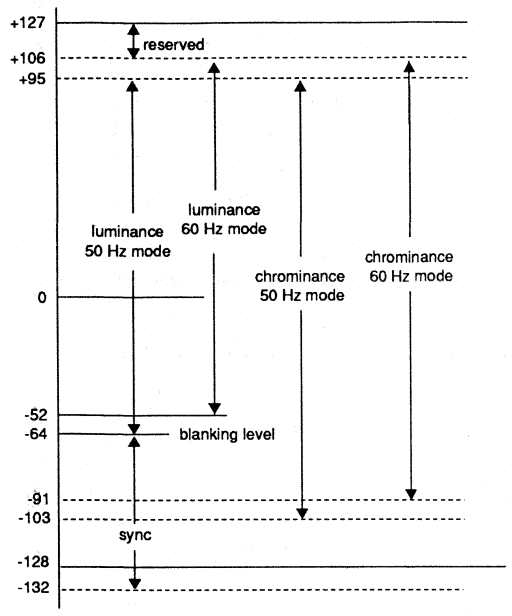
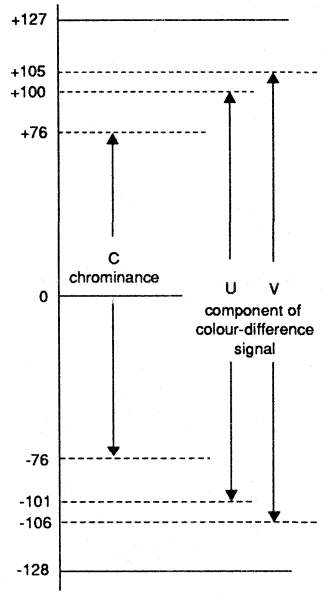


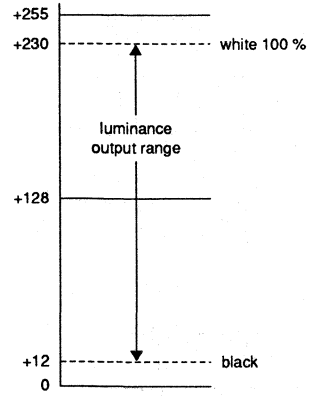
Fig.10(b) Vertical timing diagram at 60 Hz.



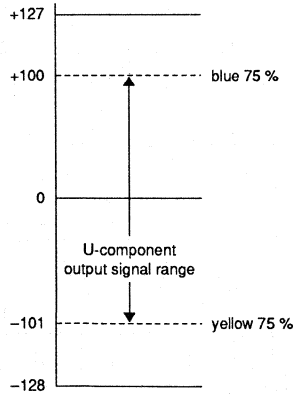
(a) CVBS input signal range.



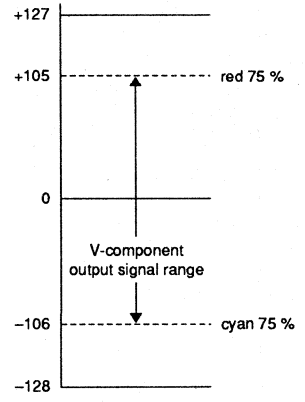
(b) CUV input signal range (U and V out of RGB; in field select mode ranges x 0.5).



(c) Y output signal range.



(d) U output signal range (B-Y).



(e) V output signal range (R-Y).

Notes: 1. All levels are related to EBU colour bar.
2. Values in decimal at 100 % luminance and 75 % chrominance amplitude.

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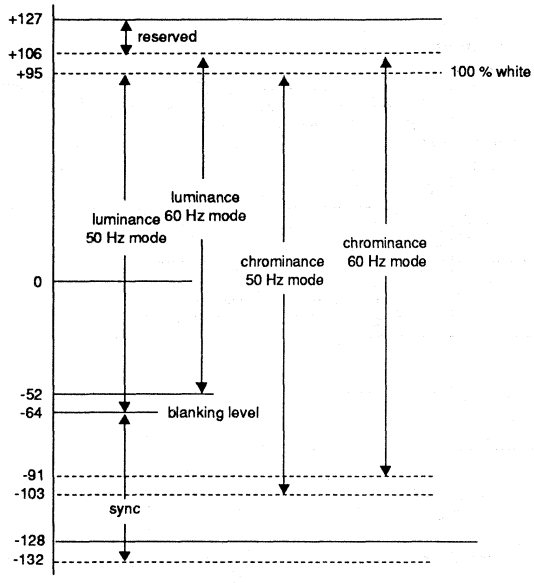
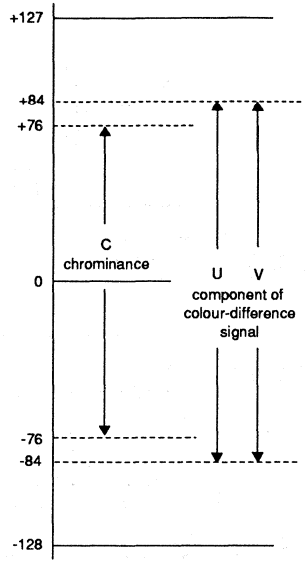
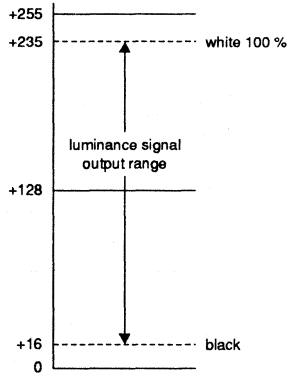
Fig.11 Input and output signal ranges in DTV mode (digital TV).



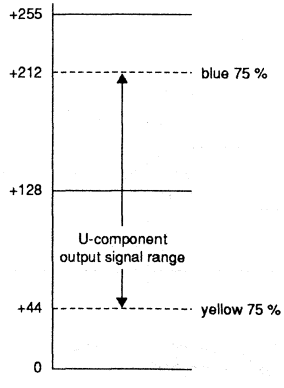
(a) CVBS input signal range.



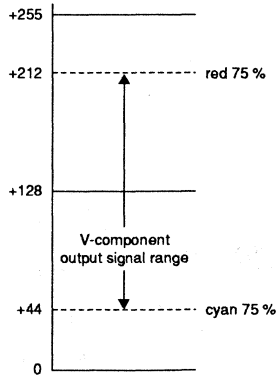
(b) CUV input signal range (U and V out of RGB; in FS mode ranges x 0.5).



(c) Y output signal range.



(d) U output signal range (B-Y).



(e) V output signal range (R-Y).

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Notes: 1. All levels are related to EBU colour bar.
2. Values in decimal at 100 % luminance and 75 % chrominance amplitude.
3. For SECAM input signals the CCIR levels will be exceeded.

Fig.12 Input and output signal ranges in CCIR mode.

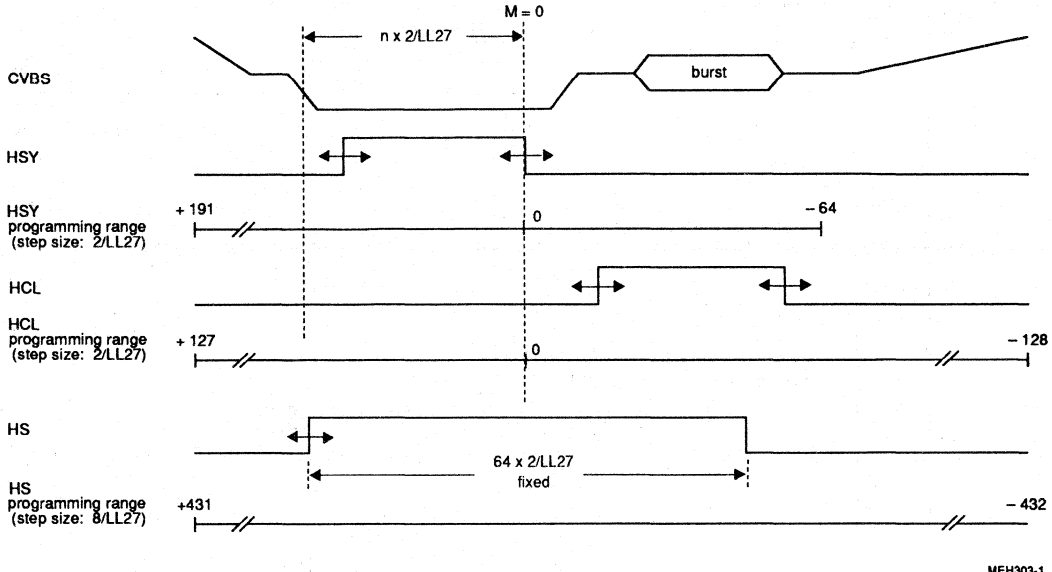


Fig.13 Horizontal sync indication HSY, HS and clamping HCL.

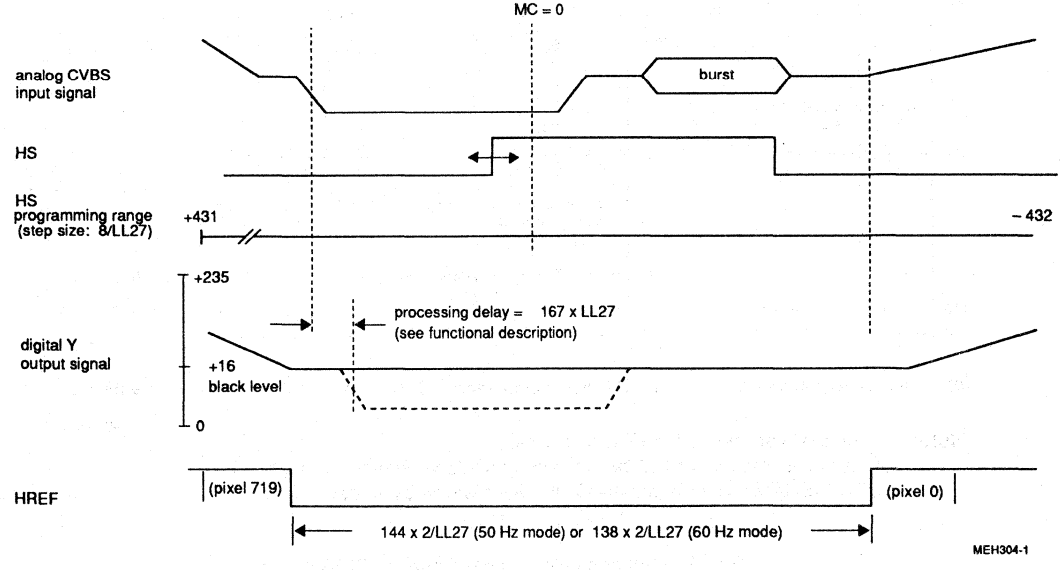


Fig.14 Data clock HREF and horizontal sync HS for 50/60 Hz.

LIMITING VALUES

In accordance with the Absolute Maximum Rating ystem (IEC 134); ground pins 19, 35, 38, 51 and 67 as well as supply pins 5, 18, 28, 37 and 52 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pins 5, 18, 28, 37, 52)	–0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{SS\ A} - V_{SS(1\ to\ 4)}$	-	±100	mV
V_I	voltage on all inputs	–0.5	V_{DD}+0.5	V
V_O	voltage on all outputs ($I_{O\ max}$ = 20 mA)	–0.5	V_{DD}+0.5	V
P_{tot}	total power dissipation	-	2.5	W
T_{stg}	storage temperature range	–65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	±2000	-	V

CHARACTERISTICS V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range (pins 5, 18, 28, 37, 52)		4.5	5	5.5	V
I_{DD}	total supply current (pins 5, 18, 28, 37, 52)	V_{DD} = 5 V; inputs LOW; outputs not connected	-	100	250	mA
I²C-bus, SDA and SCL (pins 40 and 41)						
$V_{I\,L}$	input voltage LOW		–0.5	-	1.5	V
$V_{I\,H}$	input voltage HIGH		3	-	V_{DD}+0.5	V
$I_{40,41}$	input current		-	-	±10	µA
I_{ACK}	output current on pin 40	acknowledge	3	-	-	mA
$V_{O\,L}$	output voltage at acknowledge	I_{40} = 3 mA	-	-	0.4	V
Signal and control inputs (pins 3, 4, 6 to 17, 20 to 23, 27, 64 and 68); Figures 11 and 12						
$V_{I\,L}$	LL27 input voltage (pin 27)	LOW	–0.5	-	0.6	V
$V_{I\,H}$		HIGH	2.4	-	V_{DD}+0.5	V
$V_{I\,L}$	other input voltages	LOW	–0.5	-	0.8	V
$V_{I\,H}$		HIGH	2.0	-	V_{DD}+0.5	V
I_{leak}	input leakage current		-	-	10	µA
C_I	input capacitance	data inputs; note 1	-	-	8	pF
		I/O high-impedance	-	-	8	pF
		clock inputs	-	-	10	pF
$t_{SU.DAT}$	input data set-up time	Fig.15	11	-	-	ns
$t_{HD.DAT}$	input data hold time		3	-	-	ns

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.; inputs and outputs are protected against electrostatic discharge in normal handling. Normal precautions appropriate to handle MOS devices is recommended ("Handling MOS Devices").

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
YUV-bus outputs (pins 45 to 50 and pins 53 to 62), Figures 8 and 11 to 12						
V_{OL}	output voltage LOW	notes 1 and 2	0	-	0.6	V
V_{OH}	output voltage HIGH		2.4	-	V_{DD}	V
C_L	load capacitor		15	-	50	pF
LFCO output (pin 36)						
V_o	output signal (peak-to-peak value)	note 2	1.4	-	2.6	V
V_{36}	output voltage range		1	-	V_{DD}	V
Control outputs (pins 24 to 26, 29 to 32, 39, 42, 63, 65 and 66); Fig.10, 13 and 14						
V_{OL}	output voltage LOW	notes 1 and 2	0	-	0.6	V
V_{OH}	output voltage HIGH		2.4	-	V_{DD}	V
C_L	load capacitor	YUV, HREF	15	-	50	pF
		controls	7.5	-	25	pF
Timing of YUV-bus and control outputs		Fig.8 and 10				
t_{OH}	output signal hold time for	YUV, HREF; C_L = 15 pF	13	-	-	ns
		controls; C_L = 7.5 pF	13	-	-	ns
t_{OS}	output set-up time	YUV, HREF; C_L = 50 pF	20	-	-	ns
		controls; C_L = 25 pF	20	-	-	ns
t_{SZ}	data output disable transition time	to 3-state condition	22	-	-	ns
t_{ZS}	data output enable transition time	from 3-state condition	20	-	-	ns
Chrominance PLL						
f_C	catching range		±400	-	-	Hz
Crystal oscillator		Figures 16 and 17; note 3				
f_n	nominal frequency	3rd harmonic	-	24.576	-	MHz
$\Delta f / f_n$	permissible deviation f_n		-	-	±50	10^{-6}
	temperature deviation from f_n		-	-	±20	10^{-6}
X1	crystal specification:					
	temperature range T_{amb}		0	-	70	°C
	load capacitance C_L		8	-	-	pF
	series resonance resistance R_S		-	40	80	Ω
	motional capacitance C_1		-	1.5±20%	-	fF
	parallel capacitance C_0		-	3.5±20%	-	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Line locked clock input LL27 (pin 27)		Fig.8 and 15				
t_{LL27}	cycle time	note 4	35	-	39	ns
t_p	duty factor	t_{LL27H}/t_{LL27}	40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns

Notes to the characteristics

1. Data output signals are Y7 to Y0 and UV7 to UV0. All other are control output signals.
2. Levels are measured with load circuit. YUV-bus outputs with 1.2 kΩ in parallel to 50 pF at 3 V (TTL load); LFCO output with 10 kΩ in parallel to 15 pF and other outputs with 1.2 kΩ in parallel to 25 pF at 3 V (TTL load).
3. Recommended crystal: Philips 4322 143 05291.
4. t_{SU}, t_{HD}, t_{OH} and t_{OD} include t_r and t_f.

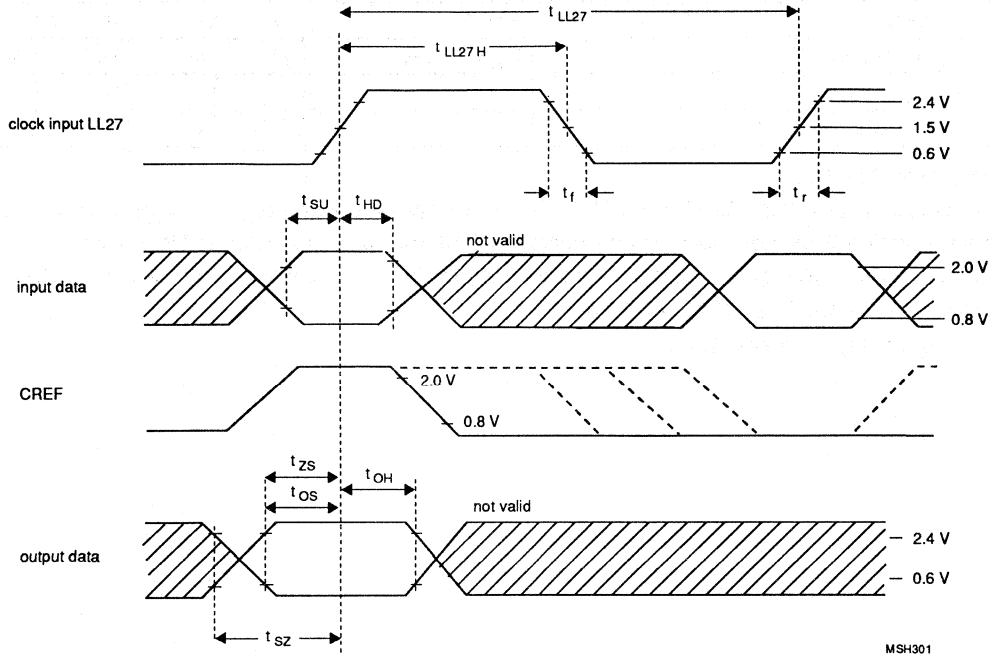


Fig.15 Data input and output timing diagram.

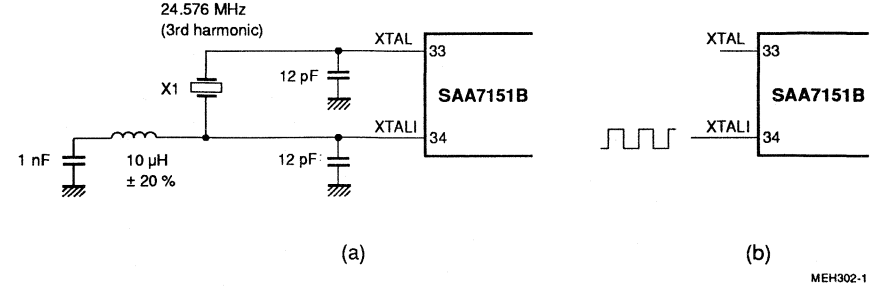


Fig.16 Oscillator application (a) and optional clock from external (b).

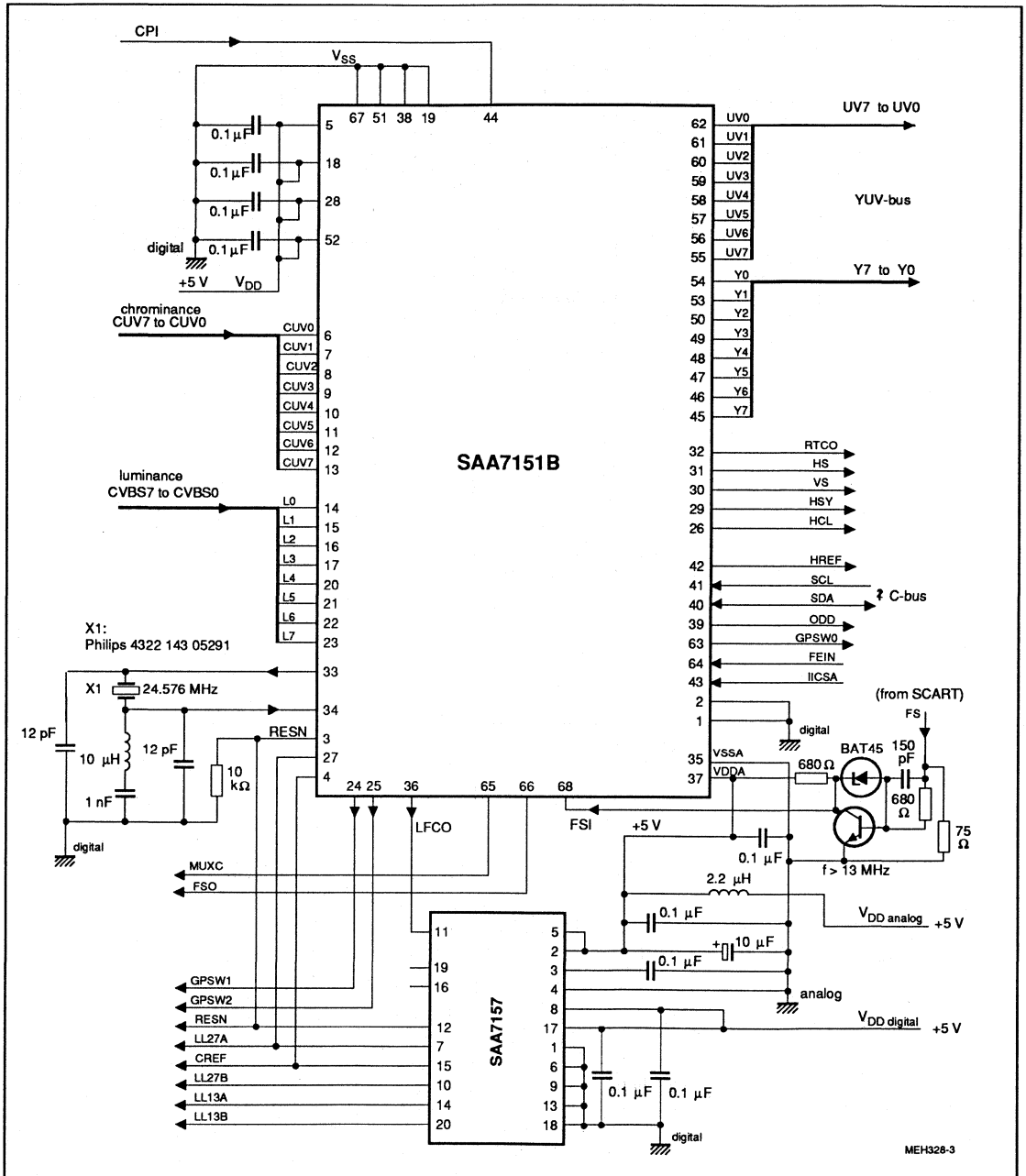


Fig.17 Application of SAA7151B.

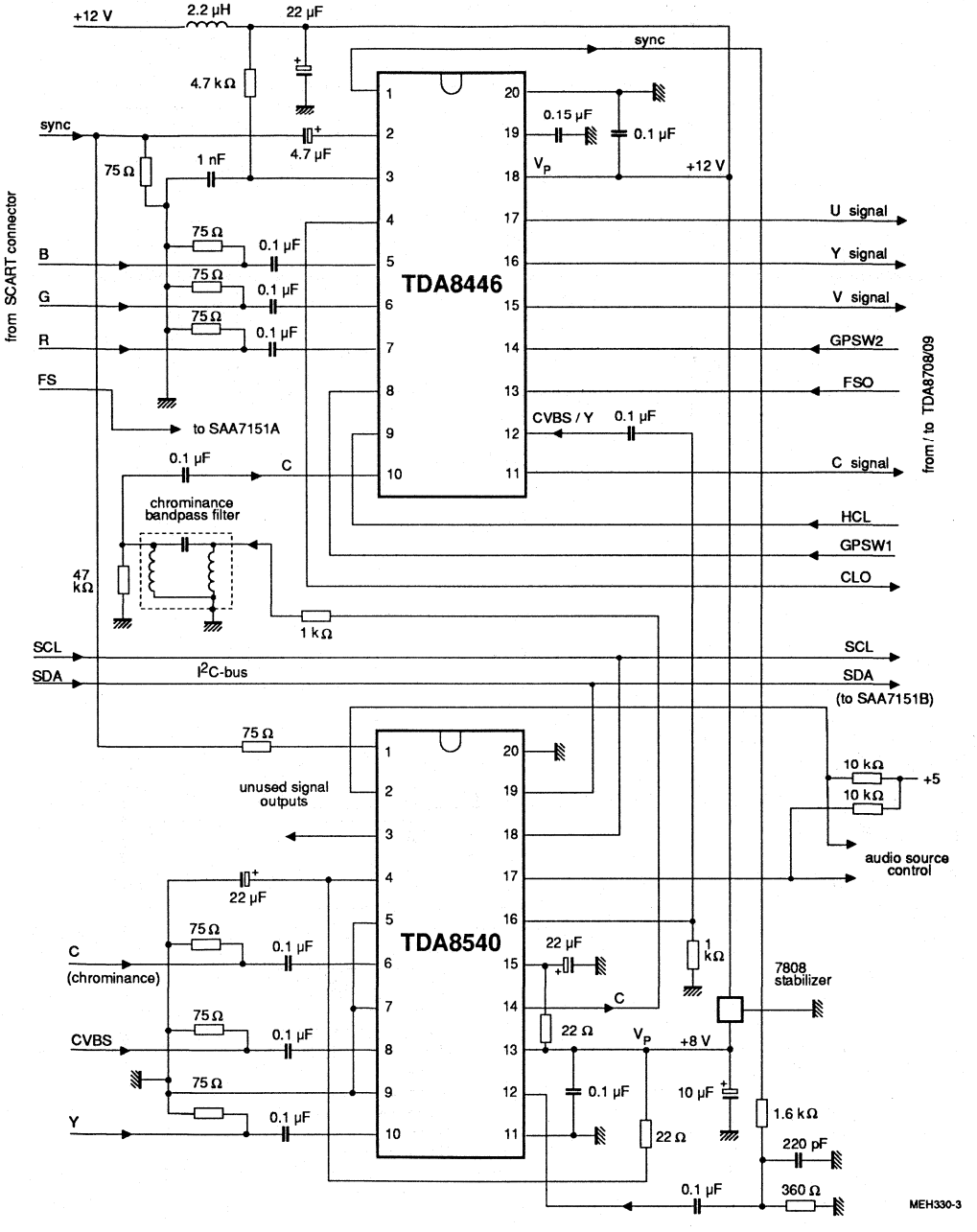


Fig.18 Application of input signal selecting (SCART interface).

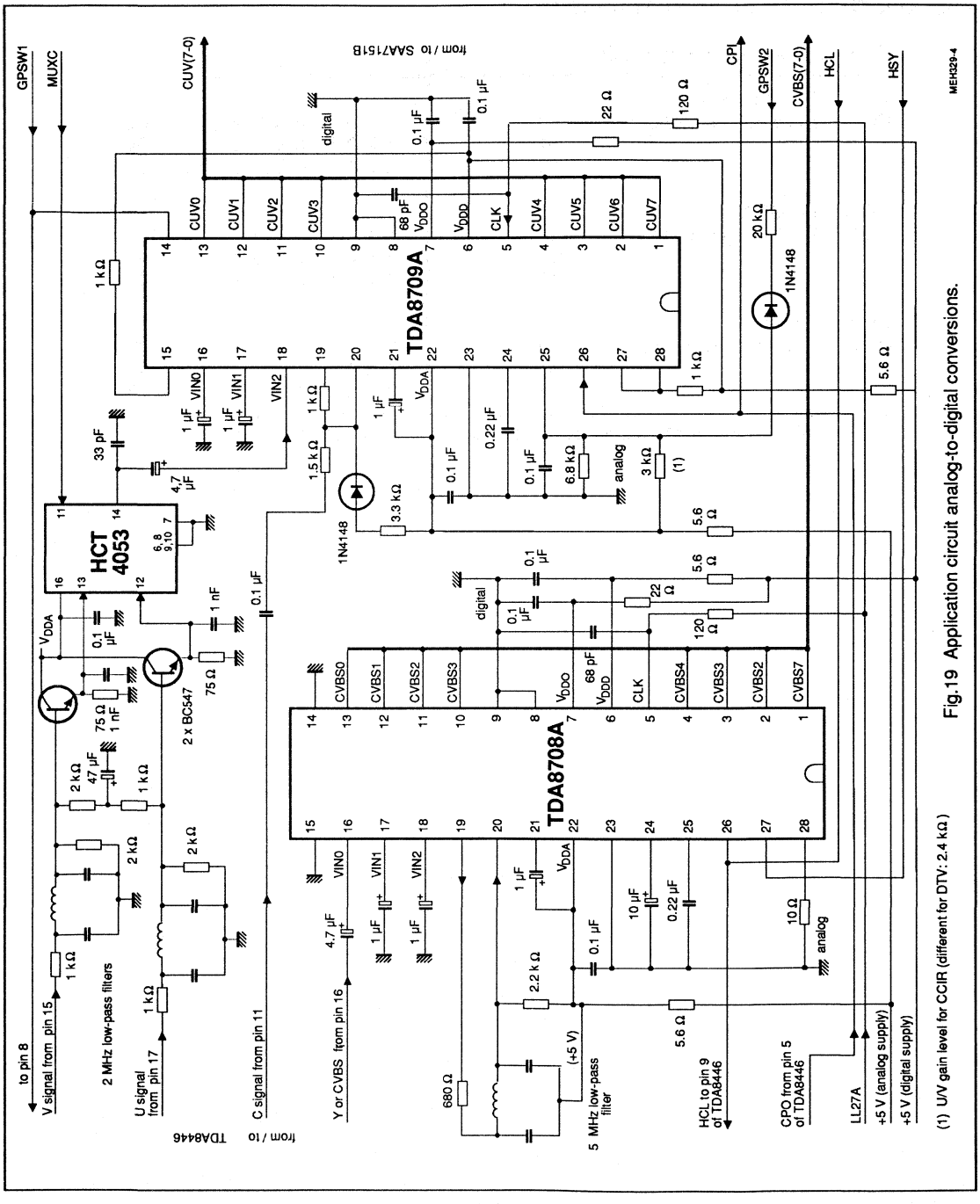


Fig.19 Application circuit analog-to-digital conversions.

(1) U/V gain level for CCIR (different for DTV: 2.4 kΩ)

Remarks to Fig.18: I²C-bus software for TDA8540.

I²C-bus address byte (write) = 90h			
Y/C input (pins 6 and 10):			
I²C-bus data byte for subaddress	00	1 1 0 1 0 0 1 0	D2
	01	1 0 0 1 0 4 0 0	94
	10	0 0 0 0 0 1 1 1	07
CVBS input (pin 8):			
I²C-bus data byte for subaddress	00	1 1 0 1 0 1 0 1	05
	01	1 0 0 1 0 1 0 0	94
	10	0 0 0 0 0 1 1 1	07
SYNC input (pin 12):			
I²C-bus data byte for subaddress	00	1 1 0 1 0 1 1 1	D7
	01	1 0 0 1 0 1 0 0	94
	10	0 0 0 0 0 0 1 1	03

X bits to set audio control bits (D0 for output pin 2; D1 for output pin 17)

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A		DATAn	A	P

S = start condition
SLAVE ADDRESS = **1000 101X** (IICSA = LOW) **or 1000 111X** (IICSA = HIGH)
A = acknowledge, generated by the slave
SUBADDRESS* = subaddress byte (Table 4)
DATA = data byte (Table 4)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 4 I²C-bus; DATA for status byte (X in address byte = 1).

FUNCTION		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
status byte		STTC	HLCK	FIDT	FSST1	FSST0	CDET2	CDET1	CDET0

Function of the bits:

STTC	Status time constant:	0 = TV mode; 1 = VCR mode
HLCK	Horizontal PLL information:	0 = HPLL locked; 1 = HPLL unlocked
FIDT	Field information:	0 = 50 Hz system detected; 1 = 60 Hz system detected

FSST1 to FSST0 — Fast swiching output mode:

FSST1	FSST0	mode
0	0	RGB; FSI = HIGH (pin 68)
0	1	Y/C; FSI = LOW (pin 68)
1	0	fast switching (toggle)
1	1	not used

CDET2 to CDET0 — Identified colour standard

CDET2	CDET2	CDET2	standard
0	0	0	PAL-B/G, -H, -I; 50 Hz
0	0	1	PAL-N; 50 Hz
0	1	0	SECAM; 50 Hz
0	1	1	PAL-M; 60 Hz
1	0	0	PAL 4.43; 60 Hz
1	0	1	NTSC-M; 60 Hz
1	1	0	NTSC 4.43; 60 Hz
1	1	1	black/white

Table 5 I²C-bus; subaddress and data bytes for writing (X in address byte = 0).

function	subaddress byte	data byte D7	D6	D5	D4	D3	D2	D1	D0
increment delay	00	IDEL7	IDEL6	IDEL5	IDEL4	IDEL3	IDEL2	IDEL1	IDEL0
H-sync HSY begin	01	HSYB7	HSYB6	HSYB5	HSYB4	HSYB3	HSYB2	HSYB1	HSYB0
H-sync HSY stop	02	HSYS7	HSYS6	HSYS5	HSYS4	HSYS3	HSYS2	HSYS1	HSYS0
H-clamp HCL begin	03	HCLB7	HCLB6	HCLB5	HCLB4	HCLB3	HCLB2	HCLB1	HCLB0
H-clamp HCL stop	04	HCLS7	HCLS6	HCLS5	HCLS4	HCLS3	HCLS2	HCLS1	HCLS0
H-sync after PHI1	05	HPHI7	HPHI6	HPHI5	HPHI4	HPHI3	HPHI2	HPHI1	HPHI0
luminance control	06	BYPS	PREF	BPSS1	BPSS0	BFBY	CORI	APER1	APER0
hue control	07	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
control #1	08	CSTD2	CSTD1	CSTD0	CKTQ4	CKTQ3	CKTQ2	CKTQ1	CKTQ0
control #2	09	OSCE	LFIS1	LFIS0	CKTS4	CKTS3	CKTS2	CKTS1	CKTS0
PAL switch sensitivity	0A	PLSE7	PLSE6	PLSE5	PLSE4	PLSE3	PLSE2	PLSE1	PLSE0
SECAM switch sensitivity	0B	SESE7	SESE6	SESE5	SESE4	SESE3	SESE2	SESE1	SESE0
control #3	0C	FSAU	GPSI2	GPSI1	CGFX	AMPF3	AMPF2	AMPF1	AMPF0
control #4	0D	COLO	CHSB	GPSW0	SUVI	SXCR	FSDL2	FSDL1	FSDL0
control #5	0E	CCIR	COFF	OEHS	OEVS	UVSS	CHRS	CDMO	CDPO
control #6	0F	AUFD	FSEL	HPLL	SCEN	VTRC	MUIV	FSIV	WIND
control #7	10	ASTD	OFTS	IPBP	CDVI	YDEL3	YDEL2	YDEL1	YDEL0
chroma gain reference	11	CHCV7	CHCV6	CHCV5	CHCV4	CHCV3	CHCV2	CHCV1	CHCV0
control #8	12	OEDY	OEDC	VNOI1	VNOI0	BFON	BOFL2	BOFL1	BOFL0

Function of the bits of Table 5

IDEL7 to IDEL0 "00"

Increment delay time , step size = 2/ 13.5 MHz = 148 ns*

D7	D6	D5	D4	D3	D2	D1	D0	decimal multiplier	note
1	1	1	1	1	1	1	1	–1 to –110	minimum –148 ns
1	0	0	1	0	0	1	0		–16.3 µs (outside available range)
1	0	0	1	0	0	0	1	–111 to –214	–16.44 µs
0	0	1	0	1	0	1	0		–31.7 µs (maximum value at FSEL = 1)
0	0	1	0	1	0	0	1	–215	–31.85 µs (outside central counter range at FSEL = 1 **)
0	0	1	0	1	0	0	0	–216	–32.0 µs (maximum value at FSEL = 0 **)
0	0	1	0	0	1	1	1	–217 to –256	–32.148 µs (outside central counter range at FSEL = 0 **)
0	0	0	0	0	0	0	0		–37.9 µs (outside central counter **)

* an internal sign-bit A8 set to HIGH indicates that all values are always negative

** H-PLL does not operate in this condition; the system clock frequency is set to a value fixed by the last update and is within ±7.1 % of the nominal frequency.

HSYB7 to HSYB0
HSYS7 to HSYS0
"01" and "02"

Horizontal sync begin, step size = 1/ 13.5 MHz = 74 ns
Horizontal sync stop, step size = 1/ 13.5 MHz = 74 ns

D7	D6	D5	D4	D3	D2	D1	D0	decimal multiplier	note
1	0	1	1	1	1	1	1	191 to 1	–14.2 µs (maximum negative value)
0	0	0	0	0	0	0	1		–74 ns
0	0	0	0	0	0	0	0	0	0 equals reference value
1	1	1	1	1	1	1	1	–1 to –64	+74 ns
1	1	0	0	0	0	0	0		+4.7 µs

HCLB7 to HCLB0
HCLS7 to HCLS0
"03" and "04"

Horizontal clamp begin, step size = 1/ 13.5 MHz = 74 ns
Horizontal clamp stop, step size = 1/ 13.5 MHz = 74 ns

D7	D6	D5	D4	D3	D2	D1	D0	decimal multiplier	note
0	1	1	1	1	1	1	1	127 to 1	–9.4 µs (maximum negative value)
0	0	0	0	0	0	0	1		–74 ns
0	0	0	0	0	0	0	0	0	0 equals reference value
1	1	1	1	1	1	1	1	–1 to –128	+74 ns
1	0	0	0	0	0	0	0		+9.5 µs (maximum positive value)

HPHI7 to HPHI0
"05"

Horizontal sync start, step size = 4/ 13.5 MHz = 296 ns

D7	D6	D5	D4	D3	D2	D1	D0	decimal multiplier	note
0	1	1	1	1	1	1	1	+127 to +109	) forbidden (outside available central
0	1	1	0	1	1	0	1		) counter range)
0	1	1	0	1	1	0	0	+108 to +1	–32 µs (maximum negative value)
0	0	0	0	0	0	0	1		–0.296 ns
0	0	0	0	0	0	0	0	0	0 equals reference value
1	1	1	1	1	1	1	1	–1 to –107	+0.296 µs
1	0	0	1	0	1	0	1		+31.7 µs (maximum positive value)
1	0	0	1	0	1	0	0	–108 to –128	) forbidden (outside available central
1	0	0	0	0	0	0	0		) counter range)

BYPS
"06"

Input mode select bit: 0 = CVBS mode (chroma trap active)
1 = S-Video mode (chroma trap by-passed)

PREF

Use of pre-emphasis: 0 = pre-filter bypassed; 1 = pre-filter on

BPSS1 to BPSS0

Aperture bandpass to select different centre frequencies (Figures 23 to 38):

BPSS1	BPSS0	centre frequency
0	0	4.1 MHz
0	1	3.8 MHz
1	0	2.6 MHz
1	1	2.9 MHz

"06" continued

BFBY: Bandfilter bypass switching: 0 = bandfilter active; 1 = bandfilter bypassed

CORI: Coring function: 0 = coring off; 1 = ±1 LSB coring

APER1 to APER0: Aperture factor (Figures 23 to 38):

APER1	APER0	factor
0	0	0
0	1	0.25
1	0	0.5
1	1	1

HUE7 to HUE0 "07": Hue control from +178.6° to −180.0°, equals data bytes 7F to 80 (hex); 0° equals 00.

CSTD2 to CSTD0 "08": Forced colour standard of input signal;

CSTD2	CSTD1	CSTD0	standard
0	0	0	PAL-B/G, -H, -I; 50 Hz
0	0	1	PAL-N; 50 Hz
0	1	0	SECAM; 50 Hz
0	1	1	PAL-M; 60 Hz
1	0	0	PAL 4.43; 60 Hz
1	0	1	NTSC-M; 60 Hz
1	1	0	NTSC 4.43; 60 Hz
1	1	1	black/white

CKTQ4 to CKTQ0: Colour killer threshold QAM (PAL/NTSC):

CKTQ4	CKTQ3	CKTQ2	CKTQ1	CKTQ0	
1	1	1	1	1	−30 to −24 dB; equals "internal colour forced on
1	0	0	0	0	−24 dB to −18 dB
0	0	0	0	0	

OSCE "09": External UV offset compensation: 0 = disabled; 1 = enabled

LFIS1 to LFIS0: Gain control (AGC filter):

LFIS1	LFIS0	control of loop filter time constant
0	0	slow
0	1	medium
1	0	fast
1	1	actual gain, stored

CKTS4 to CKTS0: Colour killer threshold SECAM as previously described under CKTQ subaddress"08"

PLSE7 to PLSE0 "0A"

PAL switch sensitivity from LOW to HIGH (HIGH means immediate sequence correction), equals FF to 00 (hex), MEDIUM equals 80.

SESE7 to SESE0 "0B"

SECAM switch sensitivity from LOW to HIGH (HIGH means immediate sequence correction), equals FF to 00 (hex), MEDIUM equals 80.

FSAU; GPSI2, GPSI1 "0C"

Set port outputs (general purpose switching, internal)

FSAU	GPSI2	GPSI1	output GPSW2 (pin 25)	output GPSW1 (pin 24)
0	0	0	LOW	LOW
0	0	1	LOW	HIGH
0	1	0	HIGH	LOW
0	1	1	HIGH	HIGH
1	X	X	status bit FSST1 set	status bit FSST0 set

CGFX

Chrominance gain pre-determination: 0 = gain controlled via loop; 1 = gain set by AMPF-bits

AMPF3 to AMPF0

Chrominance amplification factor

AMPF3	AMPF2	AMPF1	AMPF0	gain
0	0	0	0	−6 dB
0	1	0	0	0 dB
0	1	0	1	+1.5 dB
.	.	.	.	+3 to +16.5 dB (approximately 1.5 dB steps)
1	1	1	1	+17 dB

COLO "0D"

Colour-on bit: 0 = on, dependent on colour-killer; 1 = forced colour-on.

CHSB

Chrominance (UV) output code: 0 = two's complement; 1 = straightly binary

GPSW0

General purpose port output (pin 63): 0 = LOW; 1 = HIGH (attention to SERI-bit of "0F")

SUVI

SECAM UV output signal polarity: 0 = U and V positive; 1 = U and V negative

SXCR

SECAM cross-colour reduction: 0 = off; 1 = on

FDSL2 to FDSL0

Fast switching delay adjustment in 37 ns steps:

FDSL2	FDSL1	FDSL0	delay
0	0	0	0
0	0	1	37 ns
0	1	0	74 ns
0	1	1	111 ns
1	0	0	−148 ns (negative delay)
1	0	1	−111 ns
1	1	0	−74 ns
1	1	1	−37 ns

CCIR "0E"	Set CCIR mode: 0 = digital TV mode (DTV); 1 = CCIR mode
COFF	Set colour off: 0 = colour on; 1 = colour off
OEHS	Enable horizontal sync output HS: 0 = output high-impedance; 1 = HS enabled
OEVS	Enable vertical sync output VS: 0 = output high-impedance; 1 = VS enabled
UVSS	Select UV pixel sample: 1 = first pixel after U/V signal has changed; 0 = second same pixel (free of crosstalk signals)
CHRS	S-Video input mode: 0 = chrominance signal from CVBS or CUV input and controlled by BYPS (subaddress 06); 1 = S-Video mode; chrominance signal from CUV input
CDMO, CDPO	Chrominance delay: CDMO = 0, CDPO = 0: no delay CDMO = 1, CDPO = X: –37 ns (negative delay) CDMO = 0, CDPO = 1: +37 ns
AUFD "0F"	Automatical field detection: 0 = field selection by microcomputer (FSEL-bit); 1 = automatical field detection by SAA7151A.
FSEL	Field select (AUFD-bit = 0): 0 = 50 Hz (625 lines); 1 = 60 Hz (525 lines)
HPLL	Horizontal PLL: 0 = PLL closed; 1 = PLL open, horizontal frequency fixed
SCEN	Sync and clamping pulse enable: 0 = HCL and HSY outputs HIGH (pins 29 and 31); 1 = HCL and HSY outputs active
VTRC	VTR/TV mode select: 0 = TV mode; 1 = VTR mode
MUIV	MUXC signal invertion: 0 = inverted; 1 = not inverted
FSIV	Fast switch input signal inversion: 0 = not inverted; 1 = inverted
WIND	Narrow fast switch window : 0 = off; 1 = on
ASTD "10"	Automatic standard switching: 0 = off; 1 = on
OFTS	Select output format: 0 = 4 : 1 : 1 format; 1 = 4 : 2 : 2 format.
IPBP	External UV signal interpolation filter: 0 = active; 1 = bypassed
CDVI	Chrominance PLL filter selection for: 0 = VTR or TV source; 1 = fast time constant for FSC-PLL (only for special applications)
YDEL3 to YDEL0	Luminance delay compensation in 37 ns steps: YDEL3 = 0, YDEL2 = 0, YDEL1 = 0, YDEL0 = 0 YDEL3 = 0, YDEL2 = 1, YDEL1 = 1, YDEL0 = 1: 0 to 259 ns (step 0 to 6) YDEL3 = 1, YDEL2 = 0, YDEL1 = 0, YDEL0 = 0 YDEL3 = 1, YDEL2 = 1, YDEL1 = 1, YDEL0 = 1: –296 to –37 ns (negative delay; step –8 to –1)

CHCV7 to CHCV0 — Chroma gain reference value

"11"

D7	D6	D5	D4	D3	D2	D1	D0	gain	
1	1	1	1	1	1	1	1	maximum gain	
	:				:			to	)
1	0	1	1	0	0	1	1	DTV level	) default programmed values
	:				:			to	) dependend on application
0	0	1	1	1	1	0	1	CCIR level	)
	:				:			to	)
0	0	0	0	0	0	0	0	minimum gain	

OEDY "12" — Enable Y signals on YUV-bus: 0 = output high-impedance; 1 = output active

OEDC — Enable UV signals on YUV-bus: 0 = output high-impedance; 1 = output active

VNOI1, VNOI0 — Vertical noise reduction mode:

VNOI1	VNOI0	mode
0	0	normal
0	1	searching
1	0	free-running
1	1	bypassed

BFON — Bottom flutter compensation switching: 0 = off; 1 = on (controlled by BOFL-bit)

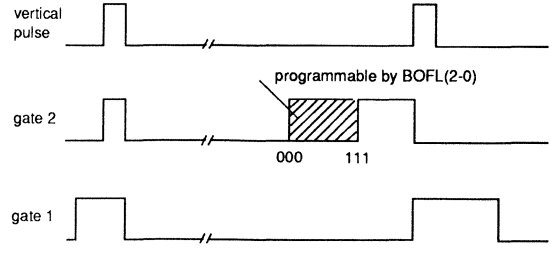
BOFL2 to BOFL0 — Bottom flutter compensation

BOFL2	BOFL1	BOFL0	start at line number
0	0	0	297 for PAL (247 for NTSC; active to end of field)
0	0	1	298 for PAL (248 for NTSC; active to end of field)
.	.	.	. .
1	1	0	303 for PAL (253 for NTSC; active to end of field)
1	1	1	304 for PAL (254 for NTSC; active to end of field)

The bottom flutter circuit is able to compensate for horizontal phase jump of up to ±16 µs.

Note: The bottom flutter gate is active at
- HPLL is locked
- HPLL in VTR mode
- the vertical noise limiter (VNL) is in the VTR mode
- gating is switched by BFON-bit = 1 (subaddress 12)

Gate 2	Gate 1	HPLL function
0	0	normal
1	0	disabled
0	1	double speed
1	1	unused



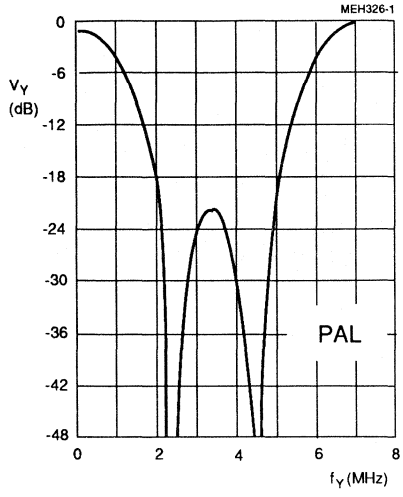


Fig.20 Frequency response of chroma stop filter in colour-difference mode for 50 Hz PAL controllable by subaddress byte 06.

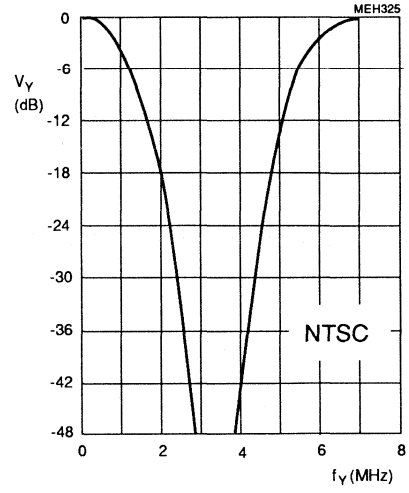


Fig.21 Frequency response of chroma stop filter in colour-difference mode for 60 Hz NTSC controllable by subaddress byte 06.

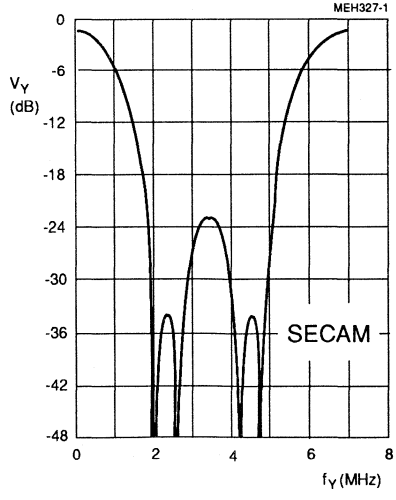


Fig.22 Frequency response of chroma stop filter in colour-difference mode for 50 Hz SECAM controllable by subaddress byte 06.

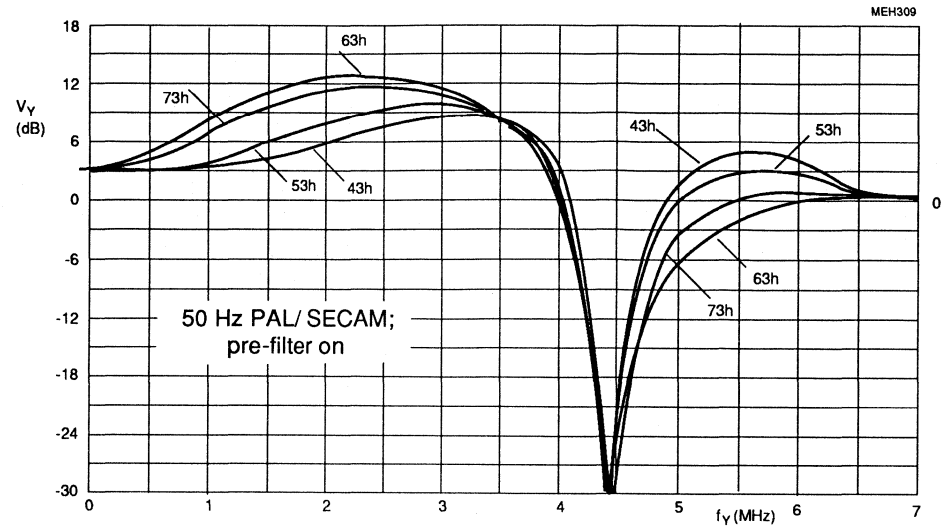


Fig.23 Maximum luminance peaking control as a function of four different aperture centre frequencies controllable by subaddress byte 06; aperture factor 1; coring off; chroma trap on; pre-filter on ; and bandfilter on.

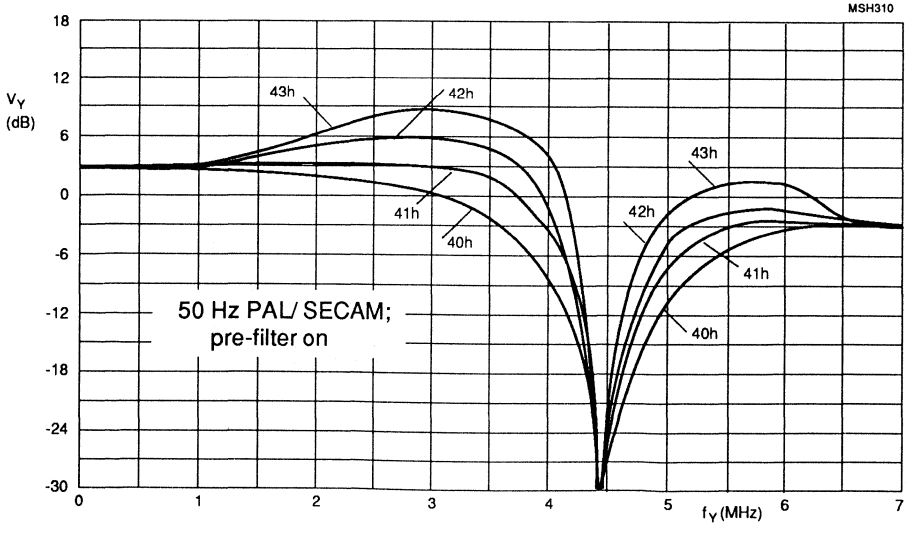


Fig.24 3.8 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; coring off; chroma trap on; pre-filter on and bandfilter on.

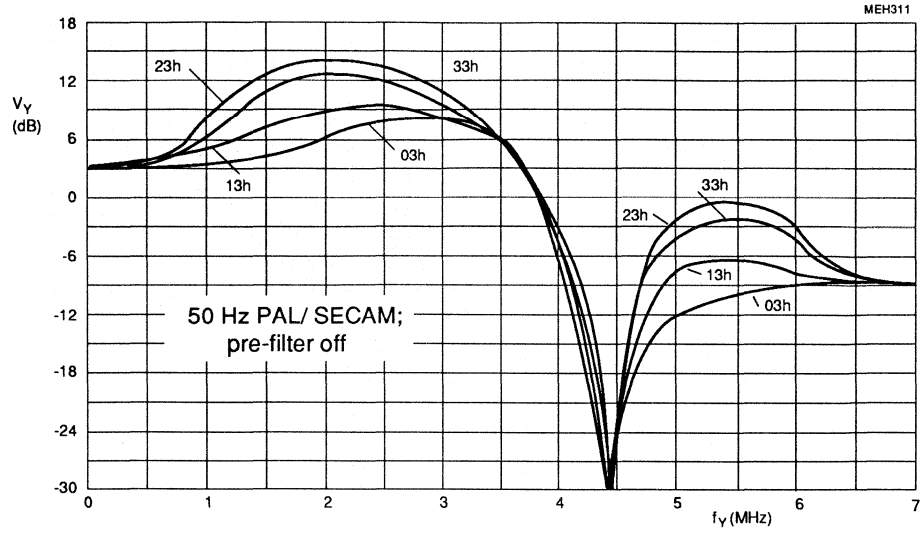


Fig.25 Maximum luminance peaking control as a function of four different aperture centre frequencies controllable by subaddress byte 06; aperture factor 1; coring off; chroma trap on; pre-filter off ; and bandfilter on.

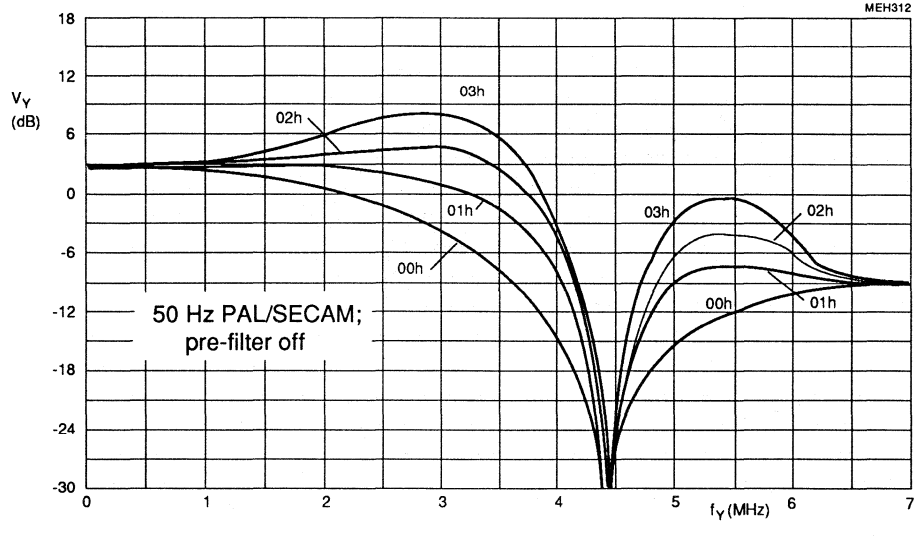


Fig.26 4.1 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; coring off; chroma trap on; pre-filter off and bandfilter on.

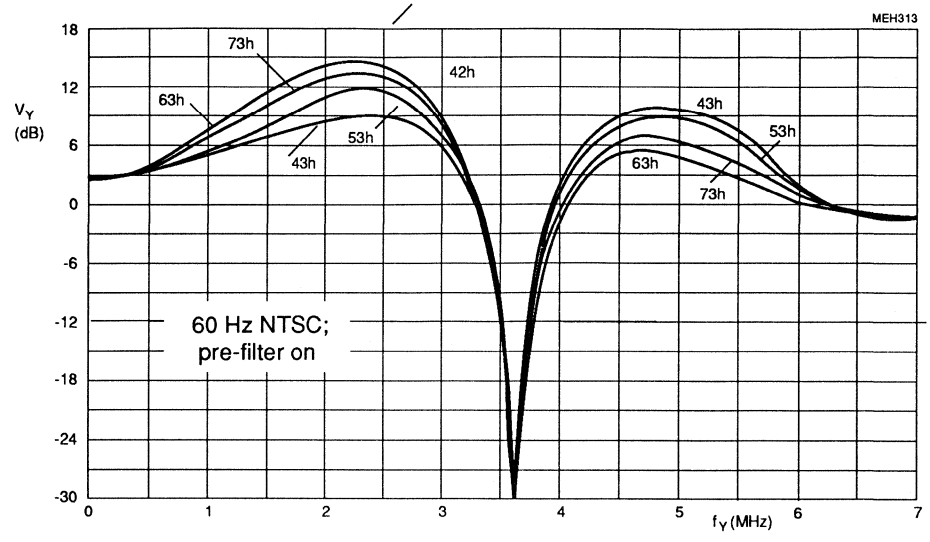


Fig.27 Maximum luminance peaking control as a function of four different aperture centre frequencies controllable by subaddress byte 06; aperture factor 1; coring off; chroma trap on; pre-filter on ; and bandfilter on.

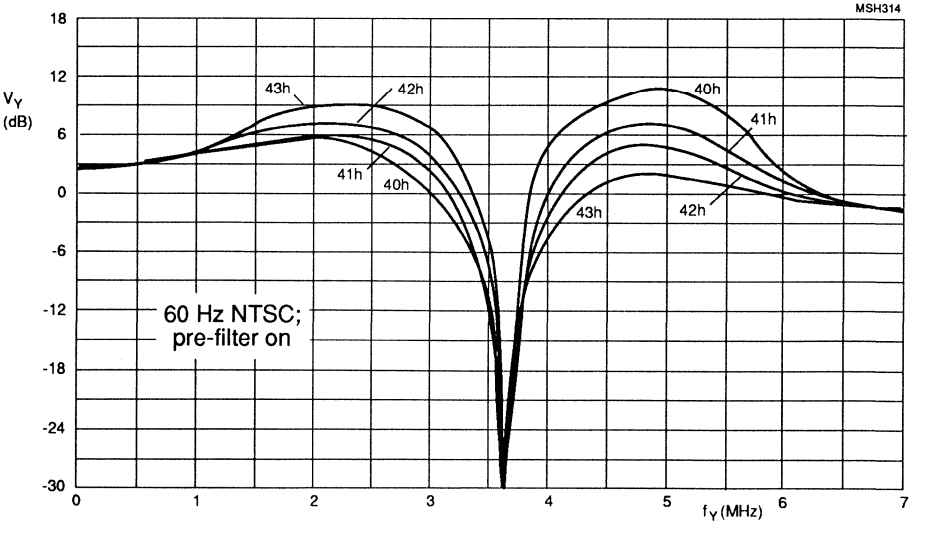


Fig.28 3.8 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; coring off; chroma trap on; pre-filter on and bandfilter on.

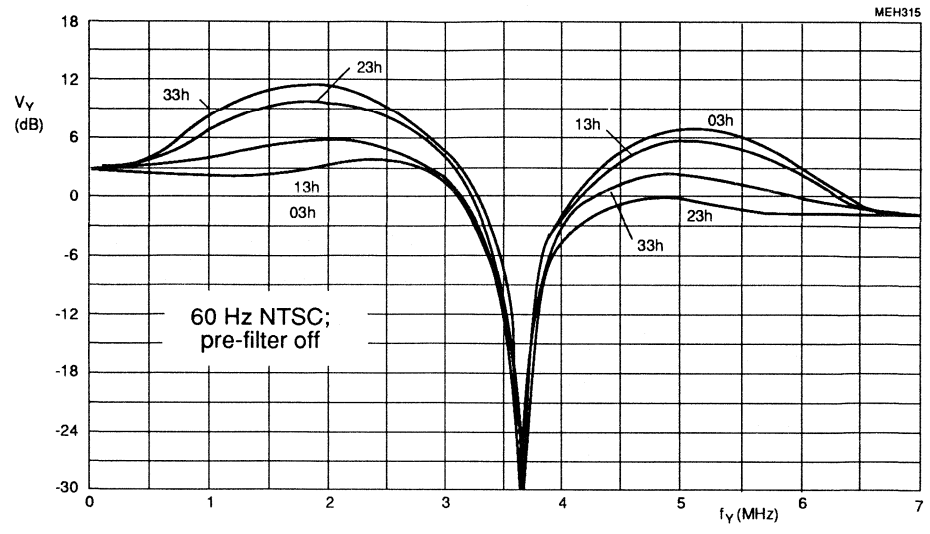


Fig.29 Maximum luminance peaking control as a function of four different aperture centre frequencies controllable by subaddress byte 06; aperture factor 1; coring off; chroma trap on; pre-filter off ; and bandfilter on.

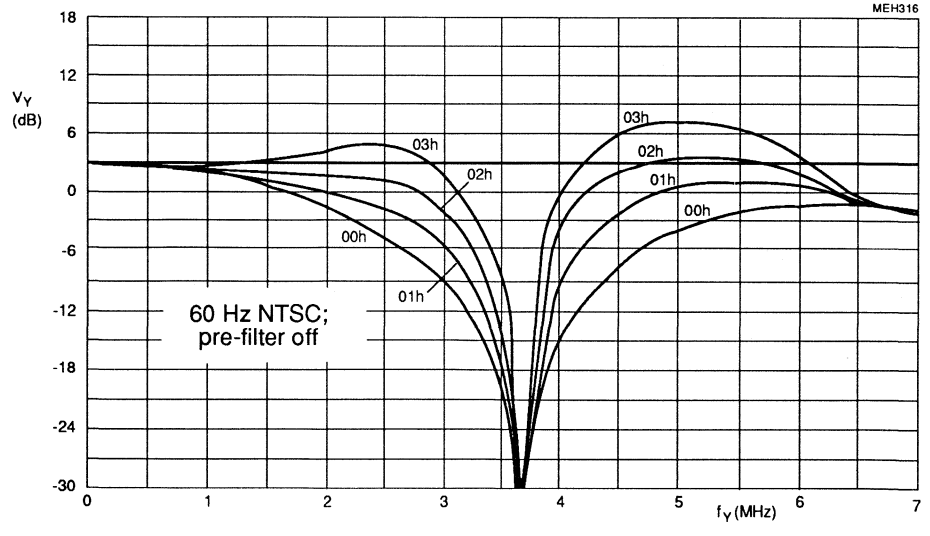


Fig.30 4.1 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; coring off; chroma trap on; pre-filter off and bandfilter on.

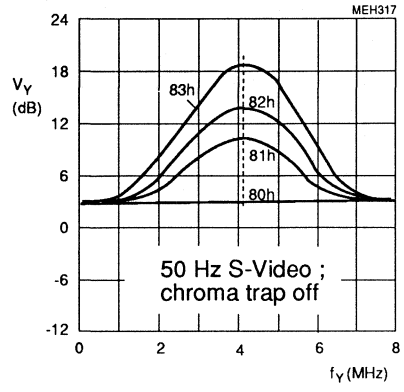


Fig.31 4.1 MHz luminance peaking control control as a function of four different aperture factors controllable by subaddress byte 06; pre-filter off; coring off and bandpass filter on.

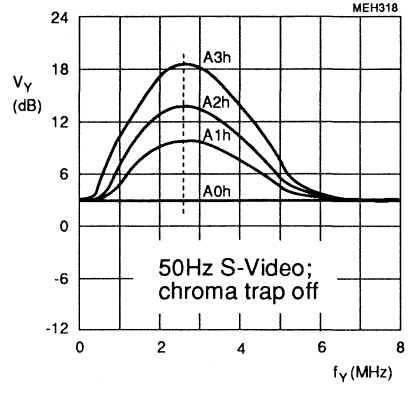


Fig.32 2.6 MHz luminance peaking control control as a function of four different aperture factors controllable by subaddress byte 06; pre-filter off; coring off and bandpass filter on.

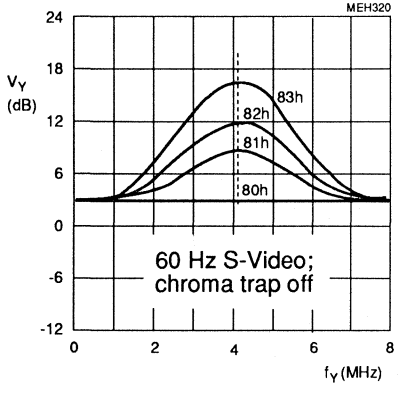


Fig.33 4.1 MHz luminance peaking control control as a function of four different aperture factors controllable by subaddress byte 06; pre-filter off; coring off and bandpass filter on.

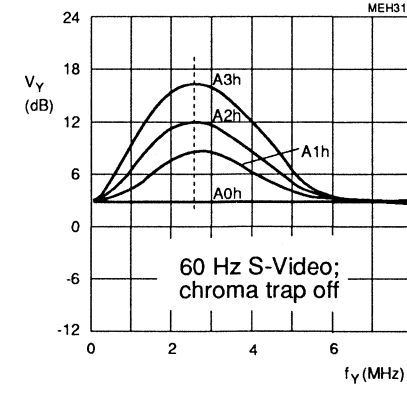


Fig.34 2.6 MHz luminance peaking control control as a function of four different aperture factors controllable by subaddress byte 06; pre-filter off; coring off and bandpass filter on.

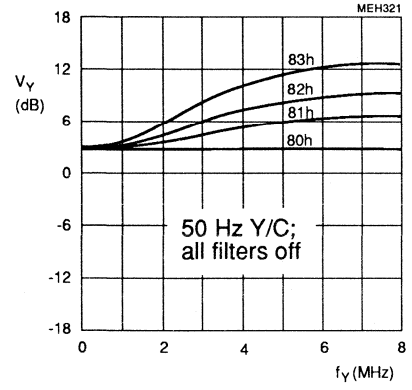


Fig.35 4.1 MHz luminance peaking control in 50 Hz / S-VHS mode as a function of four different aperture factors controllable by subaddress byte 06.

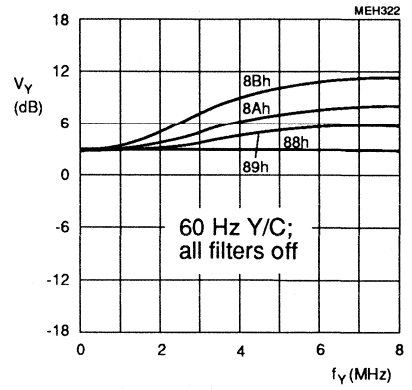


Fig.36 4.1 MHz luminance peaking control in 60 Hz / S-VHS mode as a function of four different aperture factors controllable by subaddress byte 06.

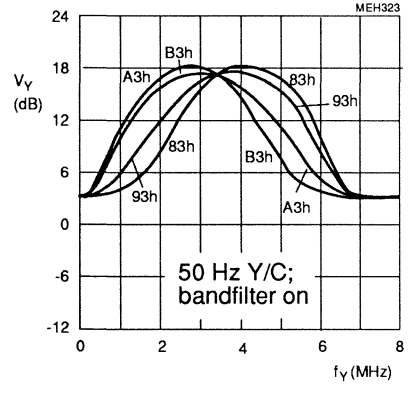


Fig.37 Maximum luminance peaking control in 50 Hz / S-VHS mode as a function of four aperture centre frequencies controllable by subaddress byte 06.

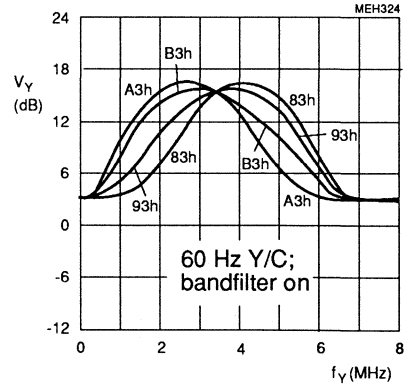
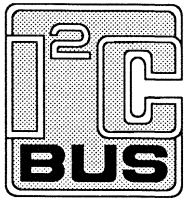


Fig.38 Maximum luminance peaking control in 60 Hz / S-VHS mode as a function of four aperture centre frequencies controllable by subaddress byte 06.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

PROGRAMMING EXAMPLE

Coefficients to set operation for application circuits Figures 17, 18 and 19. Values recommended for PAL CVBS input signal and 4:2:2 CCIR output signal (all numbers of the Table 6 are hex values).

Table 6 Recommended default values

SUBADDRESS	BIT NAME	FUNCTION	VALUE (HEX)
00	IDEL(7-0)	increment delay	4D
01	HSYB(7-0)	horizontal sync HSY begin	3D
02	HSYS(7-0)	horizontal sync HSY stop	0D
03	HCLB(7-0)	horizontal clamping HCL begin	F3
04	HCLS(7-0)	horizontal clamping HCL stop	C6
05	HPHI(7-0)	horizontal sync after PHI1	FB
06	BYPS, PREF, BPSS(1-0) BFBY, CORI, APER(1-0)	luminance control:	02
07	HUEC(7-0)	hue control (0 degree)	00
08	CSTD(2-0), CKTQ(4-0)	control #1	09
09	OSCE, LFIS(1-0),CKTS(4-0)	control #2	C0
0A	PLSE(7-0)	PAL switch sensitivity	4D
0B	SESE(7-0)	SECAM switch sensitivity	40
0C	FSAU, GPSI(2-1), CGFX, AMPF(3-0)	control #3	80
0D	COLO, CHSB, GPSW0, SUVI, SXCR, FSDL(2-0)	control #4	60
0E	CCIR, COEF, OEHS, OEVS UVSS, CHRS, CDMO, CDPO	control #5	B4
0F	AUFD, FSEL, HPLL, SCEN, VTRC, MUIV, FSIV, WIND	control #6	9F
10	ASTD, OFTS, IPBP, CDVI, YDEL(3-0)	control #7	C1
11	CHCV(7-0)	chrominance gain reference	3D
12	OEDY, OEDC, VNOI(1-0), BFON, BOFL(2-0)	control #8	C2

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	May 1992

SAA7157

Clock signal generator circuit for digital TV systems (SCGC)

FEATURES

- Clock generation suitable for digital TV systems (line-locked)
- PLL frequency multiplier to generate 4 times of input frequency
- Dividers to generate clocks LL1.5A, LL1.5B, LL3A and LL3B (4th and 2nd multiples of input frequency)
- PLL mode or VCO mode selectable
- Reset control and power fail detection
- Suitable for applications with feature box and picture memory

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8, 17)	4.5	5.0	5.5	V
I_{DDA}	analog supply current	3	-	9	mA
I_{DDD}	digital supply current	10	-	60	mA
V_{LFCO}	LFCO input voltage (peak-to-peak value)	1	-	V_{DDA}	V
f_i	input frequency range	6.0	-	7.25	MHz
V_I	input voltage LOW input voltage HIGH	0 2.0	- -	0.8 V_{DDD}	V V
V_O	output voltage LOW output voltage HIGH	0 2.6	- -	0.6 V_{DDD}	V V
T_{amb}	operating ambient temperature range	0	-	70	°C

GENERAL DESCRIPTION

The SAA7157 generates all clock signals required for a digital TV system suitable for the SAA715x family and the SAA7199B (DENC). The circuit operates in either the phase-locked loop mode (PLL) or voltage controlled oscillator mode (VCO).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7157	20	DIL	plastic	SOT146
SAA7157T	20	mini-pack (SO20)	plastic	SOT163A

Clock signal generator circuit for digital TV systems (SCGC)

SAA7157

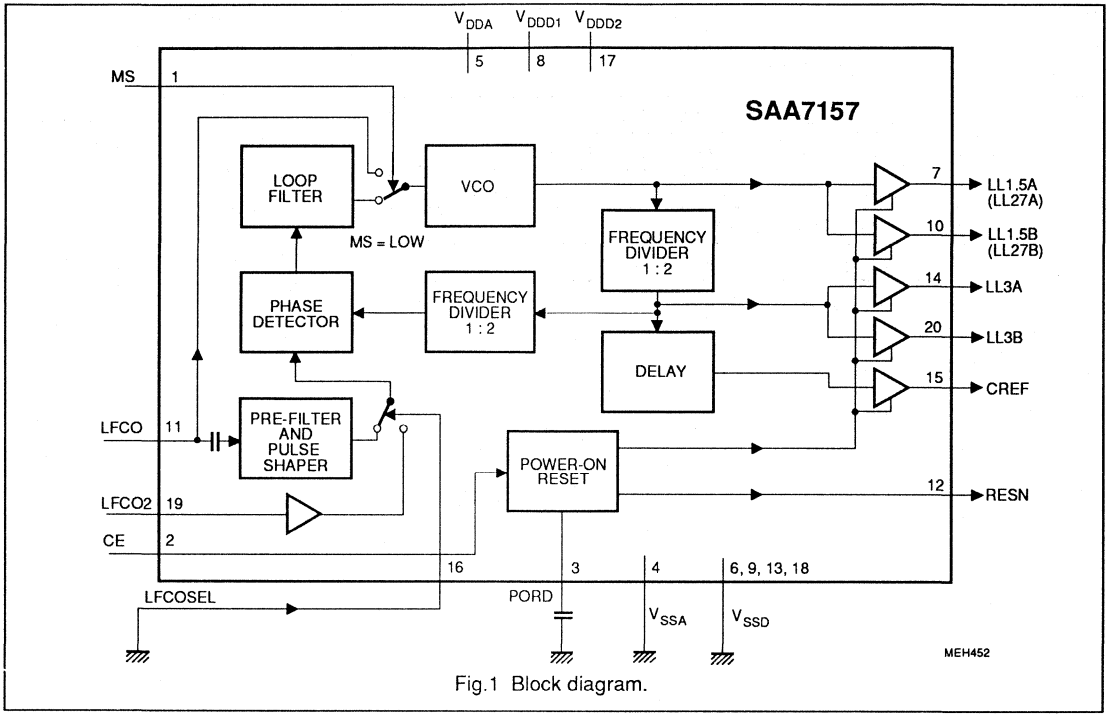


Fig.1 Block diagram.

FUNCTION DESCRIPTION

The SAA7157 generates all clock signals required for a digital TV system suitable for the SAA715x family consisting of an 8-bit analog-to-digital converter (ADC8), digital video multistandard decoder (DMSD2) and video enhancement and D/A processor circuit (VEDA). Optional extras (feature box, video memory etc.) can be driven via external buffers, advantageous for a digital TV system based on display standard conversion concepts.
The 6.75 MHz input signal LFCO (triangular waveform) coming from the DMSD or LFCO2 is multiplied to 27 MHz by the PLL (including phase detector, loop filter, VCO and frequency divider) and output on LL1.5A (pin7) and LL1.5B (pin 10). The 13.5 MHz frequencies are generated by dividers using ratio of 1:2 and are output on LL3A (pin 14) and LL3B (pin 20).

The rectangular output signals have 50 % duty factor. Outputs with equal frequency may be connected together externally. The clock outputs go HIGH during power-on reset (and chip enable) to ensure that no output clock signals are available before the PLL has locked-on.

Mode select MS

The LFCO input signal is directly connected to the VCO at MS = HIGH. The circuit operates as an oscillator and frequency divider. This function is not tested.

Source select LFCOSEL

Line frequency control signal (LFCO) is selected by LFCOSEL input.
LFCOSEL = LOW:
signal from LFCO (pin 11) is selected.
LFCOSEL = HIGH:
signal from LFCO2 (pin 19) is selected.
This function is not tested.

Chip enable CE

The buffer outputs are enabled and RESN is set to HIGH by CE = HIGH (Fig.4).
CE = LOW sets the clock outputs HIGH and RESN output LOW.

CREF output

TV2 digital clock reference output signal. Clock qualifier signal to TV system with 2 times of LFCO or LFCO2 frequency.

Power-on reset

Power-on reset is activated at power-on, when the supply voltage decreases below 3.5 V (Fig.4) or when chip enable is done. The indicator output RESN is LOW for a time determined by capacitor on pin 3. The RESN signal can be applied to reset other circuits of this digital TV system.
The LFCO or LFCO2 input signals have to be applied before RESN becomes HIGH.

Clock signal generator circuit for digital TV systems (SCGC)

SAA7157

PINNING

SYMBOL	PIN	DESCRIPTION
MS	1	mode select input (LOW = PLL mode)
CE	2	chip enable /reset (HIGH = outputs enabled)
PORD	3	power-on reset delay, dependent on external capacitor
V_{SSA}	4	analog ground (0 V)
V_{DDA}	5	analog supply voltage (+5 V)
V_{SSD1}	6	digital ground 1 (0 V)
LL1.5A	7	line-locked clock output signal 1.5A (4 times f_{LFCO})
V_{DDD1}	8	digital supply voltage 1 (+5 V)
V_{SSD2}	9	digital ground 2 (0 V)
LL1.5B	10	line-locked clock output signal 1.5B (4 times f_{LFCO})
LFCO	11	line-locked frequency control input signal 1
RESN	12	reset output (active-LOW, Fig.4)
V_{SSD3}	13	digital ground 3 (0 V)
LL3A	14	line-locked clock output signal 3A (2 times f_{LFCO})
CREF	15	clock reference output, qualifier signal (2 times f_{LFCO})
LFCOSEL	16	LFCO source select (LOW = LFCO selected)*
V_{DDD2}	17	digital supply voltage 2 (+5 V)
V_{SSD4}	18	digital ground 4 (0 V)
LFCO2	19	line-locked frequency control input signal 2*
LL3B	20	line-locked clock output signal 3B (2 times f_{LFCO})

PIN CONFIGURATION

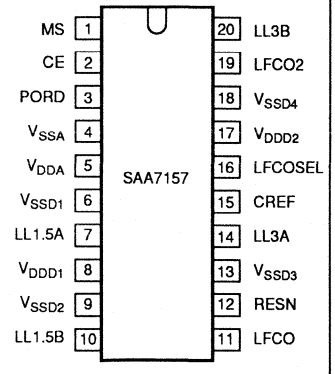


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); ground pins as well as supply pins together connected.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	−0.5	7.0	V
V_{DDD}	digital supply voltage (pins 8 and 17)	−0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{DDA} - V_{DDD}$	-	±100	mV
V_O	output voltage (I_{OM} = 20 mA)	−0.5	V_{DDD}	V
P_{tot}	total power dissipation (DIL20)	0	1.1	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling** for all pins	-	tbf	V

* MS and LFCO2 functions are not tested. LFCO2 is a multiple of horizontal frequency.

** Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take normal handling precautions appropriate to "Handling MOS devices ".

CHARACTERISTICS

V_{DDA} = 4.5 to 5.5 V; V_{DDD} = 4.5 to 5.5 V; f_{LFCO} = 6.0 to 7.25 MHz and T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8 and 17)		4.5	5.0	5.5	V
I_{DDA}	analog supply current (pin 5)		3	-	9	mA
I_{DDD}	digital supply current ($I_8 + I_{17}$)	note 1	10	-	60	mA
V_{reset}	power-on reset threshold voltage	Fig.4	-	3.5	-	V
Input LFCO (pin 11)						
V_{11}	DC input voltage		0	-	V_{DDA}	V
V_i	input signal (peak-to-peak value)		1	-	V_{DDA}	V
f_{LFCO}	input frequency range		6.0	-	7.25	MHz
C_{11}	input capacitance		-	-	10	pF
Inputs MS, CE, LFCOSEL and LFCO2 (pins 1, 2, 16 and 19); note 3						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}	V
f_{LFCO2}	input frequency range for LFCO2		6.0	-	7.25	MHz
I_{LI}	input leakage current	LFCOSEL	50	-	150	µA
		others	-	-	10	µA
C_I	input capacitance		-	-	5	pF
Output RESN (pin 12)						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −0.5 mA	2.4	-	V_{DDD}	V
t_d	RESN delay time	C_3 = 0.1µF; Fig.4	20	-	200	ms
Output CREF (pin 15)						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	-	0.6	V
V_{OH}	output voltage HIGH	I_{OH} = −0.5 mA	2.4	-	V_{DDD}	V
f_{CREF}	output frequency CREF	Fig.3	-	2 $f_{LFCO(2)}$		MHz
C_L	output load capacitance		15	-	40	pF
t_{SU}	set-up time	Fig.3; note 1	12	-	-	ns
t_{HD}	hold time	Fig.3; note 1	4	-	-	ns
Output signals LL1.5A, LL1.5B, LL3A and LL3B (pins 7, 10, 14, and 20); note 3						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	-	0.6	V
V_{OH}	output voltage HIGH	I_{OH} = −0.5 mA	2.6	-	V_{DDD}	V
t_{comp}	composite rise time	Fig.3; notes 1 and 2	-	-	8	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{LL}	output frequency LL1.5A	Fig.3	-	4 $f_{LFCO(2)}$		MHz
	output frequency LL1.5B		-	4 $f_{LFCO(2)}$		MHz
	output frequency LL3A		-	2 $f_{LFCO(2)}$		MHz
	output frequency LL3B		-	2 $f_{LFCO(2)}$		MHz
t_r, t_f	rise and fall times	note 1; Fig.3	-	-	5	ns
t_{LL}	duty factor LL1.5A, LL1.5B, LL3A and LL3B (mean values)	note 1; Fig.3; at 1.5 V level	43	50	57	%

Notes to the characteristics

1. f_{LFCO} = 7.0 MHz and output load 40 pF (Fig.3). V_{SSA} and V_{SSD} short connected together.
2. t_{comp} is the rise time from LOW of all clocks to HIGH of all clocks (Fig.3) including rise time, skew and jitter components. Measurements taken between 0.6 V and 2.6 V. Skew between two LLx clocks will not deviate more than ±2 ns if output loads are matched within 20 %.
3. MS and LFCO2 functions not tested.

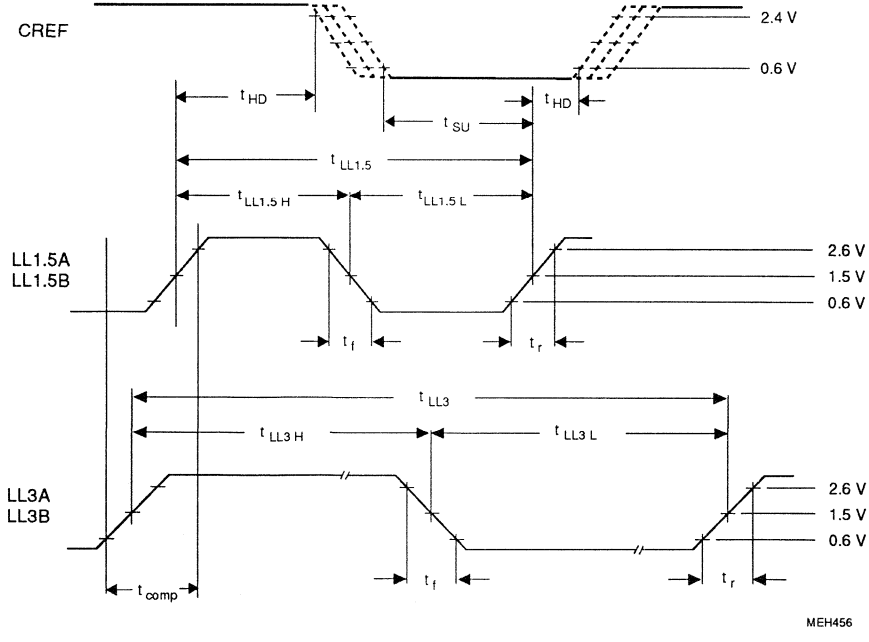


Fig.3 Output timing.

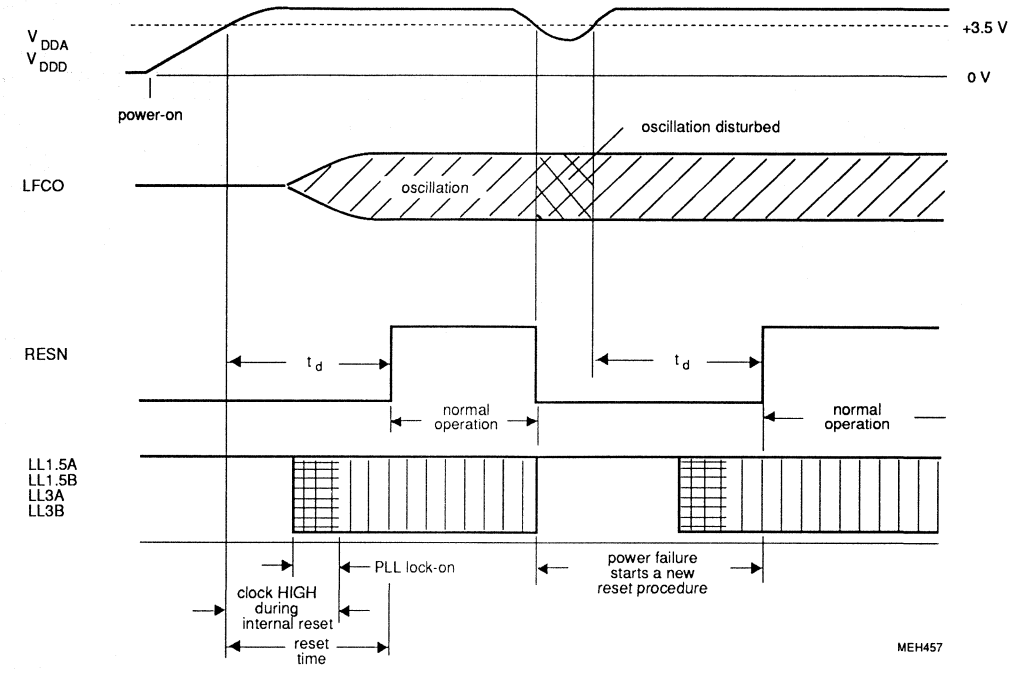


Fig.4 Reset procedure.

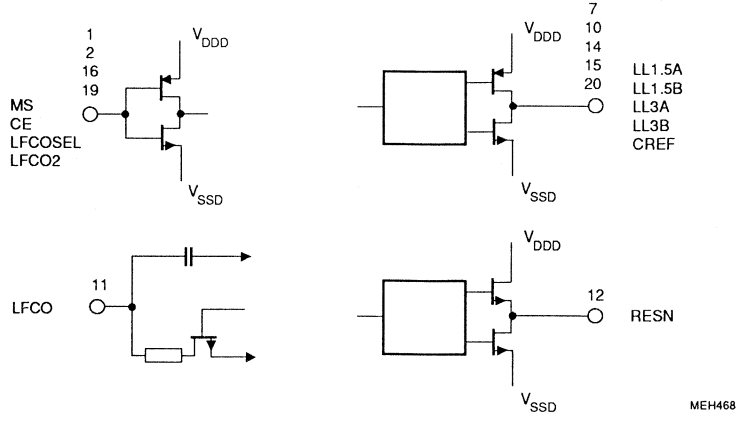
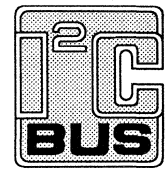


Fig.5 Internal circuit.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	May 1992

SAA7165
Video enhancement and D/A processor (VEDA2)



FEATURES

- CMOS circuit to enhance video data and to convert luminance and colour-difference signals from digital-to-analog
- Digital colour transient improvement block DCTI to increase the sharpness of colour transitions. The improved pin-compatible SAA7165 can supercede the SAA9065.
- 16-bit parallel input for YUV-bus
- Data clock input LLC (line-locked clock) for a data rate up to 30 MHz
- 8-bit luminance and 8-bit multiplexed colour-difference formats (optional 7-bit formats)
- MC input to enable input data, suitable for synchronization from an external source with a lower clock (LLC/2)
- Formatter for YUV input data; 4:2:2 format, 4:1:1 format and filter characteristics selectable
- HREF input to determine the active line (number of pixels)
- Controllable peaking of luminance signal to enhance internal data to 11 bits (signal improvement)
- Coring stage with controllable threshold to eliminate noise in luminance signal
- Interpolation filter suitable for both formats to increase the data rate in chrominance path
- Polarity of colour-difference signals selectable
- All functions controlled via I²C-bus

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	supply voltage digital part	4.5	5	5.5	V
V_{DDA}	supply voltage analog part	4.75	5	5.25	V
I_{DD}	total supply current	-	tbf	-	mA
$V_{I\,L}$	input voltage LOW on YUV-bus	−0.5	-	0.8	V
$V_{I\,H}$	input voltage HIGH on YUV-bus	2	-	V_{DDD}+0.5	V
f_{LLC}	maximum input data rate	30	-	-	MHz
$V_{o\,Y,CD}$	output signal Y, ±(R–Y) and ±(B–Y) (peak-to-peak value)	-	2	-	V
$R_{L\,Y,CD}$	output load resistance	125	-	-	Ω
ILE	DC integral linearity error in output signal (8-bit data)	-	-	1	LSB
DLE	DC differential error in output signal (8-bit data)	-	-	0.5	LSB
T_{amb}	operating ambient temperature range	0	-	70	°C

- Separate digital-to-analog converters (9-bit solution for Y; 8-bit for colour-difference signals)
- 1 V (p-p)/ 75 Ω outputs realized by two resistors
- No external adjustments

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7165	44	PLCC	plastic	SOT187

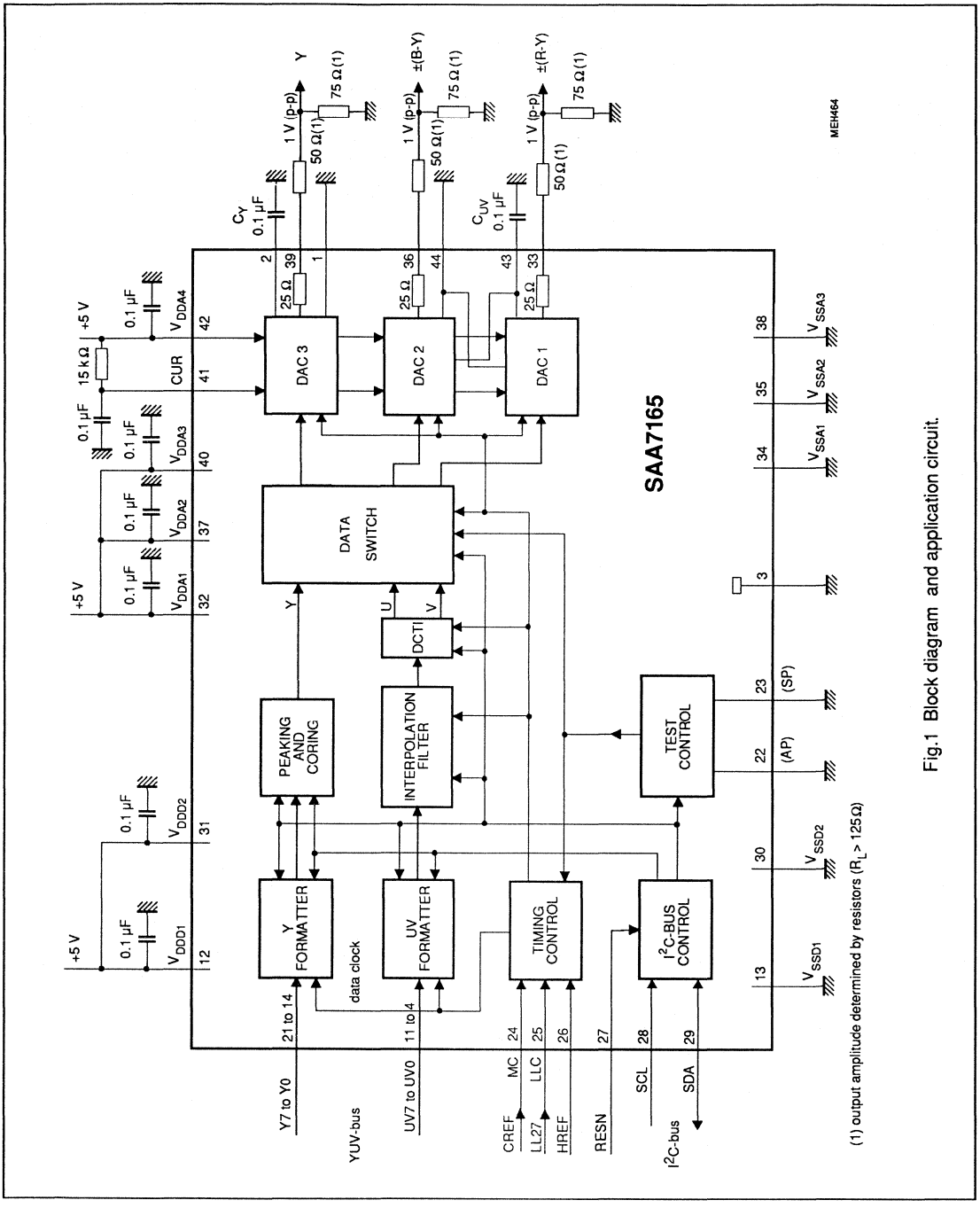


Fig.1 Block diagram and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
$REFL_Y$	1	low reference of luminance DAC (connected to V_{SSA1})
C_Y	2	capacitor for luminance DAC (high reference)
SUB	3	substrate (connected to V_{SSA1})
UV0	4	UV signal input bits UV7 to UV0 (digital colour-difference signal)
UV1	5	
UV2	6	
UV3	7	
UV4	8	
UV5	9	
UV6	10	
UV7	11	
V_{DDD1}	12	+5 V digital supply voltage 1
V_{SSD1}	13	digital ground 1 (0 V)
Y0	14	Y signal input bits Y7 to Y0 (digital luminance signal)
Y1	15	
Y2	16	
Y3	17	
Y4	18	
Y5	19	
Y6	20	
Y7	21	
AP	22	connected to ground (action pin for testing)
SP	23	connected to ground (shift pin for testing)
MC	24	data clock CREF (13.5 MHz e. g.); at MC = HIGH the LLC divider-by-two is inactive
LLC	25	line-locked clock signal (LL27 = 27 MHz)
HREF	26	data clock for YUV data inputs (for active line 768Y or 640Y long)
RESN	27	reset input (active LOW)
SCL	28	I^2C-bus clock line
SDA	29	I^2C-bus data line
V_{SSD2}	30	digital ground 2 (0 V)
V_{DDD2}	31	+5 V digital supply voltage 2
V_{DDA1}	32	+5 V analog supply voltage for buffer of DAC 1
(R–Y)	33	±(R–Y) output signal (analog signal)
V_{SSA1}	34	analog ground 1 (0 V)

SYMBOL	PIN	DESCRIPTION
V_{SSA2}	35	analog ground 2 (0 V)
(B–Y)	36	±(B–Y) output signal (analog colour-difference signal)
V_{DDA2}	37	+5 V analog supply voltage for buffer of DAC 2
V_{SSA3}	38	analog ground 3 (0 V)
Y	39	Y output signal (analog luminance signal)
V_{DDA3}	40	+5 V analog supply voltage for buffer of DAC 3
CUR	41	current input for analog output buffers
V_{DDA4}	42	supply and reference voltage for the three DACs
C_{UV}	43	capacitor for chrominance DACs (high reference)
$REFL_{UV}$	44	low reference of chrominance DACs (connected to V_{SSA1})

PIN CONFIGURATION

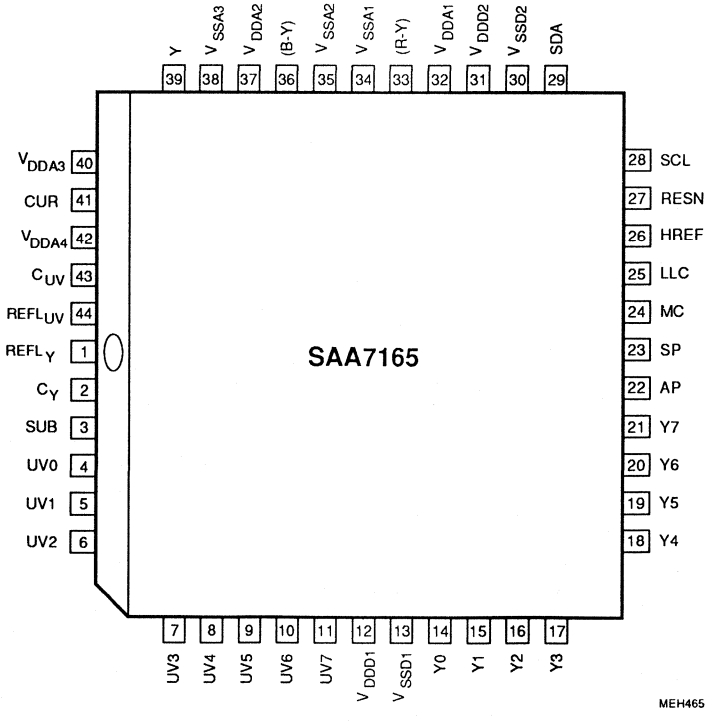


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The CMOS circuit SAA7165 processes digital YUV-bus data up to a data rate of 30 MHz. The data inputs Y7 to Y0 and UV7 to UV0 (Fig.1) are provided with 8-bit data. The data of digital colour-difference signals U and V are in a multiplexed state (serial in 4:2:2 or 4:1:1 format; Tables 2 and 3).

Data is read with the rising edge of LLC (line-locked clock) to achieve a data rate of LLC at MC = HIGH only. If MC is supplied with the frequency CREF (LLC/2 for example), data is read only at every second rising edge (Fig.3).The 8-bit input data can be reduced to 7-bit data words by means of the R78-bit (R78 = 0). Additionally, the luminance data format is converted for internal use into a two's complement format by inverting MSB. The Y input byte (bits Y7 to Y0) represent pixel information; the UV input byte (bits UV7 to UV0) one of the two digital colour-difference signals in 4:2:2 format (Table 2).

The HREF input signal (HREF = HIGH) determines the start and the end of an active line (Fig.3) the number of pixels respectively . The analog output Y is blanked at HREF = LOW, the ±(B–Y) and ±(R–Y) outputs are in a colourless state. The blanking level can be set by the BLV-bit. Nearly all characteristics are controllable via the I²C-bus

Y and UV formatters

The input data formats are formatted into the internally used processing formats (separate for 4:2:2 and 4:1:1 formats) employing a defined delay and a multiplexer cascade. The signals are prepared for interpolation, and the IFF, IFC and IFL bits switch to the input data format and determine the right interpolation filter (Figures 10 to 13).

Peaking and coring

Peaking is applied to the Y signal to compensate several bandwidth reductions of the previous analog receiver part. Y signals can be improved to obtain a better sharpness.

There are the two switchable bandpass filters BF1 and BF 2 controlled via the I²C-bus by the bits BP1, BP0 and BFB. Thus, a frequency response is achieved in combination with the peaking factor K (Figures 5 to 9; K is determined by the bits BFB, WG1 and WG0).

The coring stage with controllable threshold (4 states controlled by CO1 and CO0 bits) reduces noise disturbances (generated by the bandpass gain) by suppressing the amplitude of small signal components. The remaining high-frequent peaking component is available for a weighted addition after coring.

Table 1 LLC and MC configuration modes in DMSD applications

PIN	INPUT SIGNAL	COMMENT
LLC MC	LLC (LL27) CREF	The data rate on YUV-bus is half the clock rate on pin LLC, e. g. in SAA7151B, SAA7191 and SAA7191B single scan operation.
LLC MC	LLC (LL27) MC = HIGH	The data rate on YUV-bus must be identical to the clock rate on pin LLC, e. g. in double scan applications.
LLC MC	LLC2/LL3 MC = HIGH	The data rate on YUV-bus must be identical to the clock rate on pin LLC, e. g. SAA9051 single scan operation.
Note: YUV data are only latched with the rising edge of LLC at MC = HIGH.		

Table 2 Data format 4 : 2 : 2. (Fig.3)

INPUT	PIXEL BYTE SEQUENCE					
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7(MSB)	U7	V7	U7	V7	U7	V7
Y frame	0	1	2	3	4	5
UV frame	0		2		4	

Note to Table 2

The quoted frequencies are valid on the YUV-bus. The time frames are controlled by the HREF signal.

Interpolation

The chrominance interpolation filter consists of various filter stages, multiplexers and de-multiplexers to increase the data rate of the colour-difference signals by a factor of 2 or 4. The switching of the filters by the bits IFF, IFC and IFL is described previously. Additional signal samples with significant amplitudes between two consecutive signal samples of the low data rate are generated. The time-multiplexed U and V samples are stored in parallel for converting.

Data switch

The digital signals are switched by the timing control, then adapted to the conversation range. U and V data have 8-bit formats again; Y can have 9 bits dependent on peaking. Blanking and switching to colourless level is applied here. Bits can be inverted by INV-bit to change the polarity of colour-difference output signals.

Digital colour transient improvement (DCTI)

The DCTI circuit improves the transition behaviour of the UV colour-difference signals. As the CVBS signal allows for a 4 : 1 : 1 bandwidth representation only, the DCTI improves the transients to the same performance as signals coming from a 4 : 2 : 2 source – or even more.
In order to obtain the point of inflection, the second derivative of the signal is calculated. The improved transition is centered with respect to the point of inflection of the original signal. Thus, there is no horizontal shift of the resulting signal.

The transition area length to be improved is controlled via I²C-bus by the bits LI1 and LI0 (Table 4); the sensitivity of the DCTI block is controlled by the bits GA1 and GA0. The CMO bit controls the colour detail sensitivity. It should be set to 1 (ON) if the video signal contains fine colour details (recommended operation mode).

Digital-to-analog converters

Conversion is separate for Y, U and V. The converters use resistor chains with low-impedance output buffers. The minimum output voltage is 200 mV to reduce integral non-linearity errors. The analog signal, without load on output pin, is between 0.2 and 2.2 V floating. An application for 1 V/ 75 Ω on outputs is shown in Fig.1.

Each digital-to-analog converter has its own supply and ground pins suitable for decoupling. The reference voltage, supplying the resistor chain of all three DACs, is the supply voltage V_{DDA4}. The current into pin 41 is 0.3 mA ; a larger current improves the bandwidth but increases the integral non-linearity.

Table 3 Data format 4 : 1 : 1

INPUT	PIXEL BYTE SEQUENCE							
Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0	0	0	0	0	0	0	0	0
UV1	0	0	0	0	0	0	0	0
UV2	0	0	0	0	0	0	0	0
UV3	0	0	0	0	0	0	0	0
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7	U7	U5	U3	U1	U7	U5	U3	U1
Y frame	0	1	2	3	4	5	6	7
UV frame	0				4			

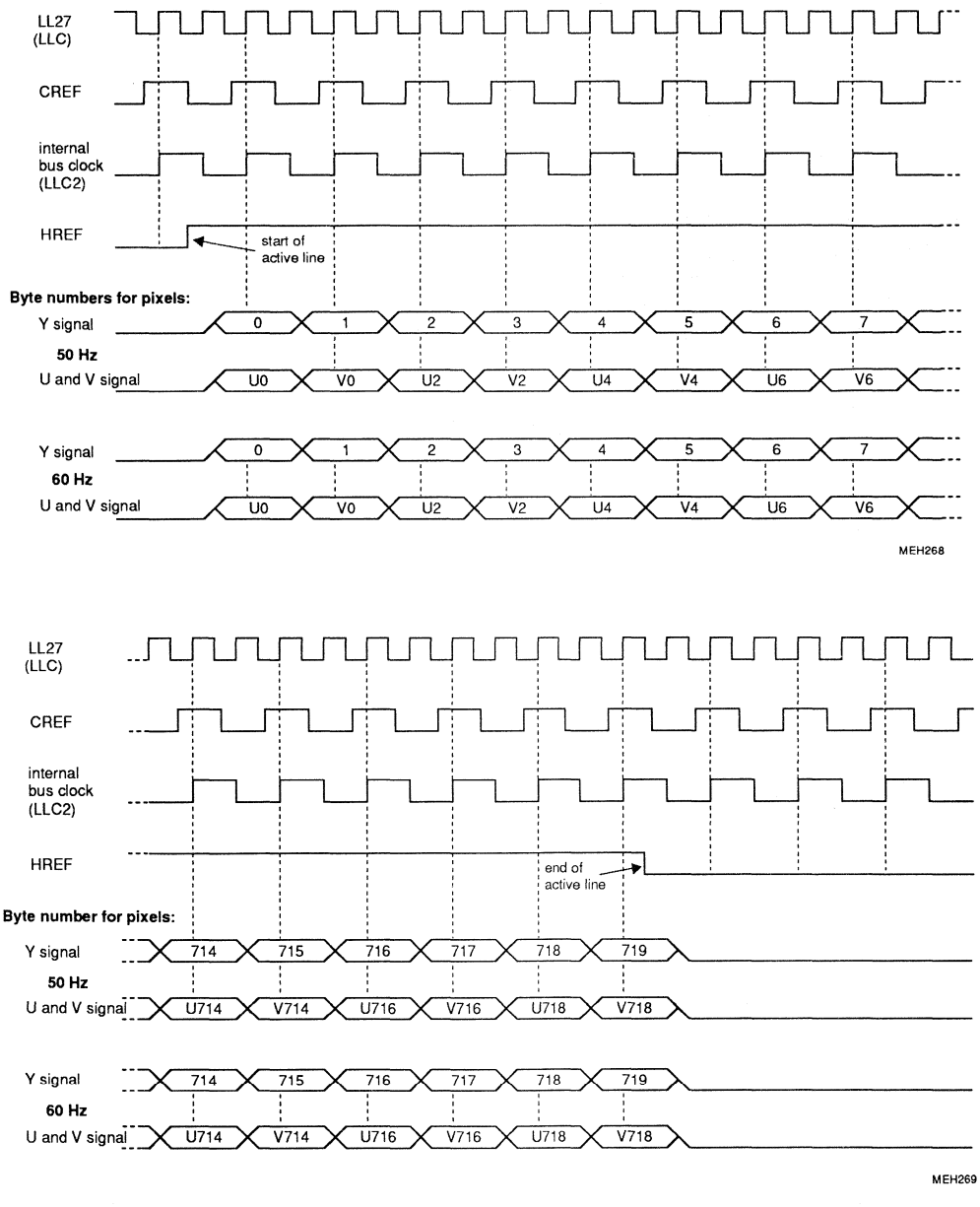


Fig.3 Line control by HREF for 4 : 2 : 2 format, CREF = 13.5 MHz; HREF = 720 pixel; 50 Hz and 60 Hz field.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD1}	supply voltage range (pin 12)	−0.3	7	V
V_{DDD2}	supply voltage range (pin 31)	−0.3	7	V
V_{DDA1}	supply voltage range (pin 32)	−0.3	7	V
V_{DDA2}	supply voltage range (pin 37)	−0.3	7	V
V_{DDA3}	supply voltage range (pin 40)	−0.3	7	V
V_{DDA4}	supply voltage range (pin 42)	−0.3	7	V
$V_{diff\ GND}$	difference voltage $V_{SSD1} - V_{SSA}$	-	±100	mV
V_n	voltage on all input pins 4 to 11, 14 to 27 and 41	−0.3	V_{DDD}	V
V_n	voltage on analog output pins 33, 36 and 39	−0.3	V_{DDD}	V
P_{tot}	total power dissipation	0	tbf	mW
T_{stg}	storage temperature range	−55	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	±2000	-	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction-to-ambient in free air	46 K/W

CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; V_{DDA} = 4.75 to 5.25 V; LLC = LL27; MC = CREF = 13.5 MHz; T_{amb} = 0 to 70 °C; measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD1}	supply voltage range (pin 12)	for digital part	4.5	5	5.5	V
V_{DDD2}	supply voltage range (pin 31)	for digital part	4.5	5	5.5	V
V_{DDA1}	supply voltage range (pin 32)	for buffer of DAC 1	4.75	5	5.25	V
V_{DDA2}	supply voltage range (pin 37)	for buffer of DAC 2	4.75	5	5.25	V
V_{DDA3}	supply voltage range (pin 40)	for buffer of DAC 3	4.75	5	5.25	V
V_{DDA4}	supply voltage range (pin 42)	DAC reference voltage	4.75	5	5.25	V
I_{DDD}	supply current (I_{DDD1} + I_{DDD2})	for digital part	-	tbf	tbf	mA
I_{DDA}	supply current (I_{DDA1} to I_{DDA4})	for DACs and buffers	-	tbf	tbf	mA
YUV-bus inputs (pins 4 to 11 and 14 to 21)		Figures 3 and 4				
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance	V_I = HIGH	-	-	10	pF
I_{LI}	input leakage current		-	-	4.5	µA
Inputs MS1, MS2, MC, LLC, HREF and RESN (pins 22 to 27)						
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance	V_I = HIGH	-	-	10	pF
I_{LI}	input leakage current		-	-	4.5	µA
V_{24}	MC input voltage for LL27	27 MHz data rate	2.0	-	V_{DDD}+0.5	V
	CREF signal on MC input	CREF data rate; note 1	-	-	-	V
I²C-bus SCL and SDA (pins 28 and 29)						
V_{IL}	input voltage LOW		−0.5	-	1.5	V
V_{IH}	input voltage HIGH		3.0	-	V_{DDD}+0.5	V
I_I	input current	V_I = LOW or HIGH	-	-	±10	µA
V_{ACK}	output voltage at acknowledge (pin 29)	I_{29} = 3 mA	-	-	0.4	V
I_{29}	output current	during acknowledge	3	-	-	mA
Digital-to-analog converters (pins 1, 2, 41, 42, 43 and 44)						
V_{DAC}	input reference voltage for internal resistor chains (pin 42)		4.75	5	5.25	V
I_{CUR}	input current (pin 41)	R_{41-42} = 15 kΩ	-	300	-	µA
$V_{1,44}$	reference voltage LOW	pin connected to V_{SSA1}	-	0	-	V
C_L	external blocking capacitor to V_{SSA1} for reference voltage HIGH (pins 2 and 43)		-	0.1	-	µF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{LLC}	minimum data conversation rate (clock)	Fig.3	-	-	32	MHz
Res	resolution	luminance DAC	-	9	-	bit
		chrominance DACs	-	8	-	bit
ILE	DC integral linearity error	8-bit data	-	-	1.0	LSB
DLE	DC differential error	8-bit data	-	-	0.5	LSB
Y, ±(R–Y) and ±(B–Y) analog outputs (pins 39, 33 and 36)						
V_o	output signal voltage (peak-to-peak value)	without load	-	2	-	V
$V_{33,36,39}$	output voltage range	without load; note 2	0.2	-	2.2	V
V_{39}	output blanking level	Y output; note 3	-	16	-	LSB
$V_{33,36}$	output no-colour level	±(R–Y), ±(B–Y); note 4	-	128	-	LSB
$R_{33,36,39}$	internal serial output resistance		-	25	-	Ω
$R_{L\ 33,36,39}$	output load resistance	external load	125	-	-	Ω
B	output signal bandwidth	-3 dB	20	-	-	MHz
t_d	signal delay from input to Y output		-	tbf	-	ns
LLC timing (pins 25)		LLC; Fig.3				
t_{LLC}	cycle time		33	37	41	ns
$t_{p\,H}$	pulse width		40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
YUV-bus timing (pins 4 to 11 and 14 to 21)		Fig.5				
t_{SU}	input data set-up time		11	-	-	ns
t_{HD}	input data hold time		3	-	-	ns
MC timing (pin24)		Fig.5				
t_{SU}	input data set-up time		11	-	-	ns
t_{HD}	input data hold time		3	-	-	ns
RESN timing (pin 27)						
t_{SU}	set-up time after power-on or failure	active LOW; note 5	4 x t_{LLC}	-	-	ns

Notes to the characteristics

1. YUV-bus data is read at MC = HIGH (pin 24) clocked with LLC (Fig.5) . Data is read only with every second rising edge of LLC when CREF = LLC/2 on MC-pin 24.
2. 0.2 to 2.2 V ouput voltage range at 8-bit DAC input data. The data word can increase to 9-bit dependent on peaking factor.
3. The luminance signal is set to the digital black level: 16 LSB for BLV-bit = 0; 0 LSB for BLV-bit = 1.
4. The chrominance amplitudes are set to the digital colourless level of 128 LSB.
5. The circuit is prepared for a new data initialization.

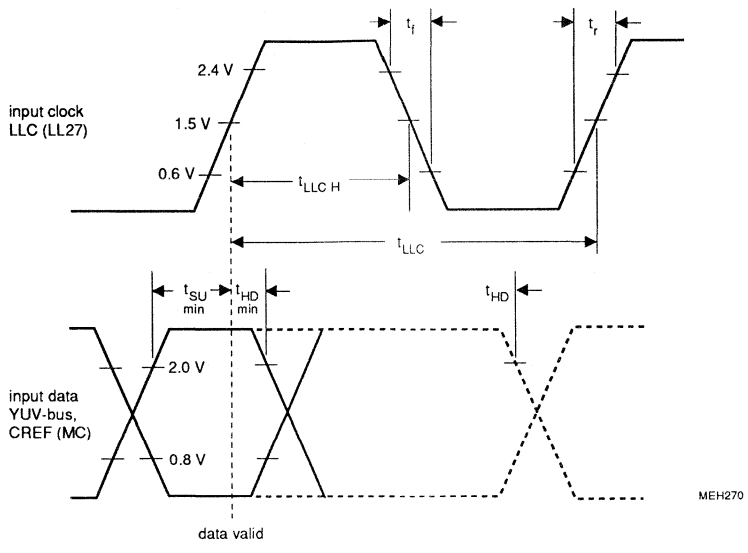


Fig.4 YUV-bus data and CREF timing.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A		DATAn	A	P

S = start condition
SLAVE ADDRESS = **1011 111X**
A = acknowledge, generated by the slave
SUBADDRESS* = subadress byte (Table 4)
DATA = data byte (Table 4)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 4 I²C-bus transmission

FUNCTION	SUBADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Peaking and coring	01	AFB	CO1	CO0	BP1	BP0	BFB	WG1	WG0
Input formats; interpolation	02	IFF	IFC	IFL	CMO	LI1	LI0	GA1	GA0
Input/output setting	03	0	0	DC1	DC0	DRP	BLV	R78	INV

Bit functions in data bytes:

"01" CO1 and CO0 — Control of coring threshold:

CO1	CO0	
0	0	coring off
0	1	small noise reduction
1	0	medium noise reduction
1	1	high noise reduction

AFB, BP1, BP0, BFB — Bandpass filter selection:

AFB	BP1	BP0	BFB	
X	0	0	0	characteristic Fig.5
X	0	1	0	characteristic Fig.6
X	1	0	0	characteristic Fig.7
X	1	1	0	characteristic Fig.8
0	X	X	1	BF1 filter bypassed Fig.9(a)
1	X	X	1	BF1 filter bypassed Fig.9(b)

BFB, WG1 and WG0 — Peaking factor K:

BFB	WG1	WG0	
0	0	0	K = 1/8; minimum peaking
0	0	1	K = 1/4
0	1	0	K = 1/2
0	1	1	K = 1; maximum peaking
1	0	0	K = 0; peaking off
1	0	1	K = 1/4; minimum peaking
1	1	0	K = 1/2
1	1	1	K = 1; maximum peaking

"02" IFF, IFC, IFL — Input format and filter control at 13.5 MHz data rate:

IFF	IFC	IFL	
0	0	0	4 : 1 : 1 format; –3 dB attenuation at 1.6 MHz video frequency; Fig.10
0	0	1	4 : 1 : 1 format; –3 dB attenuation at 600 kHz video frequency; Fig.11
0	1	X	4 : 1 : 1 format; –3 dB attenuation at 1.2 MHz video frequency; Fig.12
1	0	0	4 : 2 : 2 format; –3 dB attenuation at 1.6 MHz video frequency; Fig.10
1	0	1	4 : 2 : 2 format; –3 dB attenuation at 600 kHz video frequency; Fig.11
1	1	X	4 : 2 : 2 format; –3 dB attenuation at 2.5 MHz video frequency; Fig.13

CMO — Choice modulation: 0 = modulation off; 1 = modulation on

LI1 and LI0 — DCTI timing range:

LI1	LI0	range
0	0	+4 / –4
0	1	+6 / –6
1	0	+8 / –8
1	1	+12 / –12

GA1 and GA0 — DCTI gain factor:

GA1	GA0	factor
0	0	off
0	1	1/4
1	0	1/2
1	1	1

"03" DC1 and DC0 — Delay compensation of luminance signal:

DC1	DC0	delayed clock cycles
0	0	0
0	1	+1
1	0	–2
1	1	–1

DRP	UV input data code:	0 = two's complement; 1 = offset binary
BLV	Blanking level on Y output:	0 = 16 LSB; 1 = 0 LSB
R78	YUV input data solution:	0 = 7-bit data; 1 = 8-bit data
INV	Polarity of colour-difference output signals:	0 = normal polarity equal to input signal 1 = inverted polarity

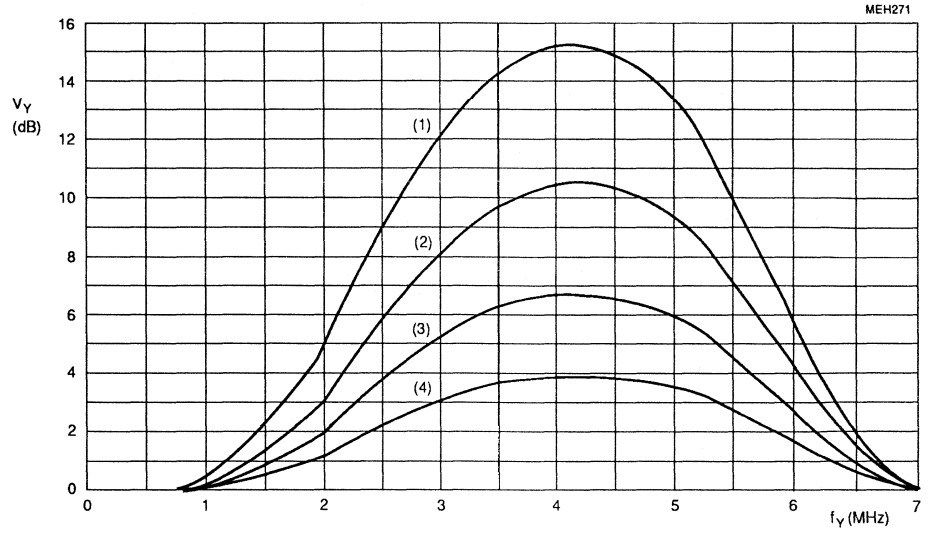


Fig.5 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 0 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

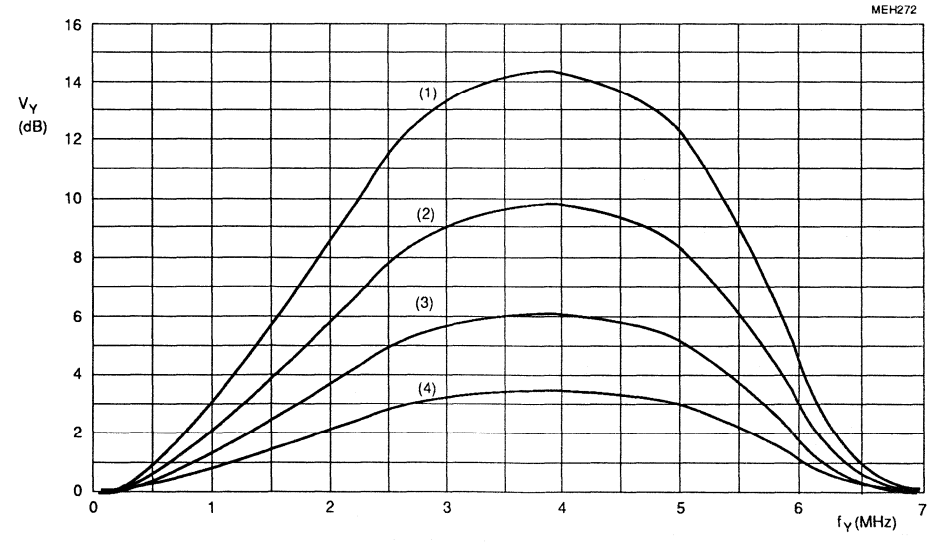


Fig.6 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 1 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

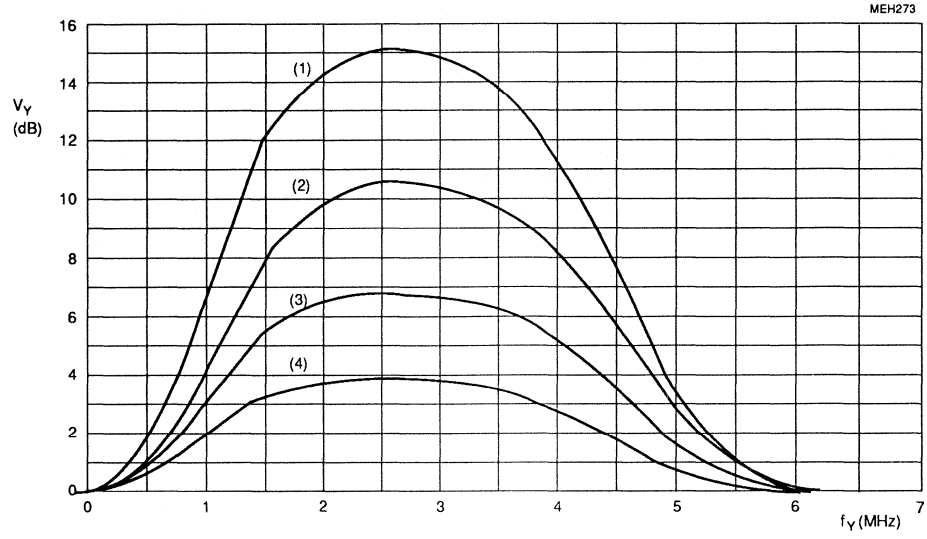


Fig.7 Peaking frequency response with I²C-bus control bits BP1 = 1; BP0 = 0 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

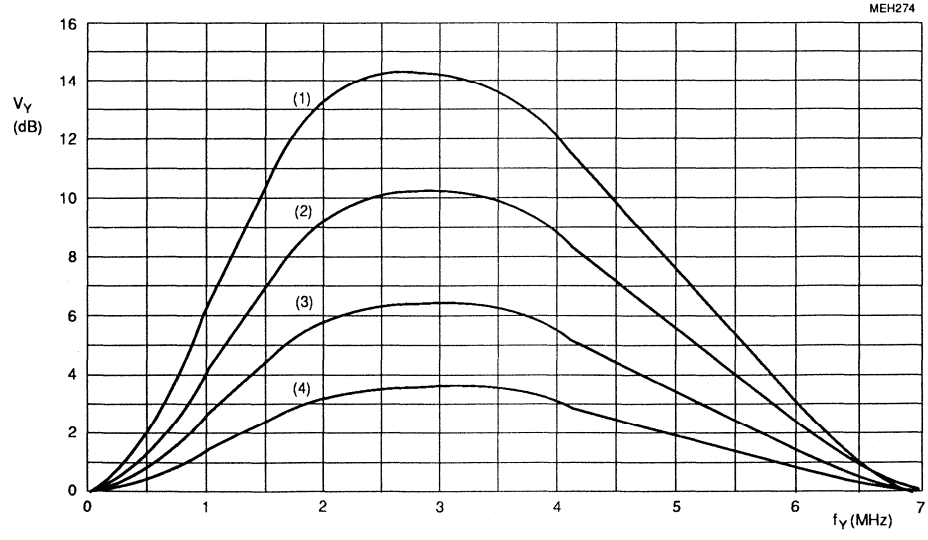


Fig.8 Peaking frequency response with I²C-bus control bits BP1 = 1; BP0 = 1 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

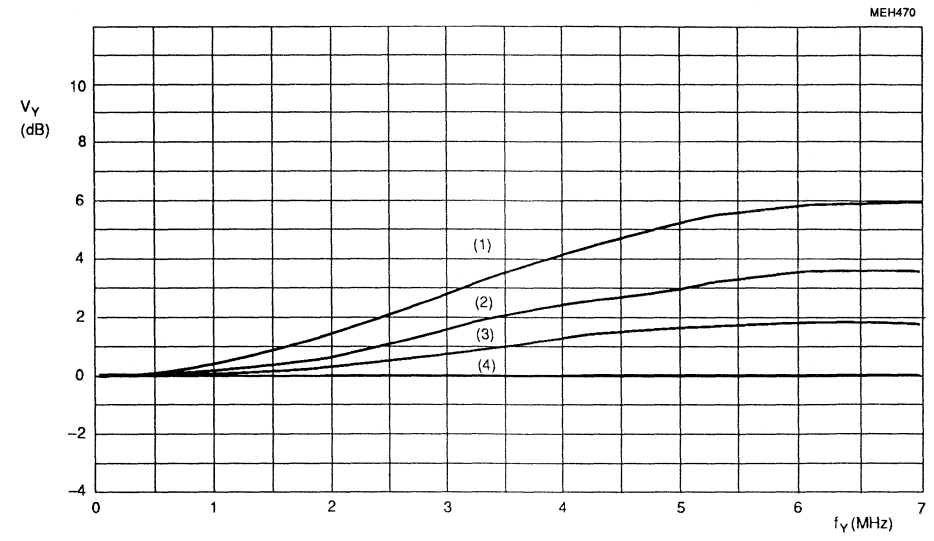


Fig.9(a) Peaking frequency response with I²C-bus control bits AFB = 0, BP1 = 0, BP0 = 0 and BFB = 1; bandpass filter BF1 bypassed and peaking off; (1) K = 1, (2) K = 1/2, (3) K = 1/4 and (4) K = 0

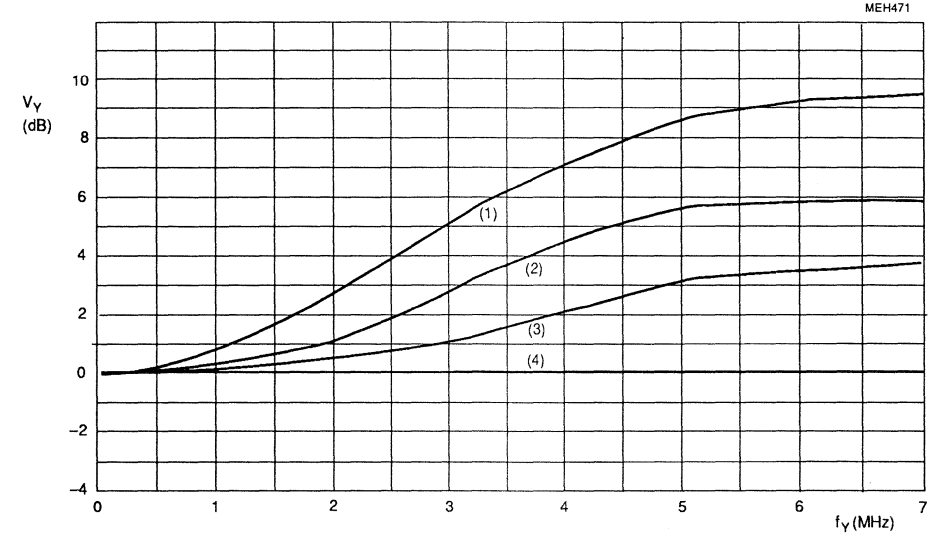


Fig.9(b) Peaking frequency response with I²C-bus control bits AFB = 1, BP1 = 0, BP0 = 0 and BFB = 1; bandpass filter BF1 bypassed and peaking off; (1) K = 1, (2) K = 1/2, (3) K = 1/4 and (4) K = 0.

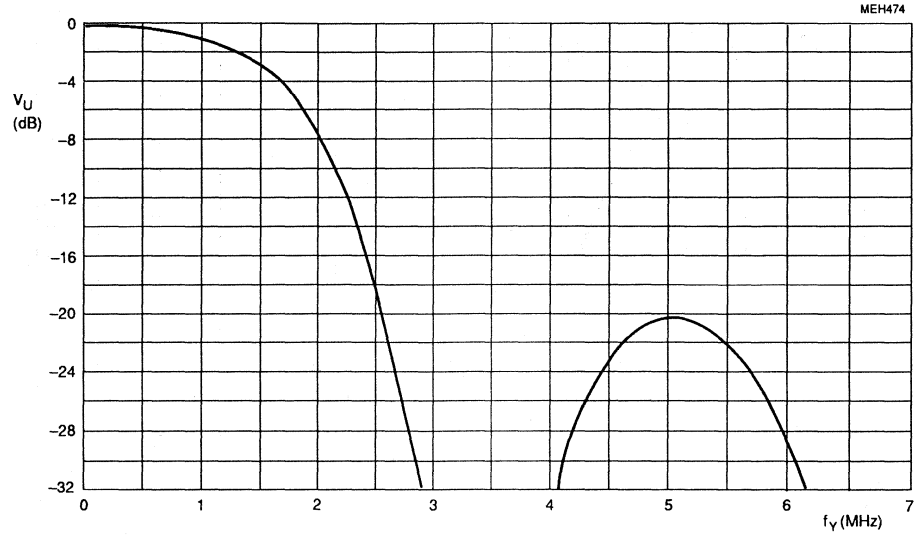


Fig.10 Interpolation filter at DCTI off with I²C-bus control bits IFF = 0; IFC = 0 and IFL = 0 in 4:1:1 format and control bits IFF = 1; IFC = 0 and IFL = 0 in 4:2:2 format; 13.5 MHz data rate.

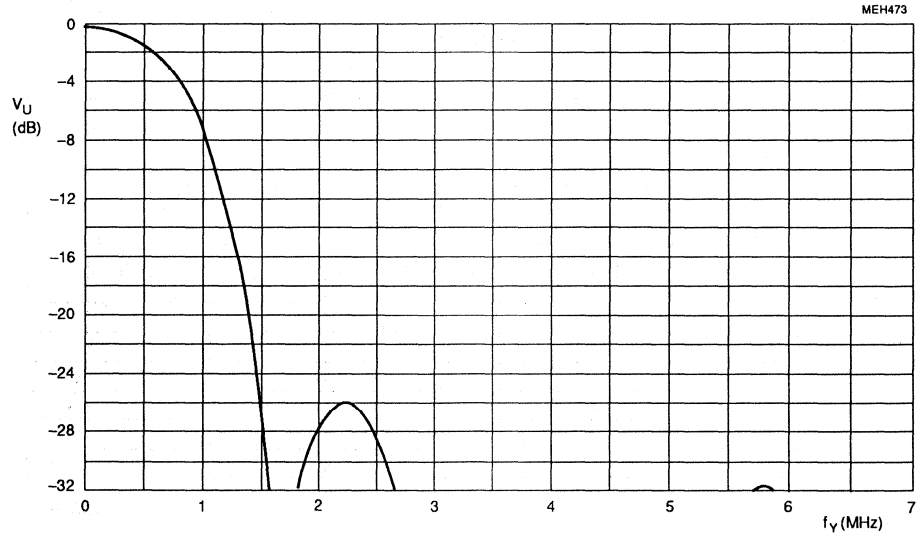


Fig.11 Interpolation filter at DCTI off with I²C-bus control bits IFF = 0; IFC = 0 and IFL = 1 in 4:1:1 format and control bits IFF = 1; IFC = 0 and IFL = 1 in 4:2:2 format; 13.5 MHz data rate.

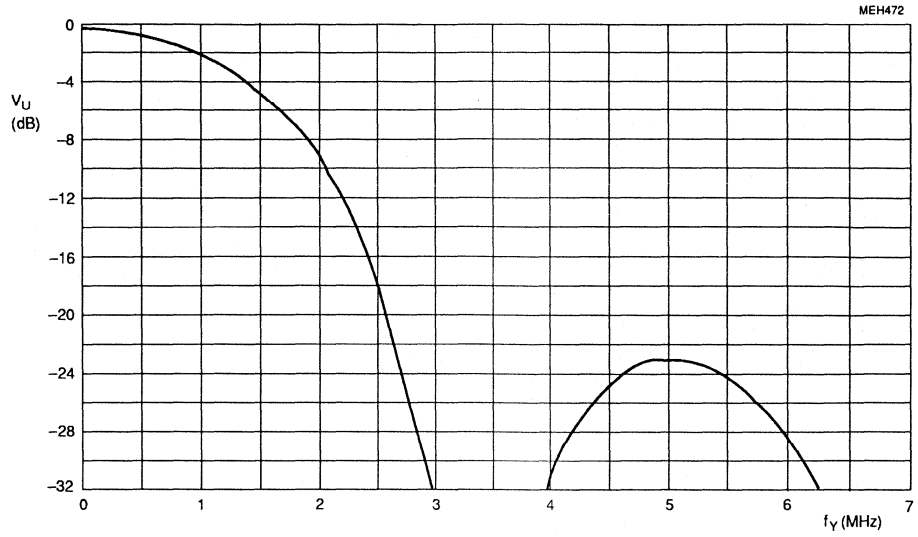


Fig.12 Interpolation filter at DCTI off with I²C-bus control bits IFF = 0; IFC = 1 and IFL = 0 in 4:1:1 format; 13.5 MHz data rate.

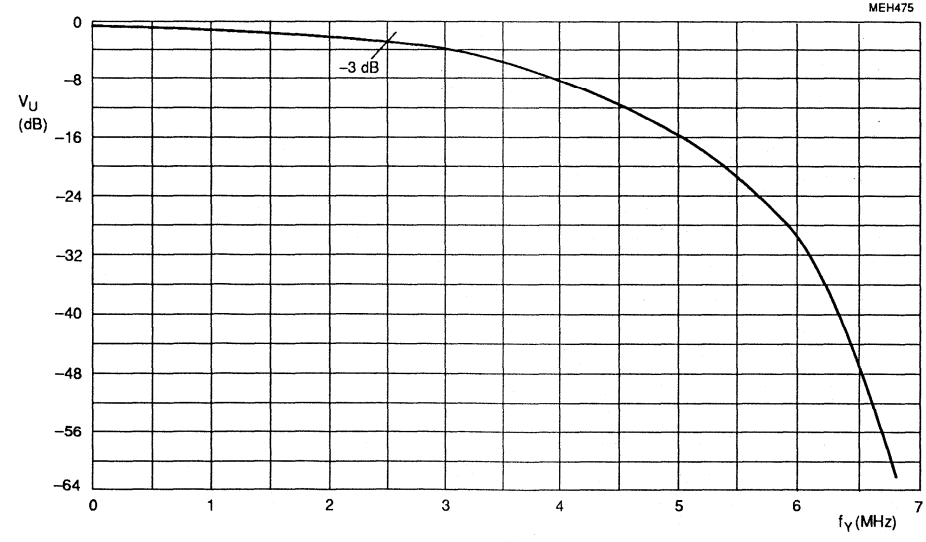


Fig.13 Interpolation filter with I²C-bus control bits IFF = 1; IFC = 1 and IFL = X in 4:2:2 format; 13.5 MHz data rate.

Data sheet	
status	Preliminary specification
date of issue	April 1992

SAA7169

35 MHz triple 9-bit D/A converter for high-speed video

FEATURES

- CMOS circuit to convert high-speed video data from digital to analog
- Three equal 9-bit digital-to-analog converters
- Input signals TTL-compatible
- Input registers for positive edge-triggered data signals
- Clock frequency for a conversion rate up to 35 MHz
- 20 MHz analog bandwidth
- 2 V (p-p) analog output voltage range without load on output (0.2 to 2.2 V DC)
- 1 V / 75 Ω outputs (0.1 to 1.1 V DC); Fig.1
- No de-glitching circuit required
- Typical 225 mW power dissipation

GENERAL DESCRIPTION

The triple high-speed D/A converter can be used in applications for

- desktop video processing
- digital television
- graphic displays
- television decoders
- general high frequency conversion

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	supply voltage digital part	4.5	5	5.5	V
V_{DDA}	supply voltage analog part	4.75	5	5.25	V
$I_{DD\ tot}$	total supply current	-	-	38	mA
V_I	data input levels	TTL-compatible			
f_{CLK}	conversion frequency	1	-	35	MHz
V_o	nominal output amplitude on pins 1, 3, 43 (peak-to-peak value)	-	2	-	V
B	bandwidth (–3 dB)	20	-	-	MHz
DNL	differential non-linearity	-	-	±0.5	LSB
INL	integral non-linearity	-	-	±0.2	%
α_{CR}	crosstalk attenuation	48	-	-	dB
R_o	internal serial output resistance	-	25	-	Ω
R_L	output load resistance	125	-	-	Ω
T_{amb}	operating ambient temperature range	0	-	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7169	44	PLCC	plastic	SOT187

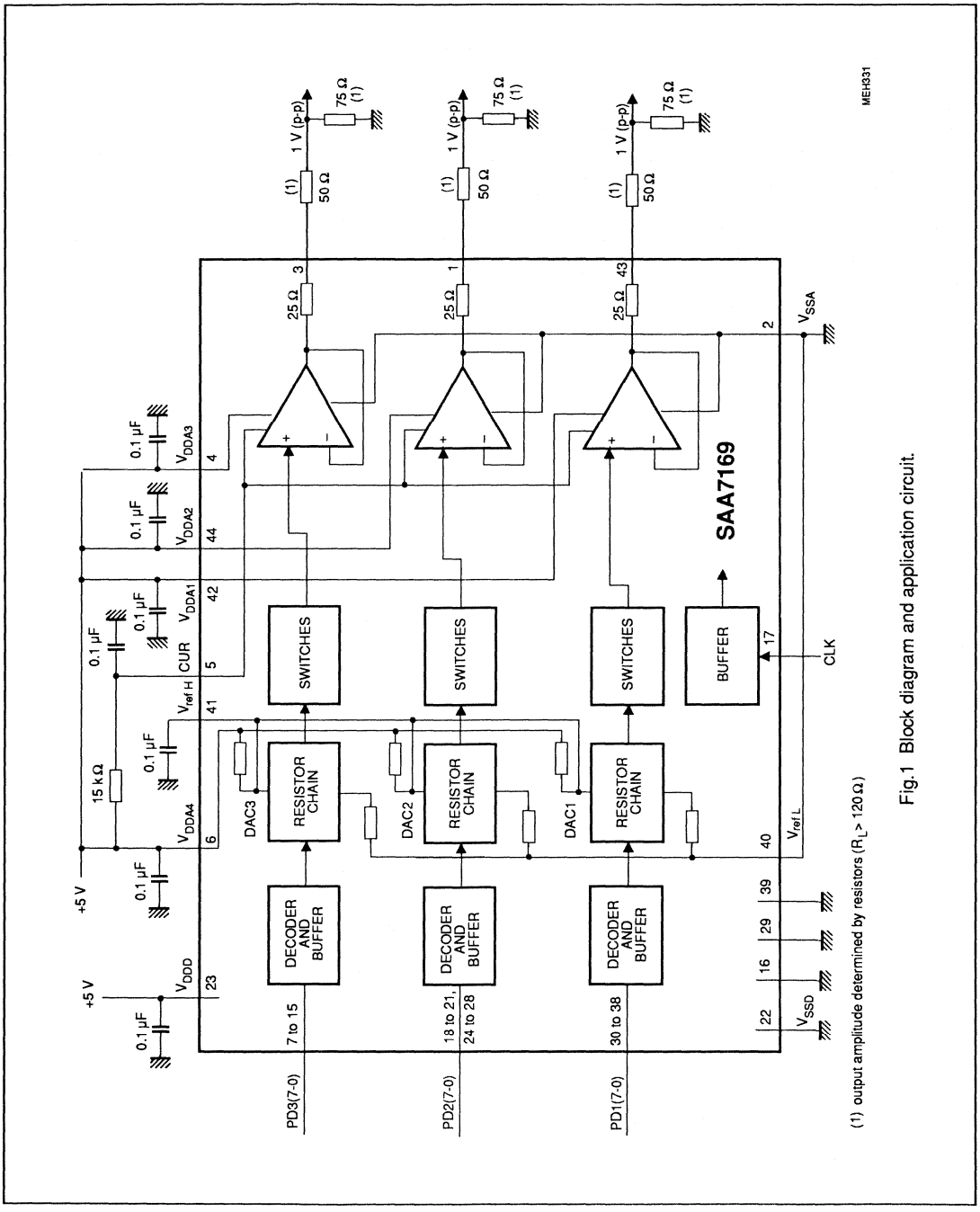


Fig.1 Block diagram and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{o\,2}$	1	analog output voltage of channel 2
V_{SSA}	2	analog ground (0 V)
$V_{o\,3}$	3	analog output voltage of channel 3
V_{DDA3}	4	+5 V supply voltage for buffer amplifier of channel 3
CUR	5	current input for analog output buffers, decoupled to V_{SSA}
V_{DDA4}	6	+5 V supply voltage for analog reference part
PD3(8)	7	9-bit data input of channel 3
PD3(7)	8	
PD3(6)	9	
PD3(5)	10	
PD3(4)	11	
PD3(3)	12	
PD3(2)	13	
PD3(1)	14	
PD3(0)	15	
i.c.	16	connect to digital ground (input not used)
CLK	17	clock frequency input
PD2(8)	18	9-bit data input of channel 2 (bits PD2(8-5))
PD2(7)	19	
PD2(6)	20	
PD2(5)	21	
V_{SSD}	22	digital ground (0 V)
V_{DDD}	23	+5 V supply voltage for digital part
PD2(4)	24	9-bit data input of channel 2 (bits PD2(4-0))
PD2(3)	25	
PD2(2)	26	
PD2(1)	27	
PD2(0)	28	
i.c.	29	connect to digital ground (input not used)
PD1(8)	30	9-bit data input of channel 1 (bits PD1(8-4))
PD1(7)	31	
PD1(6)	32	
PD1(5)	33	
PD1(4)	34	

SYMBOL	PIN	DESCRIPTION
PD1(3)	35	9-bit data input of channel 1 (bits PD1(3-0))
PD1(2)	36	
PD1(1)	37	
PD1(0)	38	
i.c.	39	connect to digital ground (input not used)
$V_{ref\,L}$	40	reference voltage LOW; analog ground (V_{SSA})
$V_{ref\,H}$	41	internal generated reference voltage HIGH, decoupled to V_{SSA}
V_{DDA1}	42	+5 V supply voltage for buffer amplifier of channel 1
$V_{o\,1}$	43	analog output voltage of channel 1
V_{DDA2}	44	+5 V supply voltage for buffer amplifier of channel 2

PIN CONFIGURATION

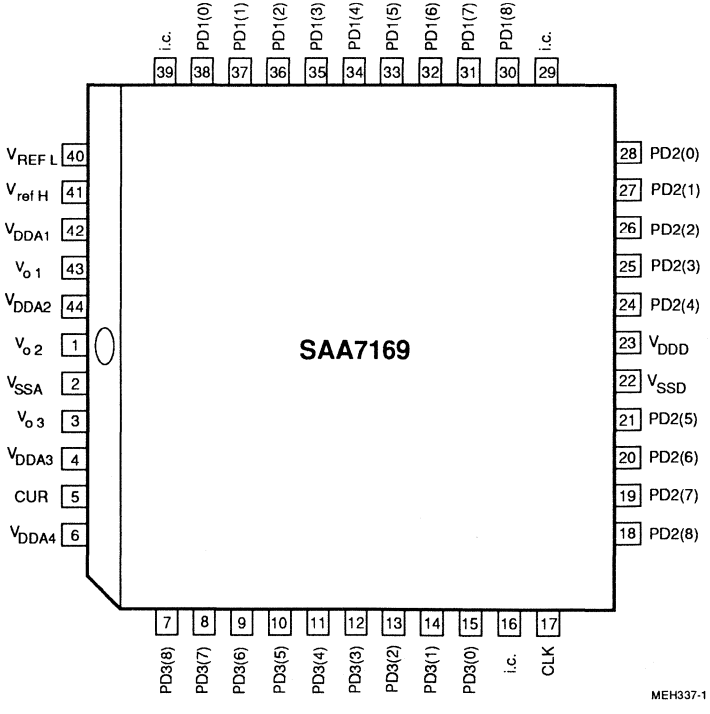


Fig.2 Pin configuration.

35 MHz triple 9-bit D/A converter for high-speed video

SAA7169

FUNCTIONAL DESCRIPTION

The integrated monolithic CMOS circuit SAA7169 is a triple 9-bit digital-to-analog converter for high-speed video applications. Its three channels are equal. The maximum conversion rate is 35 MHz.

The converters use a combination of resistor chains with low-impedance output buffers. The bottom output voltage is 200 mV to reduce integral non-linearity errors. The analog signal, without load on output pin, is between 0.2 and 2.2 V. Fig.1 shows the application for 1 V/ 75 Ω outputs, using the serial 25 Ω + 50 Ω resistors.

Each digital-to-analog converter has its own supply pin for purpose of decoupling. V_{DDA4} is the supply voltage for the resistor chains of the three DACs. The accuracy of this supply voltage influences directly the output amplitudes.
The current CUR into pin 5 is 0.3 mA (V_{DDA4} = 5 V, R_{5-6} = 15 kΩ); a larger current improves the bandwidth but increases the integral non-linearity.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage range (pin 23)	−0.3	7	V
V_{DDA1}	analog supply voltage range (pin 42)	−0.3	7	V
V_{DDA2}	analog supply voltage range (pin 44)	−0.3	7	V
V_{DDA3}	analog supply voltage range (pin 4)	−0.3	7	V
V_{DDA4}	analog supply voltage range (pin 6)	−0.3	7	V
$V_{diff\ GND}$	difference voltage $V_{SSD} - V_{SSA(1\ to\ 4)}$	-	±100	mV
V_n	voltage on all input pins 7 to 15, 18 to 21 and 24 to 40	−0.3	V_{DDD}	V
P_{tot}	total power dissipation	0	tbf	mW
T_{amb}	operating ambient temperature range	0	70	°C
T_{stg}	storage temperature range	−65	150	°C
V_{ESD}	electrostatic handling* for all pins	±2000	-	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; V_{DDA} = 4.75 to 5.25 V; CLK = 35 MHz; f_{DATA} = 17.5 MHz (squarewave, full scale); T_{amb} = 0 to 70 °C; measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	supply voltage range (pin 23)	for digital part	4.5	5	5.5	V
V_{DDA1}	supply voltage range (pin 42)	for buffer of DAC 1	4.75	5	5.25	V
V_{DDA2}	supply voltage range (pin 44)	for buffer of DAC 2	4.75	5	5.25	V
V_{DDA3}	supply voltage range (pin 4)	for buffer of DAC 3	4.75	5	5.25	V
V_{DDA4}	supply voltage range (pin 6)	DAC reference voltage	4.75	5	5.25	V
I_{DDD}	supply current	for digital part; note 1	-	-	20	mA
I_{DDA}	supply current (I_{DDA1} to I_{DDA4})	without load on outputs	-	-	18	mA
9-bit data inputs (pins 7 to 15; 18 to 21, 24 to 28 and 30 to 38)						
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance		-	-	10	pF
I_{leak}	input leakage current		-	-	10	µA
t_{SU}	data set-up time	Fig.3	11	-	-	ns
t_{HD}	data hold time		3	-	-	ns
CLK input (pin 17)		Fig.3				
f_{CLK}	frequency range		1	-	35	MHz
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance		-	-	10	pF
I_{leak}	input leakage current		-	-	10	µA
t_{CLK}	cycle time		28.5	-	-	ns
t_{pH}	duty factor	t_{CLKH} / t_{CLK}	40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
Digital-to-analog converters (pins 5, 6 and 40)						
V_{DDA4}	reference input voltage for internal resistor chains (pin 6)		4.75	5	5.25	V
I_{CUR}	input current (pin 5)	R_{6-5} = 15 kΩ	-	-	400	µA
Analog outputs V_{o1}; V_{o2} and V_{o3} (pins 43, 1 and 3)						
V_o	nominal output signal (peak-to-peak value)	without load	-	2	-	V
$V_{43, 1, 3}$	minimum output voltage	without load; V_{DDA4} = 5 V	0.16	-	0.24	V
	maximum output voltage	without load; V_{DDA4} = 5 V	2.1	-	2.3	V
DTDM	DAC to DAC matching	between all channels	-	-	|30|	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
B	output signal bandwidth	-3 dB	20	-	-	MHz
α_{CR}	crosstalk attenuation	note 2	48	-	-	dB
DNL	differential non-linearity	9-bit data; R_L = 125 Ω	-	-	±0.5	LSB
INL	integral non-linearity	9-bit data; R_L = 125 Ω	-	-	±0.2	%
$R_{43, 1, 3}$	internal serial output resistor		-	25	-	Ω
$R_{L\ 43, 1, 3}$	load resistance on output		125	-	-	Ω

Notes to the characteristics

1. With f_{CLK} = 35 MHz; f_{DATA} = 17.5 MHz (squarewave, full scale)
2. Crosstalk from channel to channel. One DAC with digital 5 MHz (sinusoidal, full scale) input signal, the other input data LOW. Measurements taken on outputs with 5.46 MHz filters (–3 dB at 5.87 MHz and –45 dB at 7.24 MHz).

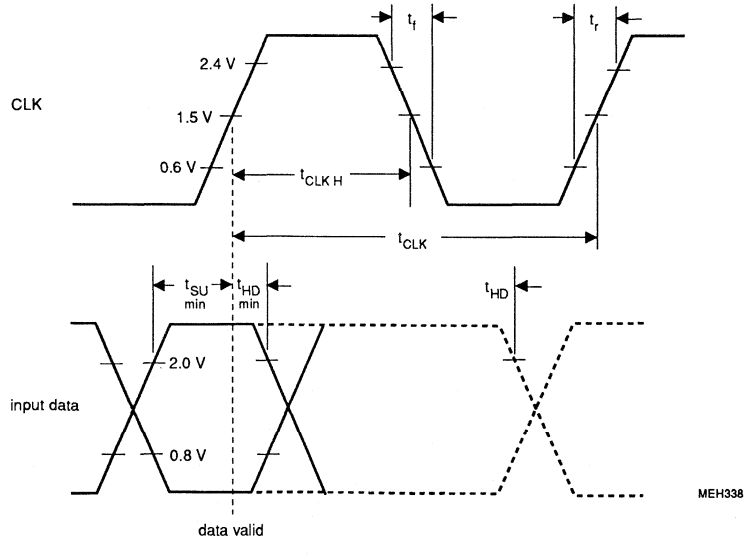


Fig.3 Input data timing.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	May 1992

SAA7186
Digital video scaler

FEATURES

- Scaling of video picture windows down to randomly sized windows
- Processes maximum 768 pixels per line and 576 lines per field
- Two-dimensional data processing for improved signal quality of scaled video data and for compression of video data
- 16-bit YUV input data formatter
- Interlace/non-interlace video data processing and field control
- Line memories in Y path and UV path to store two lines, each with 2 x 768 x 8 bit capacity
- Vertical sync processing by scale control
- Non-scaled mode to get full picture or to gate videotext lines
- Input and output data selection binary/two's complement (UV)
- Switchable RGB matrix and anti-gamma ROMs
- 16-word FIFO register for 32-bit output data
- Output formats: 5-bitand 8-bit RGB, 8-bit YUV or 8-bit monochrome

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5	5.5	V
$I_{DD\ tot}$	total supply current (inputs LOW, without output load)	-	-	180	mA
V_I	data input level	TTL-compatible			
V_O	data output level	TTL-compatible			
LLC	input clock frequency	-	-	32	MHz
T_{amb}	operating ambient temperature range	0	-	70	°C

GENERAL DESCRIPTION

The CMOS circuit SAA7186 scales and filters digital video data to randomly sized picture windows. YUV input data in 4:2:2 format are required (SAA7191B source).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7186	100	QFP	plastic	SOT317B4

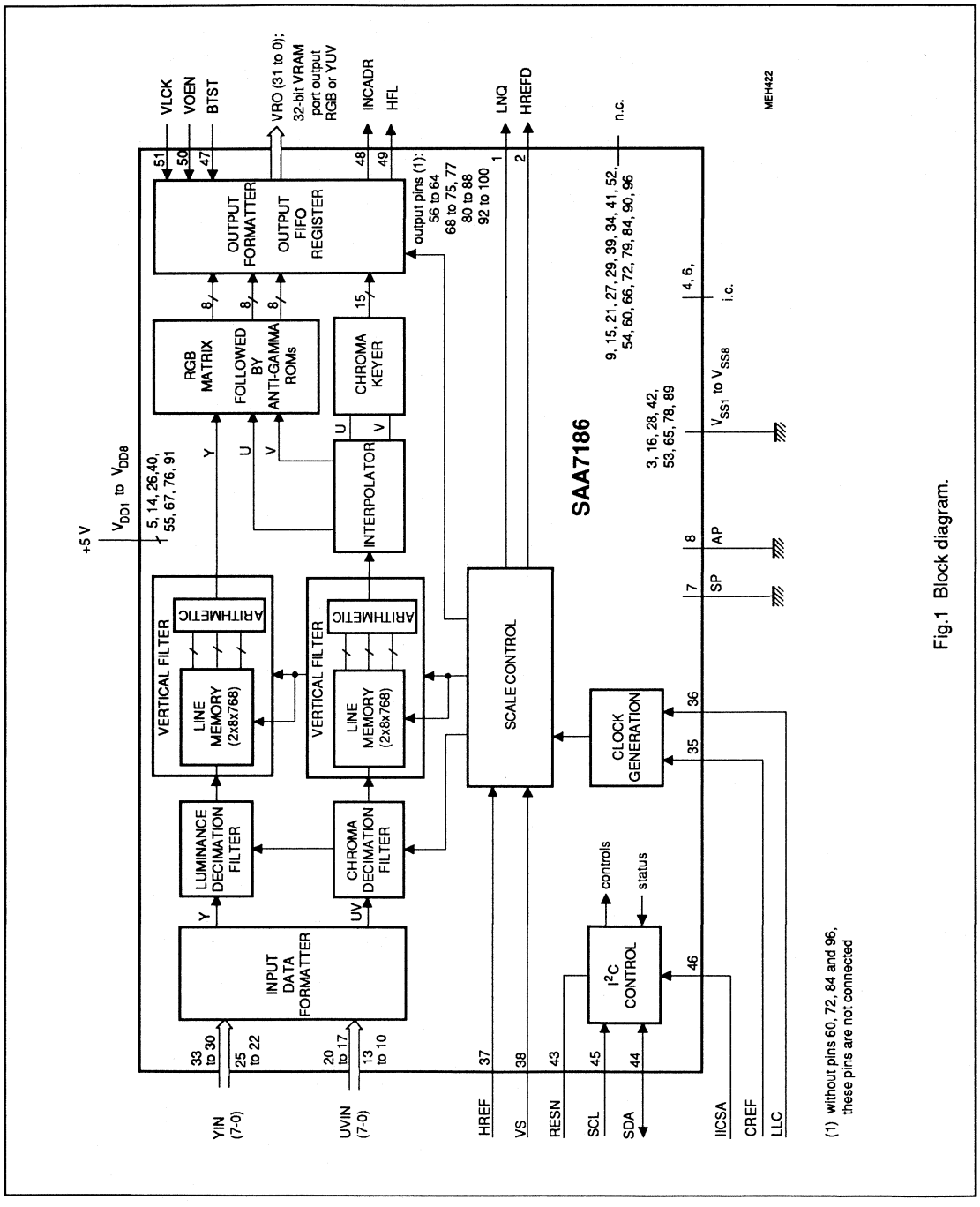


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	STATUS	DESCRIPTION
LNQ	1	O	line qualifier signal; active polarity defined by QPL-bit ("10")
HREFD	2	O	delay-compensated HREF output signal
V_{SS1}	3	-	GND1 (0 V)
i.c.	4	-	internally connected
V_{DD1}	5	-	+5 V supply voltage 1
i.c.	6	-	internally connected
SP	7	I	connected to ground (shift pin for testing)
AP	8	I	connected to ground (action pin for testing)
n.c.	9	-	not connected
UVIN0	10	I	time-multiplexed colour-difference input data (bits 0 to 3)
UVIN1	11	I	
UVIN2	12	I	
UVIN3	13	I	
V_{DD2}	14	-	+5 V supply voltage 2
n.c.	15	-	not connected
V_{SS2}	16	-	GND2 (0 V)
UVIN4	17	I	time- multiplexed colour-difference input data (bits 4 to 7)
UVIN5	18	I	
UVIN6	19	I	
UVIN7	20	I	
n.c.	21	-	not connected
YIN0	22	I	luminance input data (bits 0 to 3)
YIN1	23	I	
YIN2	24	I	
YIN3	25	I	
V_{DD3}	26	-	+5 V supply voltage 3
n.c.	27	-	not connected
V_{SS3}	28	-	GND3 (0 V)
n.c.	29	-	not connected
YIN4	30	I	luminance input data (bits 4 to 7)
YIN5	31	I	
YIN6	32	I	
YIN7	33	I	
n.c.	34	-	not connected

SYMBOL	PIN	STATUS	DESCRIPTION
CREF	35	I	clock reference, external sync signal
LLC	36	I	line-locked system clock input signal (twice of pixel rate)
HREF	37	I	horizontal reference, pixel data clock signal (also present during vertical blanking)
VS	38	I	vertical sync input signal (approximately 6 lines long)
n.c.	39	-	not connected
V_{DD4}	40	-	+5 V supply voltage 4
n.c.	41	-	not connected
V_{SS4}	42	-	GND4 (0 V)
RESN	43	I	reset input (active-LOW for at least 30LLC periods)
SDA	44	I/O	IIC-bus data line
SCL	45	I	IIC-bus clock line
IICSA	46	I	set module address input of IIC-bus (LOW = B8, HIGH = BC)
BTST	47	I	output disable input; HIGH sets all data outputs to high-impedance state
INCADR	48	O	line increment / vertical reset control output line
HFL	49	O	FIFO register half-full flag output
VOEN	50	I	VRAM port output enable input (active-LOW)
VCLK	51	I	FIFO register clock input signal
n.c.	52	-	not connected
V_{SS5}	53	-	GND5 (0 V)
n.c.	54	-	not connected
V_{DD5}	55	-	+5 V supply voltage 5
VRO31	56	O	video output; 32-bit VRAM output port (bits 31 to 28)
VRO30	57	O	
VRO29	58	O	
VRO28	59	O	
n.c.	60	-	not connected
VRO27	61	O	video output; 32-bit VRAM output port (bits 27 to 24)
VRO26	62	O	
VRO25	63	O	
VRO24	64	O	
V_{SS6}	65	-	GND6 (0 V)
n.c.	66	-	not connected
V_{DD6}	67	-	+5 V supply voltage 6
VRO23	68	O	video output; 32-bit VRAM output port (bits 23 to 22)
VRO22	69	O	

SYMBOL	PIN	STATUS	DESCRIPTION
VRO21	70	O	video output; 32-bit VRAM output port (bits 21 to 20)
VRO20	71	O	
n.c.	72	-	not connected
VRO19	73	O	video output; 32-bit VRAM output port (bits 19 to 17)
VRO18	74	O	
VRO17	75	O	
V_{DD7}	76	-	+5 V supply voltage 7
VRO16	77	O	video output; 32-bit VRAM output port (bit16)
V_{SS7}	78	-	GND7 (0 V)
n.c.	79	-	not connected
VRO15	80	O	video output; 32-bit VRAM output port (bits 15 to 12)
VRO14	81	O	
VRO13	82	O	
VRO12	83	O	
n.c.	84	-	not connected
VRO11	85	O	video output; 32-bit VRAM output port (bits 11 to 8)
VRO10	86	O	
VRO9	87	O	
VRO8	88	O	
V_{SS8}	89	O	GND8 (0 V)
n.c.	90	-	not connected
V_{DD8}	91	-	+5 V supply voltage 8
VRO7	92	O	video output; 32-bit VRAM output port (bits 7 to 4)
VRO6	93	O	
VRO5	94	O	
VRO4	95	O	
n.c.	96	-	not connected
VRO3	97	O	video output; 32-bit VRAM output port (bits 3 to 0)
VRO2	98	O	
VRO1	99	O	
VRO0	100	O	

PIN CONFIGURATION

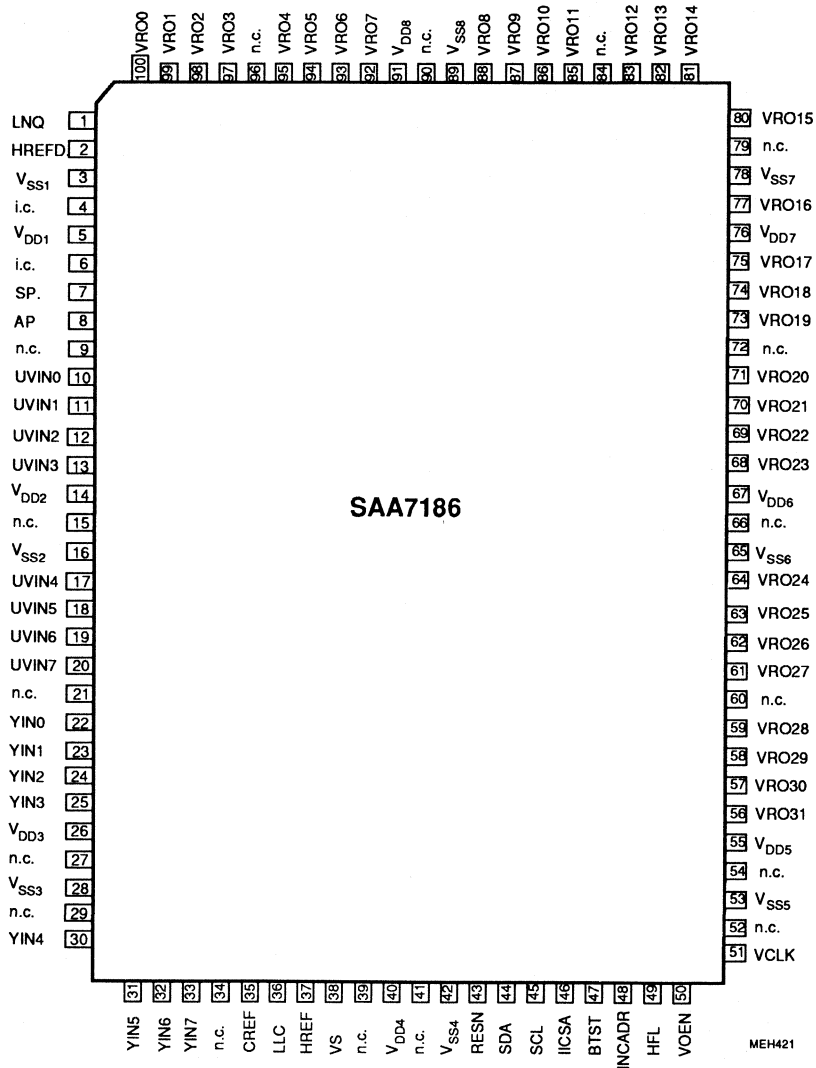


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The input port is output of Philips digital video multistandard decoders (SAA7151B, SAA7191B) or other similar sources.
The SAA7186 input supports the 16-bit YUV 4:2:2 format.
The video data from the input port are converted into a unique internal two's complement data stream and are processed in horizontal direction in two separate decimation filters.Then they are processed in vertical direction by the vertical processing unit (VPU).
Chrominance data are interpolated to a 4:4:4 format; a chroma keying bit is generated.
The 4:4:4 YUV data are then converted from the YUV to the RGB domain in a digital matrix. ROM tables in the RGB data path can be used for anti-gamma correction of gamma-corrected input signals. Uncorrected RGB and YUV signals can be bypassed.
A scale control unit generates reference and gate signals for scaling of the processed video data. After data formatting to the various VRAM port formats, the scaled video data are buffered in the 16 word x 32-bit output FIFO register. The FIFO output is directly connected to the VRAM output bus VRO(31-0). Specific reference signals support an easy memory interfacing.
All functions of the SAA7186 are controlled via I²C-bus using 17 subaddresses. The external microcontroller can get information by reading the status register.

Video input port

The 16-bit YUV input data in 4:2:2 format (Table 1) consist of 8-bit luminance data Y (pins YIN(7-0)) and 8-bit time-multiplexed colour-difference data UV (pins UVIN(7-0)).
The input data are clocked in by the signals LLC and CREF (Fig.3). HREF and VS inputs define the video scan pattern (window).

Sequential input data

- are limited to maximum 768 active pixels per line if the vertical filter is active
- UV can be processed in straight binary and two's complement representation (controlled by TCC)

Decimation filters

The decimation filters perform accurate horizontal filtering of the input data stream.
Signal characteristics are matched in front of the pixel decimation stage, thus disturbing artifacts, caused by the pixel dropping, are reduced.
The signal bandwidth can be reduced in steps of:

2-tap filter = −6 dB at 0.325 pixel rate
3-tap filter = −6 dB at 0.25 pixel rate
4-tap filter = −6 dB at 0.21 pixel rate
5-tap filter = −6 dB at 0.125 pixel rate
9-tap filter = −6 dB at 0.075 pixel rate

The different characteristics are choosen dependent on the defined scaling parameters in an adaptive filter mode (AFS-bit = 1).
The filter characteristics can also be selected independently by control bits HF2 to HF0 at AFS-bit = 0.

Vertical filters

Y and UV data are handled in separate filters (Fig.1). Each of the two line memories has a capacity of 2 x 768 x 8-bit. Thus two complete video lines of 4:2:2 YUV data can be stored. The VPU is split into two memory banks and one arithmetic unit. The available processing modes, respectively transfer functions, are selectable by the bits VP1 and VP0 if AFS = 0.
An adaptive mode is selected by AFS = 1. Disturbing artifacts, generated by line dropping, are reduced.

RGB matrix

Y data and UV data are converted after interpolation into RGB data according to CCIR601 recommendation. Data are bypassed in YUV or monochrome modes.

Table 1 4 : 2 : 2 format (pixels per line). The time frames are controlled by the HREF signal.

INPUT	PIXEL BYTE SEQUENCE				
YIN7	Ye7	Yo7	Ye7	Yo7	Ye7
YIN6	Ye6	Yo6	Ye6	Yo6	Ye6
YIN5	Ye5	Yo5	Ye5	Yo5	Ye5
YIN4	Ye4	Yo4	Ye4	Yo4	Ye4
YIN3	Ye3	Yo3	Ye3	Yo3	Ye3
YIN2	Ye2	Yo2	Ye2	Yo2	Ye2
YIN1	Ye1	Yo1	Ye1	Yo1	Ye1
YIN0	Ye0	Yo0	Ye0	Yo0	Ye0
UVIN7	Ue7	Ve7	Ue7	Ve7	Ue7
UVIN6	Ue6	Ve6	Ue6	Ve6	Ue6
UVIN5	Ue5	Ve5	Ue5	Ve5	Ue5
UVIN4	Ue4	Ve4	Ue4	Ve4	Ue4
UVIN3	Ue3	Ve3	Ue3	Ve3	Ue3
UVIN2	Ue2	Ve2	Ue2	Ve2	Ue2
UVIN1	Ue1	Ve1	Ue1	Ve1	Ue1
UVIN0	Ue0	Ve0	Ue0	Ve0	Ue0
Y frame	0	1	2	3	4
UV frame	0		2		4

e = even pixel; o = odd pixel

The matrix equations are these considering the digital quantization:

R = Y + 1.375 V
G = Y − 0.703125 V − 0.34375 U
B = Y + 1.734375 U.

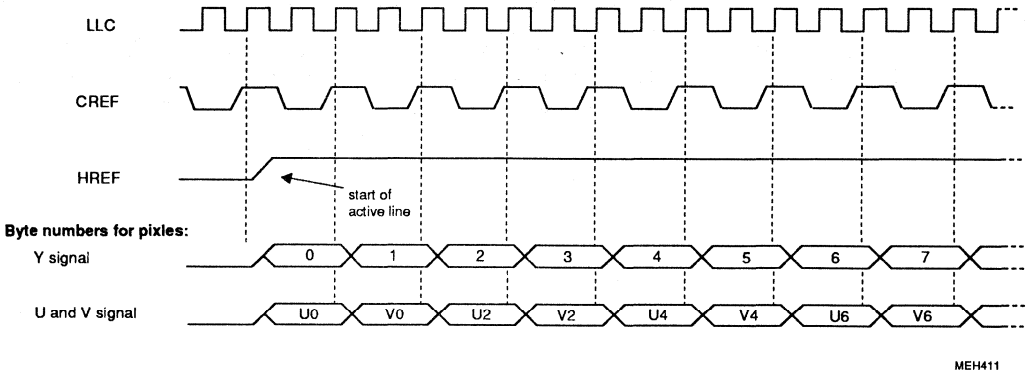
Anti-gamma ROM tables:
ROM tables are implemented at the matrix output to provide anti-gamma correction of the RGB data. A curve for a gamma of 1.4 is implemented according to the following equation:

$$data = round\ (255\ (addr / 255)^{1.4}) + 4$$

The tables can be used (RTB-bit = 0) to compensate gamma correction for linear data representation of RGB output data.

Chrominance signal keyer

The keyer generates an alpha signal to achieve a 5-5-5 +1 RGB alpha output signal. Therefore, the processed UV data amplitudes are compared with thresholds set via



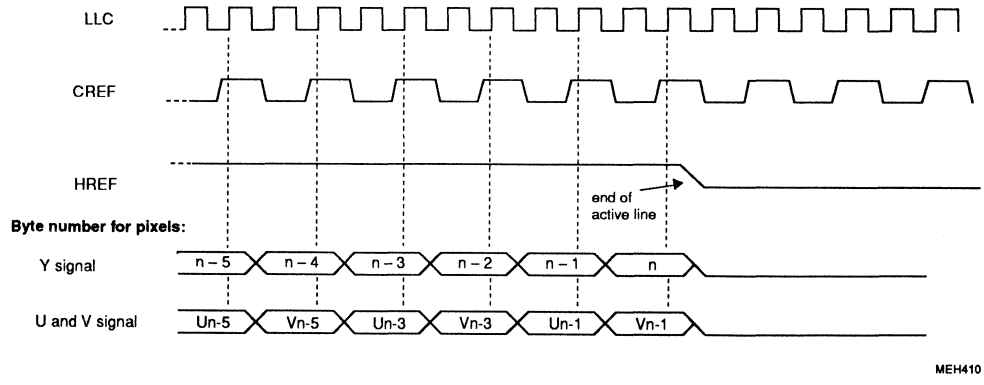


Fig.3 Horizontal and data multiplex timing.

I²C-bus (subaddresses "0C to 0F"). A logical "1" signal is generated if the amplitude is inside the specified amplitude range, otherwise a logical "0" is generated.
Keying can be switched off by setting the lower limit higher than the upper limit ("0C or 0E" and "0D or 0F").

Scale control and vertical regions

The scale control block SC includes vertical address/sequence counters to define the current position in the input field and to address the internal VPU memories.
To perform scaling, XD of XS pixel selection in horizontal direction and YD of YS line selection in vertical direction are applied. The pixel and line dropping are controlled at the input of the FIFO register.
To control the decimation filter function and the vertical data processing in the adaptive mode (AFS = 1), the scaling ratio in horizontal and vertical direction is estimated in the SC block.

The input field can be divided into two vertical regions – the bypass region and the scaling region, which are defined via I²C-bus by the parameters VS, VC, YO and YS.

Vertical bypass region:

Data are not scaled and the output format is always 8-bit grayscale (monochrome). The SAA7186 outputs all active pixels of a line, defined by the HREF input signal if the vertical bypass region is active. This can be used, for example, to store videotext information in the field memory.

The start line of the bypass region is defined by VS; the number of lines to be bypassed is defined by VC.

Vertical scaling region:

Data is scaled with start at line YO and the output format is choosen. This is the "normal operation" area.

The input/output screen dimensions in horizontal and vertical direction are defined by the parameters

XO, XS and XD for horizontal

YO, YS and YD for vertical.

The circuit processes XS samples of a line. Remaining pixels are ignored if a line is longer than XS. If a line is shorter than XS, processing is aborted when the falling edge of HREF is detected.

Vertical regions in Fig.4:

- the two regions an be programmed via I²C-bus, whereby regions should not overlap (active region overrides the bypass region).
- the start of a normal active picture depends on video standard and has to be programmed to the correct value.
- the offsets XO and YO are set according to the internal processing delays to ensure the complete number of destination pixels and lines.
- the scaling parameters can be used to perform a panning function over the video frame/field.

Output data representation and levels

Output data representation of the YUV data can be modified by bit

MCT (subaddress 10).
The DC gain is 1 for YUV input data. The corresponding RGB levels are defined by the matrix equations. The luminance levels are limited according to CCIR 601

16 (239) = black
235 (20) = white
(..) = grayscale luminance levels if the YUV or monochrome luminance output formats are selected.

The signal levels of the RGB formats are limited in 8-bit to "0" or "255". For the 5-bit RGB formats a truncation from 8-bit to 5-bit is implemented.

Fill values are inserted dependent on longword position and destination size:

- "0" in RGB formats and for Y two'2 complement U, V
- "128" for U, V (straight binary)
- "255" in 8-bit grayscale format

The unused output values of the YUV and grayscale formats can be used for other purposes.

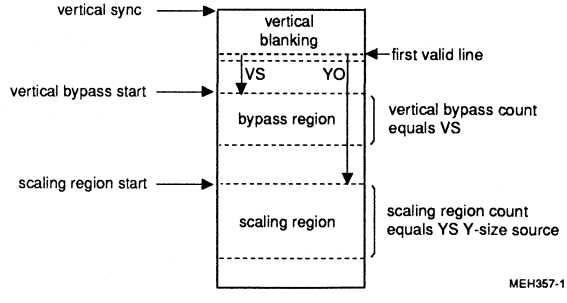


Fig.4 Vertical regions.

Table 2 VRAM port output data formats at EFE-bit = 0 dependend on FS1 and FS0 bits (set via I²C-bus)

PIXEL OUTPUT BITS	FS1 = 0; FS0 = 0 RGB 5-5-5 + 1 32-BIT WORDS			FS1 = 0; FS0 = 1 YUV 4:2:2 32-BIT WORDS			FS1 = 1; FS0 = 0 YUV 4:2:2 TEST 16-BIT WORDS			FS1 = 1; FS0 = 1 8-bit monochrome 32-BIT WORDS		
PIXEL ORDER	n	n+2	n+4	n	n+2	n+4	n	n+1	n+2	n n+1	n+4 n+5	n+8 n+9
VRO31	α	α	α	Ye7	Ye7	Ye7	Ye7	Yo7	Ye7	Ya7	Ya7	Ya7
VRO30	R4	R4	R4	Ye6	Ye6	Ye6	Ye6	Yo6	Ye6	Ya6	Ya6	Ya6
VRO29	R3	R3	R3	Ye5	Ye5	Ye5	Ye5	Yo5	Ye5	Ya5	Ya5	Ya5
VRO28	R2	R2	R2	Ye4	Ye4	Ye4	Ye4	Yo4	Ye4	Ya4	Ya4	Ya4
VRO27	R1	R1	R1	Ye3	Ye3	Ye3	Ye3	Yo3	Ye3	Ya3	Ya3	Ya3
VRO26	R0	R0	R0	Ye2	Ye2	Ye2	Ye2	Yo2	Ye2	Ya2	Ya2	Ya2
VRO25	G4	G4	G4	Ye1	Ye1	Ye1	Ye1	Yo1	Ye1	Ya1	Ya1	Ya1
VRO24	G3	G3	G3	Ye0	Ye0	Ye0	Ye0	Yo0	Ye0	Ya0	Ya0	Ya0
VRO23	G2	G2	G2	Ue7	Ue7	Ue7	Ue7	Ve7	Ue7	Yb7	Yb7	Yb7
VRO22	G1	G1	G1	Ue6	Ue6	Ue6	Ue6	Ve6	Ue6	Yb6	Yb6	Yb6
VRO21	G0	G0	G0	Ue5	Ue5	Ue5	Ue5	Ve5	Ue5	Yb5	Yb5	Yb5
VRO20	B4	B4	B4	Ue4	Ue4	Ue4	Ue4	Ve4	Ue4	Yb4	Yb4	Yb4
VRO19	B3	B3	B3	Ue3	Ue3	Ue3	Ue3	Ve3	Ue3	Yb3	Yb3	Yb3
VRO18	B2	B2	B2	Ue2	Ue2	Ue2	Ue2	Ve2	Ue2	Yb2	Yb2	Yb2
VRO17	B1	B1	B1	Ue1	Ue1	Ue1	Ue1	Ve1	Ue1	Yb1	Yb1	Yb1
VRO16	B0	B0	B0	Ue0	Ue0	Ue0	Ue0	Ve0	Ue0	Yb0	Yb0	Yb0
PIXEL ORDER	n+1	n+3	n+5	n+1	n+3	n+5	OUTPUTS NOT USED			n+2 n+3	n+6 n+7	n+10 n+11
VRO15	α	α	α	Yo7	Yo7	Yo7	X	X	X	Yc7	Yc7	Yc7
VRO14	R4	R4	R4	Yo6	Yo6	Yo6	X	X	X	Yc6	Yc6	Yc6
VRO13	R3	R3	R3	Yo5	Yo5	Yo5	X	X	X	Yc5	Yc5	Yc5
VRO12	R2	R2	R2	Yo4	Yo4	Yo4	X	X	X	Yc4	Yc4	Yc4
VRO11	R1	R1	R1	Yo3	Yo3	Yo3	X	X	X	Yc3	Yc3	Yc3
VRO10	R0	R0	R0	Yo2	Yo2	Yo2	X	X	X	Yc2	Yc2	Yc2
VRO9	G4	G4	G4	Yo1	Yo1	Yo1	X	X	X	Yc1	Yc1	Yc1
VRO8	G3	G3	G3	Yo0	Yo0	Yo0	X	X	X	Yc0	Yc0	Yc0
VRO7	G2	G2	G2	Ve7	Ve7	Ve7	X	X	X	Yd7	Yd7	Yd7
VRO6	G1	G1	G1	Ve6	Ve6	Ve6	X	X	X	Yd6	Yd6	Yd6
VRO5	G0	G0	G0	Ve5	Ve5	Ve5	X	X	X	Yd5	Yd5	Yd5
VRO4	B4	B4	B4	Ve4	Ve4	Ve4	X	X	X	Yd4	Yd4	Yd4
VRO3	B3	B3	B3	Ve3	Ve3	Ve3	X	X	X	Yd3	Yd3	Yd3
VRO2	B2	B2	B2	Ve2	Ve2	Ve2	X	X	X	Yd2	Yd2	Yd2
VRO1	B1	B1	B1	Ve1	Ve1	Ve1	X	X	X	Yd1	Yd1	Yd1
VRO0	B0	B0	B0	Ve0	Ve0	Ve0	X	X	X	Yd0	Yd0	Yd0

α = keying bit; R, G, B, Y. U and V = digital signals; e = even pixel number; o = odd pixel number;
a b c d = consecutive pixels

Table 3 VRAM port output data formats at EFE-bit = 1 dependend on FS1 and FS0 bits (set via I²C-bus)

PIXEL OUTPUT BITS	FS1 = 0; FS0 = 0 RGB 5-5-5 + 1 16-BIT WORDS			FS1 = 0; FS0 = 1 YUV 4:2:2 16-BIT WORDS			FS1 = 1; FS0 = 0 RGB 8-8-8 24-BIT WORDS			FS1 = 1; FS0 = 1 8-bit monochrome 16-BIT WORDS		
PIXEL ORDER	**n**	**n+1**	**n+2**	**n**	**n+1**	**n+2**	**n**	**n+1**	**n+2**	**n n+1**	**n+2 n+3**	**n+4 n+5**
VRO31	α	α	α	Ye7	Yo7	Ye7	R7	R7	R7	Ya7	Ya7	Ya7
VRO30	R4	R4	R4	Ye6	Yo6	Ye6	R6	R6	R6	Ya6	Ya6	Ya6
VRO29	R3	R3	R3	Ye5	Yo5	Ye5	R5	R5	R5	Ya5	Ya5	Ya5
VRO28	R2	R2	R2	Ye4	Yo4	Ye4	R4	R4	R4	Ya4	Ya4	Ya4
VRO27	R1	R1	R1	Ye3	Yo3	Ye3	R3	R3	R3	Ya3	Ya3	Ya3
VRO26	R0	R0	R0	Ye2	Yo2	Ye2	R2	R2	R2	Ya2	Ya2	Ya2
VRO25	G4	G4	G4	Ye1	Yo1	Ye1	R1	R1	R1	Ya1	Ya1	Ya1
VRO24	G3	G3	G3	Ye0	Yo0	Ye0	R0	R0	R0	Ya0	Ya0	Ya0
VRO23	G2	G2	G2	Ue7	Ue7	Ue7	G7	G7	G7	Yb7	Yb7	Yb7
VRO22	G1	G1	G1	Ue6	Ue6	Ue6	G6	G6	G6	Yb6	Yb6	Yb6
VRO21	G0	G0	G0	Ue5	Ue5	Ue5	G5	G5	G5	Yb5	Yb5	Yb5
VRO20	B4	B4	B4	Ue4	Ue4	Ue4	G4	G4	G4	Yb4	Yb4	Yb4
VRO19	B3	B3	B3	Ue3	Ue3	Ue3	G3	G3	G3	Yb3	Yb3	Yb3
VRO18	B2	B2	B2	Ue2	Ue2	Ue2	G2	G2	G2	Yb2	Yb2	Yb2
VRO17	B1	B1	B1	Ue1	Ue1	Ue1	G1	G1	G1	Yb1	Yb1	Yb1
VRO16	B0	B0	B0	Ue0	Ue0	Ue0	G0	G0	G0	Yb0	Yb0	Yb0
PIXEL ORDER	**n**	**n+1**	**n+2**	**n**	**n+1**	**n+2**	**n**	**n+1**	**n+2**	**n n+1**	**n+2 n+3**	**n+4 n+5**
VRO15	X	X	X	X	X	X	B7	B7	B7	X	X	X
VRO14	X	X	X	X	X	X	B6	B6	B6	X	X	X
VRO13	X	X	X	X	X	X	B5	B5	B5	X	X	X
VRO12	X	X	X	X	X	X	B4	B4	B4	X	X	X
VRO11	X	X	X	X	X	X	B3	B3	B3	X	X	X
VRO10	X	X	X	X	X	X	B2	B2	B2	X	X	X
VRO9	X	X	X	X	X	X	B1	B1	B1	X	X	X
VRO8	X	X	X	X	X	X	B0	B0	B0	X	X	X
VRO7 (1)	α	α	α	α	X	α	α	α	α	α	α	α
VRO6	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E
VRO5 (2)	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT
VRO4 (2)	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT
VRO3	X	X	X	X	X	X	X	X	X	X	X	X
VRO2	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF
VRO1 (2)	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ
VRO0 (2)	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ

α = keying bit; R, G, B, Y. U and V = digital signals; e = even pixel number; o = odd pixel number; a b c d = consecutive pixels; O/E = odd/even flag

(1) YUV 16-bit format: the keying signal α is defined only for YU time steps. The corresponding YV sample has also to be keyed. The α signal in monochrome mode can be used only in the transparent mode (TTR = 1), in this case Ya = Yb.

(2) Data valid only when transparent mode active (TTR-bit = 1) and VCLK pin connected to LLC/2 clock rate.

Output FIFO register and VRAM output port

The output FIFO register is the buffer between the video data stream and the VRAM data input port. Resized video data are buffered and formatted. 32-, 24- and 16-bit video data modes are supported. The various formats are selected by the bits EFE, FS1 and FS0. VRAM port formats are shown in Tables 2 and 3. The FIFO register capacity is 16 word x 32 bit (for 32-, 24-, or 16-bit video data).

VRAM port inputs are:
VCLK to clock the FIFO register output data and VOEN to enable output data.

VRAM port outputs are:
the HFL flag (half-full flag), the signal INCADR (refer to section "data burst transfer") and the reference signals for pixel and line selection on outputs VRO(7-0) (only for 24- and 16-bit video data formats refer to "transparent data transfer").

VRAM port transfer procedures

Data transfer on the VRAM port can be done asynchroneously controlled by outputs HFL, INCADR and input VCLK (data burst transfer with bit TTR = 0).

Data transfer on the VRAM port can be done synchroneously controlled by output reference signals on outputs VRO(7-0) and a clock rate of LLC/2 on input VCLK (transparent data transfer with bit TTR = 1).

The scaling capability of the SAA7186 can be used in various applications.

Data burst transfer mode

Data transfer on the VRAM port is asynchroneously (TTR = 0). This mode can be used for all output formats. Four signals for communication with the external memory are provided.

- HFL flag, the half-full flag of the FIFO output register is raised when the FIFO contains at least 8 data words (HFL = HIGH).
  By setting HFL = 1, the SAA7186 requests a data burst transfer by the external memory controller, that has to start a transfer cycle within the next 32 LLC cycles for 32-bit longword modes (16 LLC cycles for 16- and 24-bit modes). If there are pixels in the FIFO at the end of a line, which are not transferred, the circuit fills up the FIFO register with "fill pixels" until it is half-full and sets the HFL flag to request a data burst transfer. After transfer is done, HFL is used in combination with INCADR to indicate the line increments (Figures 6 and 7).
- INCADR output signal is used in combination with HFL to control horizontal and vertical address generation for a memory controller. The pulse sequence depends on field formats (interlace/ non-interlace or odd/even fields, Figures 6 and 7) and control bits OF (subaddress 00).

  HFL = 1 at the rising edge of INCADR:

  the end of line is reached, line address is incremented and pixel address reset

  HFL = 0 at the rising edge of INCADR:

  the end of field/frame is reached, line and pixel addresses are reset

  (The distance from the last half-full request HFL to the INCADR pulse may be longer than 64 x LLC. The HFL state is defined for minimum 4 x LLC in front of the rising edge of INCADR and minimum 2 x LLC afterwards.)
- VCLK input signal to clock the FIFO register output data VRO(n). New data are placed on the VRO(n) port with the rising edge of VCLK (Fig.5).
- VOEN input enables output data VRO(n).The outputs are in 3-state mode at VOEN = HIGH.
  VOEN changes only when VCLK is LOW. If VCLK pulses are applied during VOEN = HIGH, the outputs remain inactive, but the FIFO register accepts the pulses.

Transparent data transfer mode

Data transfer on the VRAM port can be achieved synchroneously (TTR =1) controlled by output reference signals on outputs VRO(7-0), and a contineous clock rate of LLC/2 on input VCLK. The SAA7186 delivers a contineously processed data stream. Therefore, the extended formats of the VRAM output port are selected (bit EFE = 1; Table 3).
The output signals VRO(7-0) can be used to buffer qualified pre-processed RGB or YUV video data. Control output signals in Table 3 are:

α	keying signal of the chroma keyer
O/E	odd/even field bit according to the internal field processing
VGT	vertical gate signal, "1" marks the scaling window in vertical direction from YO to (YO + YS) lines, cut by VS.
HGT	horizontal gate signal, "1" marks horizontal direction from XO to (XO + XS) lines, cut by HREF.
HRF	delay compensated horizontal reference signal.
LNQ	line qualifier signal, active polarity is defined by QPL bit.
PXQ	pixel qualifier signal, active polarity is defined by QPP bit.

Power-on reset

- the FIFO register contents are undefined
- outputs VRO are set to high-impedance state
- output INCADR = HIGH
- output HFL = LOW until the VPE bit is set to "1"
- subaddress "10" is set to 00h and VPE-bit in subaddress "00" is set to zero (Table 4)

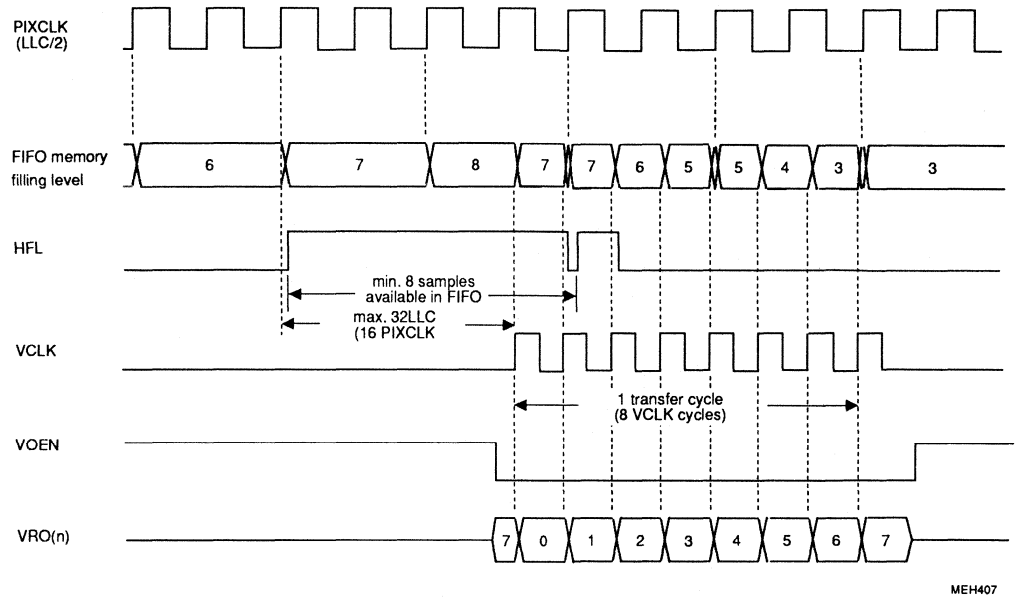


Fig.5 Output port transfer to VRAM at 32-bit data format without scaling. If VCLK cycles occur at VOEN = HIGH, the FIFO register is unchanged, but the outputs VRO(31-0) remain in 3-state position.

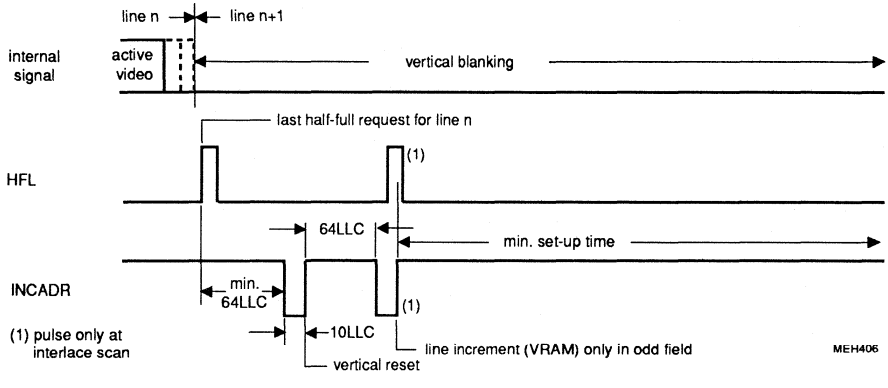


Fig.6 Vertical reset timing to the VRAM.

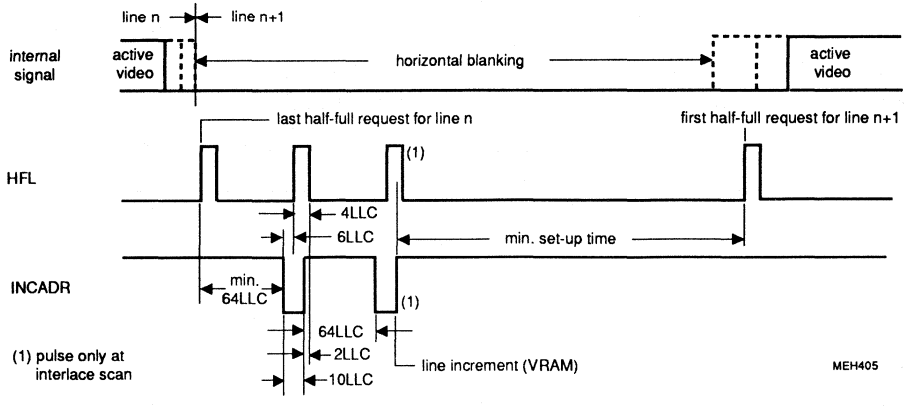


Fig.7 Horizontal increment timing to the VRAM.

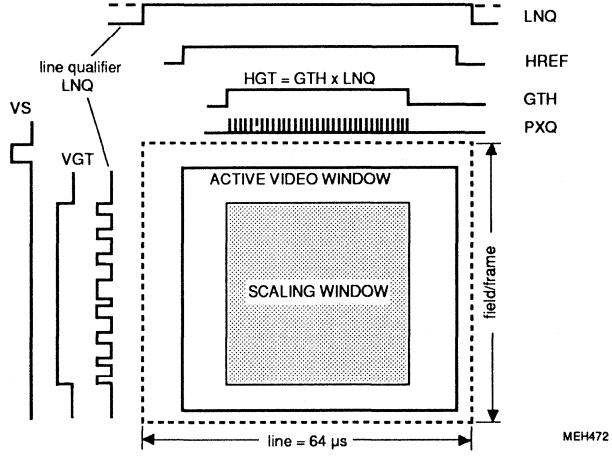


Fig.8 Reference signals for scaling window.

Field processing

The phase of the field sequence (odd/even dependent on inputs HREF and VS) is detected by means of the falling edge of VS. The current field phase is reported in the status byte by the OEF bit (Table 5). OEF bit can be stable 0 or 1 for non-interlaced input frames or non standard input signals VS and/or HREF (nominal condition for VS and HREF – SAA7191 B with active vertical noise limiter). A free-running odd/even flag is generated for internal field processing if the detection reports a stable OEF bit. The POE bit (subaddress 0B) can be used to change the polarity of the internal flag (in case of non-standard VS and HREF signals) to control the phase of the free-running flag, and to compensate mis-detections. Thus, the SAA7186 can be used under various VS/HREF timing conditions.

The SAA7186 operates on fields. To support progressive displays and to avoid movement blurring and artifacts, the circuit can process both or single fields of interlaced or non-interlaced input data. Therefore the OF bits can be used. The bits OF1 and OF0 (Table 6) determine the INCADR/HFL generation in "data burst transfer mode". One of the fields (odd or even) is ignored when OF1 = 1; then no line increment sequence (INCADR/HFL) is generated, the vertical reset pulse is only generated.

With OF1 = OF0 = 0 the circuit supports correct interlaced data storage. Two INCADR/HFL sequences are generated in each qualified line; additionally an INCADR/HFL sequence after the vertical reset sequence of an odd field is generated. Thereby, the scaled lines are automatically stored in the right sequence.

Operation cycle

The operation is synchronized by the input field. The cycle is specified in the flow chart (Fig.9).
The circuit is inactive after power-on reset, VPO is 0 and the FIFO control is set "empty". The internal control registers are updated with the falling edge of VS signal. The circuit is switched active and waits for a transmission of VS and a vertical reset sequence to the memory controller. Afterwards, the circuit waits for the beginning of a scaling or bypass region. The processing of a current line is finished when a vertical sync pulse appears. The circuit performs a coefficient update and generates a new vertical reset (if it is still active).

Line processing starts when a line is decided to be active, the circuit starts to scale it. Active pixels are loaded into the FIFO register. An HFL flag is generated to initialize a data transfer when eight words are completed. The line end is reached when the programmed pixel number is processed or when a horizontal sync pulse occurs. If there are pixels in the FIFO register, it is filled up until it is half-full to cause a data transfer. Horizontal increment pulses are transmitted after this data transfer.

Remarks:
The SAA7186 will always wait for the HREF/VS pulse before the line increment/vertical reset sequence is performed.
After each line/field, the FIFO control is set to empty when INCADR/HFL sequence is transmitted.
No additional actions are necessary if the memory controller has ignored the HFL signal. There is no need to handle overflow/underflow of the FIFO register.

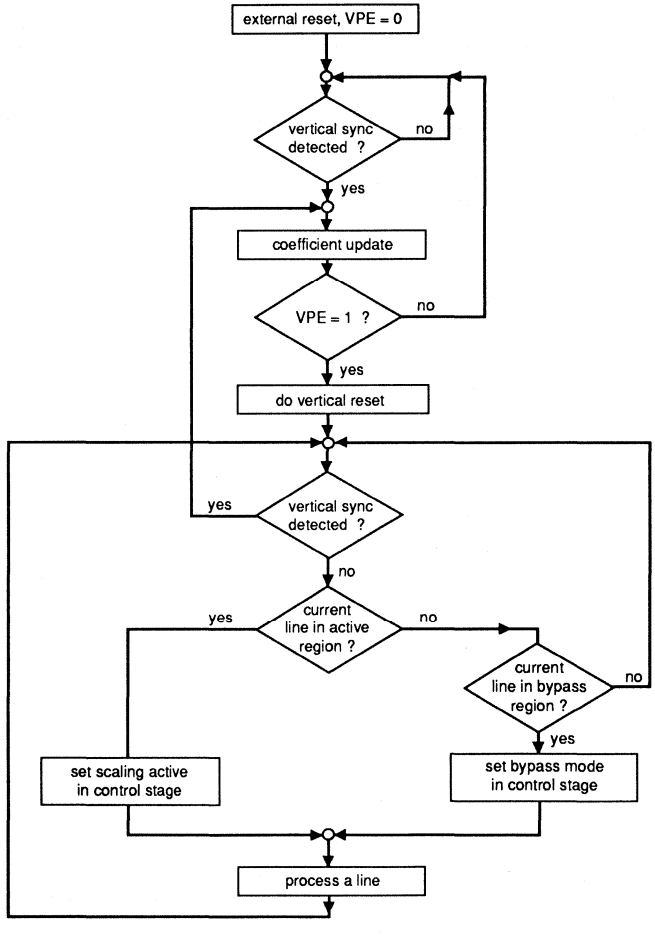


Fig.9 Operation cycle

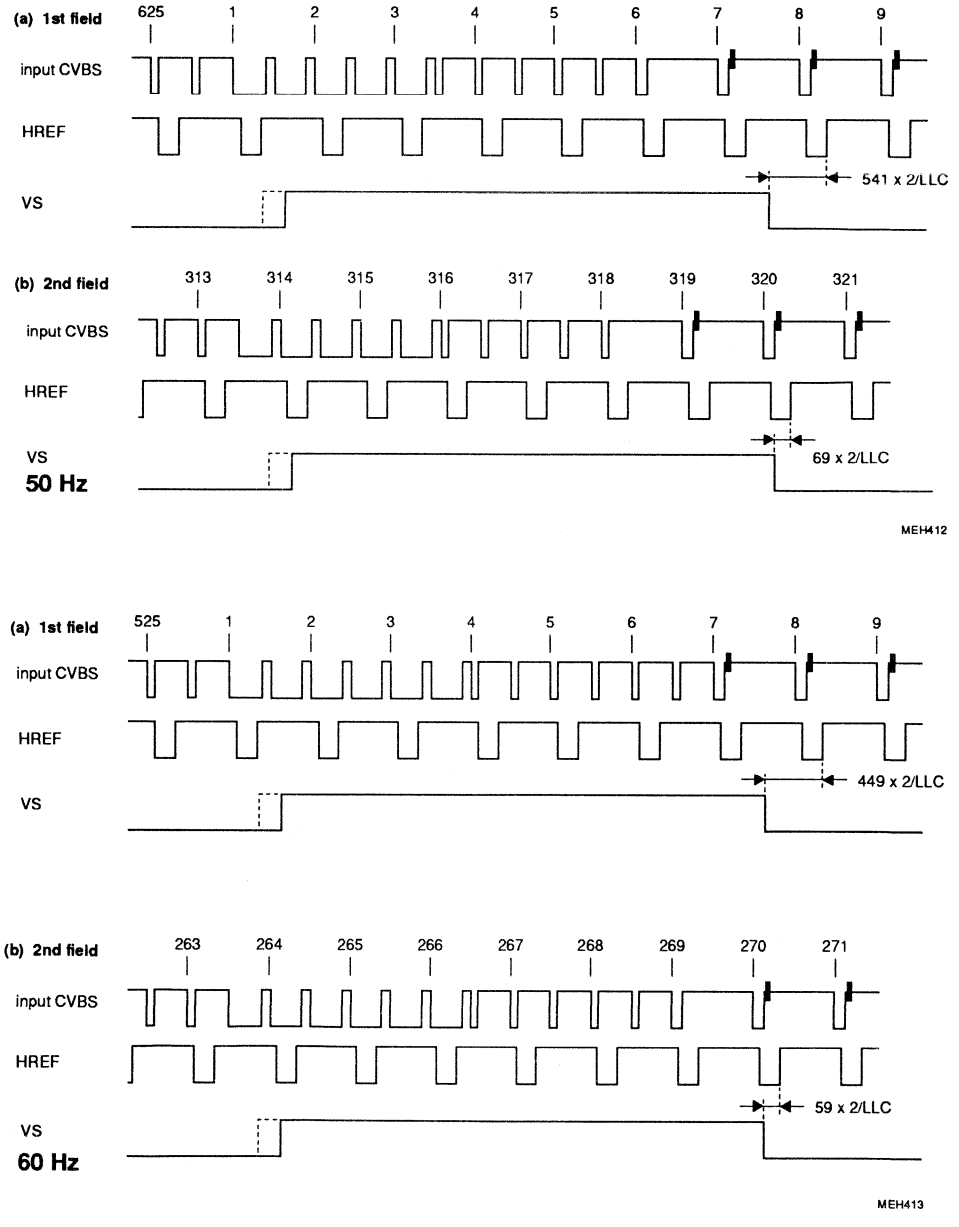


Fig.10 VS timing for video input port (CVBS).

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A		DATAn	A	P

S = start condition
SLAVE ADDRESS = **1000 100X** (IICSA = LOW) **or 1011 110X** (IICSA = HIGH)
A = acknowledge, generated by the slave
SUBADDRESS* = subaddress byte (Table 4)
DATA = data byte (Table 4)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 4 I²C-bus; subaddress and data bytes for writing (X in address byte = 0).

FUNCTION	SUBADDRESS	DATA D7	D6	D5	D4	D3	D2	D1	D0	DF*
Formats and sequence	00	RTB	OF1	OF0	VPE	LW1	LW0	FS1	FS0	tbf
Output data pixel/line	01	XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0	
continued in	04							XD9	XD8	
Input data pixel/line	02	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
continued in	04					XS9	XS8			
Horizontal window start	03	XO7	XO6	XO5	XO4	XO3	XO2	XO1	XO0	
Pixel decimation filter	04	HF2	HF1	HF0	XO8	XS9	XS8	XD9	XD8	
Output data lines/field	05	YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0	
continued in	09							YD9	YD8	
Input data lines/field	06	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
continued in	09					YS9	YS8			
Vertical window start	07	YO7	YO6	YO5	YO4	YO3	YO2	YO1	YO0	
AFS/vertical processing	08	AFS	VP1	VP0	YO8	YS9	YS8	YD9	YD8	
Vertical bypass start	09	VS7	VS6	VS5	VS4	VS3	VS2	VS1	VS0	
continued in	0B				VS8					
Vertical bypass count	0A	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0	
continued in	0B	0	TCC	0	VS8	0	VC8	0	POE	
Chroma keying										
lower limit for V	0C	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	
upper limit for V	0D	VU7	VU6	VU5	VU4	VU3	VU2	VU1	VU0	
lower limit for U	0E	UL7	UL6	UL5	UL4	UL3	UL2	UL1	UL0	
upper limit for U	0F	UU7	UU6	UU5	UU4	UU3	UU2	UU1	UU0	
Byte 10**	10	0	0	0	MCT	QPL	QPP	TTR	EFE	
Unused	11 to 1F									

*) Default register contents fill in by hand
**) Byte 10 is set to 00h after power-on reset.

Table 5 I²C-bus status byte (X in address byte = 1)

FUNCTION		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
status byte		ID3	ID3	ID3	ID3	0	0	OEF	SVP

Function of status bits:

ID3 to ID0 — Software version of SAA7186 compatible with

ID3	ID2	ID1	ID0	version
0	0	0	1	1

OEF — Identification of field sequence dependent on inputs HREF and VS:
0 = even field detected; 1 = odd field detected

SVP — State of VRAM port:
0 = inputs HFL and INCADR inactive;
1 = inputs HFL and INCADR active.

Table 6 Function of the register bits of Table 4

"00" RTB — ROM table bypass switch: 0 = anti-gamma ROM active; 1 = table is bypassed

OF1 to OF0 — Set output field mode:

OF1	OF0	field mode DVS process
0	0	both fields for interlaced storage
0	1	both fields for non-interlaced storage
1	0	odd fields only (even fields ignored) for non-interlaced storage
1	1	even fields only(odd fields ignored) for non-interlaced storage

VPE — VRAM port outputs enable: 0 = HFL and INCADR inactive; VRO outputs in 3-state position (HFL = LOW, INCADR = HIGH)
1 = HFL and INCADR enabled; VRO outputs dependent on VOEN

LW1 to LW0 — First pixel position in VRO data for FS1 = 0; FS0 = 0 (RGB) and FS1 = 0; FS0 = 1(YUV):

LW1	LW0	31 to 24	23 to 16	15 to 8	7 to 0	
0	0	pixel 0	pixel 0	pixel 1	pixel 1	EFE = 0
0	1	pixel 0	pixel 0	pixel 1	pixel 1	
1	0	black	black	pixel 1	pixel 1	
1	1	black	black	pixel 1	pixel 1	

First pixel position in VRO data for FS1 = 1; FS0 = 1 (monochrome):

LW1	LW0	31 to 24	23 to 16	15 to 8	7 to 0	
0	0	pixel 0	pixel 1	pixel 2	pixel 3	EFE = 0
0	1	black	pixel 0	pixel 1	pixel 2	
1	0	black	black	pixel 2	pixel 3	
1	1	black	black	black	pixel 3	
0	0	pixel 0	pixel 1	X	X	EFE = 1
0	1	black	pixel 0	X	X	
1	0	pixel 0	pixel 1	X	X	
1	1	black	pixel 0	X	X	

FS1 to FS0

FIFO output register format select (EFE- bit see "10"):

EFE	FS1	FS0	output format (Tables 2 and 3)
0	0	0	RGB 5-5-5 + alpa; 2x16-bit/pixel; 32-bit word length; RGB matrix on, VRAM output format
0	0	1	YUV 4:2:2; 2x16-bit/pixel; 32-bit word length; RGB matrix off, VRAM output format
0	1	0	YUV 4:2:2; video test mode; 1x16-bit/pixel;16-bit word length; RGB matrix off, optional output format
0	1	1	monochrome mode; 4x8-bit/pixel; 32-bit word length; RGB matrix off, VRAM output format
1	0	0	RGB 5-5-5 + alpa; 1x16-bit/pixel; 16-bit word length; RGB matrix on, VRAM output + transparent format
1	0	1	YUV 4:2:2 + alpa; 1x16-bit/pixel; 16-bit word length; RGB matrix off, VRAM output + transparent format
1	1	0	RGB 8-8-8 + alpa; 1x24-bit/pixel; 24-bit word length; RGB matrix on, VRAM output + transparent format
1	1	1	monochrome mode; 2x8-bit/pixel; 16-bit word length; RGB matrix off, VRAM output + transparent format

"01 and 04"
XD9 to XD0

Pixel number per line (straight binary) on output (VRO):
00 0000 0000 to 11 1111 1111 (number of XS pixels as a maximum)

"02 and 04"
XS9 to XS0

Pixel number per line (straight binary) on inputs (YIN and UVIN):
00 0000 0000 to 11 1111 1111 (number of input pixels per line as maximum)

"03 and 04"
XO8 to XO0

Horizontal start position (straight binary) of scaling window (take care of active pixel number per line).

start with 1st pixel after HREF rise = tbf (0000 0000 to 1111 1111)

window start and window end may be cut by internal delay compensated HREF = 0 phase. XO has to be matched to the internal processing delay to get full scaling range

"04"
HF2 to HF0

Horizontal decimation filter

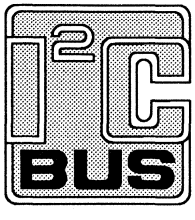
HF2	HF1	HF0	taps	filter
0	0	0	2	filter 1 $(1/2\ (1 + z^{-1}))$
0	0	1	3	filter 2 $(1/4\ (1 + 2z^{-1} + z^{-2}))$
0	1	0	5	filter 3 $(1/8\ (1 + 2z^{-1} + 2z^{-2} + 2z^{-3} + z^{-4}))$
0	1	1	9	filter 4 $(1/16\ (1 + 2z^{-1} + 2z^{-2} + 2z^{-3} + 2z^{-4} + 2z^{-5} + 2z^{-6} + 2z^{-7} + z^{-8}))$
1	0	0	1	filter bypassed
1	0	1	1	filter bypassed + delay in Y channel of 1T
1	1	0	8	filter 5 $(1/16\ (1 + 3z^{-1} + 3z^{-2} + z^{-3} + z^{-4} + 3z^{-5} + 3z^{-6} + z^{-7}))$
1	1	1	4	$(1/8\ (1 + 3z^{-1} + 3z^{-2} + z^{-3}))$

"05 and 08"
YD9 to YD0

Line number per output field (straight binary):
00 0000 0000 to 11 1111 1111 (number of YS lines as a maximum)

"06 and 08" YS9 to YS0	Line number per input field (straight binary): 00 0000 0000 0 line 11 1111 1111 1023 lines (maximum = number of lines/field – 3)
"07 and 08" YO8 to YO0	Vertical start of scaling window. "0" equals 3rd line after rising slope of VS input signal. Take care of active line number per field (straight binary). 0 0000 0000 start with 3rd line after the rising slope of VS 1 1111 1111 511 + 3 lines after the rising slope of VS (maximum value)
"08" AFS	Adaptive filter switch: 0 = off; use VP1, VP0 and HF2 to HF0 bits 1 = on; filter characteristics are selected by the scaler
VP1 to VP0	Vertical data processing VP1 VP0 | processing 0 0 | bypassed 0 1 | delay of one line $H(z) = z^{-H}$ 1 0 | vertical filter 1 consecutive with line interpolation ($H(z) = 1/2\ (1 + z^{-H})$) 1 1 | vertical filter 2 consecutive with line interpolation ($H(z) = 1/4\ (1 + 2z^{-H} + z^{-2H})$)
"09 and 0B" VS8 to VS0	Vertical bypass start, sets begin of the bypass region (straight binary). Scaling region overrides bypass region (YO bits): 0 0000 0000 start with 3rd line after the rising slope of VS 1 1111 1111 511 + 3 lines after the rising slope of VS (maximum value)
"0A and 0B" VC8 to VC0	Vertical bypass count, sets length of bypass region (straight binary): 0 0000 0000 0 line length 1 1111 1111 511 lines length (maximum = number of lines/field – 3)
POE	Polarity, internally detected odd/even flag O/E: 0 = flag unchanged; 1 = flag inverted
"0C" VL7 to VL0	Set lower limit for V colour-difference signal (8 bit; two's complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level
"0D" VU7 to VU0	Set upper limit for V colour-difference signal (8 bit; two's complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level
"0E" UL7 to UL0	Set lower limit for U colour-difference signal (8 bit; two's complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level

"0F" UU7 to UU0	Set upper limit for U colour-difference signal (8 bit; two's complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level
"10" TCC	Two's complement input data select (U, V): 0 = binary input data 1 = two`complement input data
MCT	Monochrome and two's complement output data select: 0 = inverse grayscale luminance (if grayscale is selected by FS bits) or straight binary U, V data output 1 = non-inverse monochrome luminance (if grayscale is selected by FS bits) or two`complement U, V data output
QPL	Line qualifier polarity flag : 0 = LNQ is active-LOW (pin 1 and on VRO1, pin 99); 1 = LNQ is active-HIGH
QPP	Pixel qualifier polarity flag : 0 = PXQ is active-LOW (VRO0, pin 100); 1 = PXQ is active-HIGH
TTR	Transparent data transfer: 0 = normal operation (VRAM protocol valid,) 1 = FIFO register transparent (output FIFO in shift register mode)
EFE	Extended formats enable, FS-bits in subaddress "00"



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pins 5, 14, 26, 40, 55, 67, 76 and 91)	−0.5	6.5	V
V_I	DC input voltage on all pins	−0.5	V_{DD}	V
I_{DD}	supply current (pins 5, 14, 26, 40, 55, 67, 76 and 91)	-	70	mA
P_{tot}	total power dissipation	0	1	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	-	±2000	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

DC CHARACTERISTICS

V_{DD1} to V_{DD8} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range (pins 5, 14, 26, 40, 55, 67, 76 and 91)		4.5	5	5.5	V
I_P	total supply current (I_{DD1} + I_{DD2} + I_{DD3} I_{DD4} + I_{DD5} + I_{DD6} + I_{DD7} + I_{DD8})	inputs LOW and outputs without load	-	80	-	mA
Data and control inputs						
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DD}+0.5	V
I_{LI}	input leakage current	V_{IL} = 0	-	-	10	µA
C_I	input capacitance	data	-	-	8	pF
		clocks	-	-	10	pF
Data and control outputs						
V_{OL}	output voltage LOW	note 1	-	-	0.6	V
V_{OH}	outputt voltage HIGH	note 1	2.4	-	-	V
3-state outputs						
$I_{O\,off}$	high-impedance output current		-	-	±5	µA
C_I	high-impedance output capacitance		-	-	8	pF
I²C-bus, SDA and SCL (pins 44 and 45)						
V_{IL}	input voltage LOW		−0.5	-	1.5	V
V_{IH}	input voltage HIGH		3	-	V_{DD}+0.5	V
$I_{44,45}$	input current		-	-	±10	µA
I_{ACK}	output current on pin 44	acknowledge	3	-	-	mA
V_{OL}	output voltage at acknowledge	I_{44} = 3 mA	-	-	0.4	V

AC CHARACTERISTICS

V_{DD1} to V_{DD8} = 4.5 to 5.5 V; T_{amb} = 0 to 60 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LLC timing (pin 36)		Fig.11				
t_{LLC}	cycle time		31	-	45	ns
t_p	pulse width (duty factor)	$t_{LLC\,H} / t_{LLC}$	40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
Input data timing		Fig.11				
t_{SU}	setup time		0	-	11	ns
t_{HD}	hold time		0	-	3	ns
VCLK timing (pin 51)		Fig.12				
t_{VCLK}	VRAM port clock cycle time	note 2	50	-	200	ns
$t_{p\,L}$, $t_{p\,H}$	LOW and HIGH times	note 3	17	-	-	ns
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
Output data and reference signal timing		Figures 11 and 12				
C_L	load capacitance	VRO outputs	15	-	40	pF
		other outputs	7.5	-	25	pF
t_{OH}	VRO data hold time	C_L = 10 pF; note 4	0	-	-	ns
t_{OHL}	related to LCC (INCADR, HFL)	C_L = 10 pF; note 5	0		-	ns
t_{OHV}	related to VCLK (HFL)	C_L = 10 pF; note 5	0		-	ns
t_{OD}	VRO data delay time	C_L = 40 pF; note 4	-	-	25	ns
t_{ODL}	related to LCC (INCADR, HFL)	C_L = 25 pF; note 5	-	-	60	ns
t_{ODV}	related to VCLK (HFL)	C_L = 25 pF; note 5	-	-	60	ns
t_D	output disable time to 3-state	C_L = 40 pF; note 6	-	-	40	ns
t_E	output enable time from 3-state	C_L = 40 pF; note 6	-	-	40	ns
$t_{HFL\ VOE}$	HFL maximum response time	VRAM port enabled	-	-	810	ns
$t_{HFL\ VCLK}$	HFL maximum response time	HFL set at beginning of VCLK burst	-	-	840	ns

Notes to the caracteristics

1. Levels are measured with load circuit. VRO outputs with 1.2 kΩ in parallel to 25 pF at 3 V (TTL load).
2. Maximum t_{VCLK} = 200 ns for test mode only depends on data format, horizontal scaling and input data rate.
3. Measured at 1,5 V level; $t_{p\,L}$ may be unlimited.
4. Timings of VRO refer to the rising edge of VLCK.
5. The timing of INCADR refers to LLC; the rising edge of HFL always refers to LLC. During a VRAM transfer is the falling edge of HFL generated by VCLK. Both edges of HFL refer to LLC during horizontal increment and vertical reset cycles.
6. Asynchronous signals with timing refering to the 1.5 V switching point of VOEN input signal (pin 50).

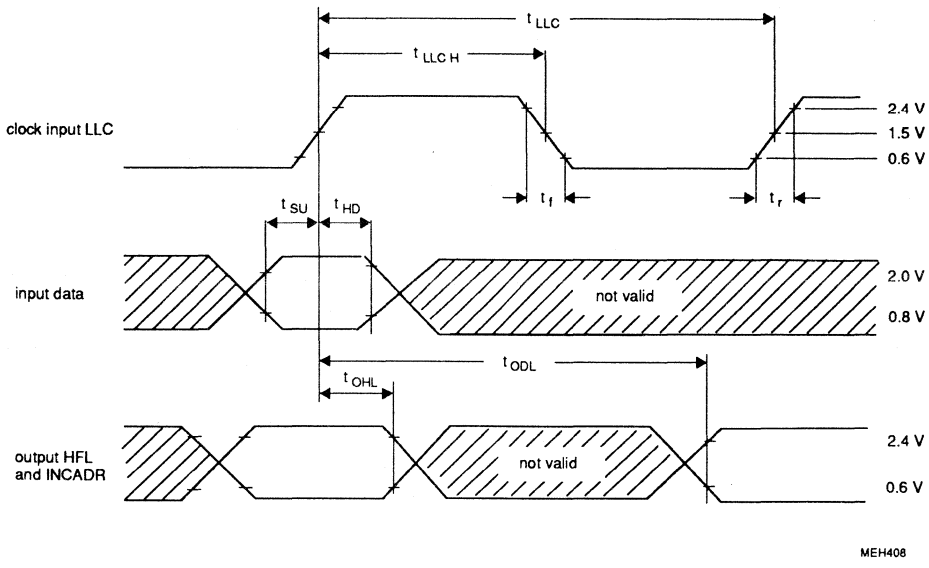


Fig.11 Data input timing

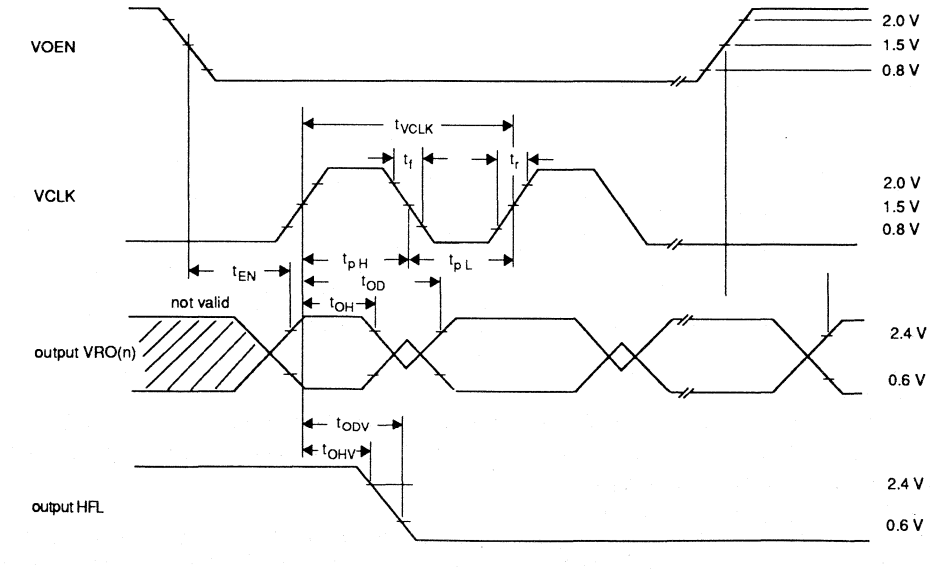


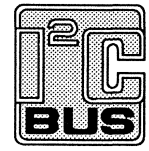
Fig.12 Data output timing (VCLK).

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	April 1992

SAA7191B

Digital multistandard colour decoder, square pixel (DMSD-SQP)



FEATURES

- Separate 8-bit luminance (Y or CVBS) and 8-bit chrominance inputs (CVBS or C) from CVBS, Y/C, S-Video (S-VHS or Hi8) sources
- Luminance and chrominance signal processing for standards PAL-B/G, NTSC-M, SECAM
- Horizontal and vertical sync detection for all standards
- Real-time control output RTCO to be used for frequency-locked digital video encoder (SAA7199B). RTCO contains serialized information about actual clock frequency, subcarrier frequency and PAL/SECAM sequence.
- Controls via the I²C-bus
- User programmable aperture correction (horizontal peaking)
- Compatible with memory-based features (line-locked clock)
- Cross-colour reduction by chrominance comb-filtering (NTSC) or by special cross colour cancellation (SECAM)
- 8-bit quantization of input signals
- 768/640 active samples per line equals 50/60 Hz (SQP)
- The YUV bus supports data rates of 780 x f_H equal to 12.2727 MHz for 60 Hz (NTSC-M) and 944 x f_H equal to 14.75 MHz for 50 Hz (PAL–B/G, SECAM) in 4 : 1 : 1 or 4 : 2 : 2 formats (via the I²C-bus)
- One crystal oscillator of 26.8 MHz

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage (pins 5, 18, 28, 37 and 52)	4.5	5	5.5	V
I_{DD}	total supply current (pins 5, 18, 28, 37 and 52)	-	100	250	mA
V_{IL}	input levels	TTL-compatible			
V_{OL}	output levels	TTL-compatible			
T_{amb}	operating ambient temperature	0	-	70	°C

GENERAL DESCRIPTION

The SAA7191B is a digital multistandard colour decoder suitable for 8-bit CVBS input signals or for 8-bit luminance and 8-bit chrominance input signals (Y/C).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7191B	68	PLCC	plastic	SOT188AA

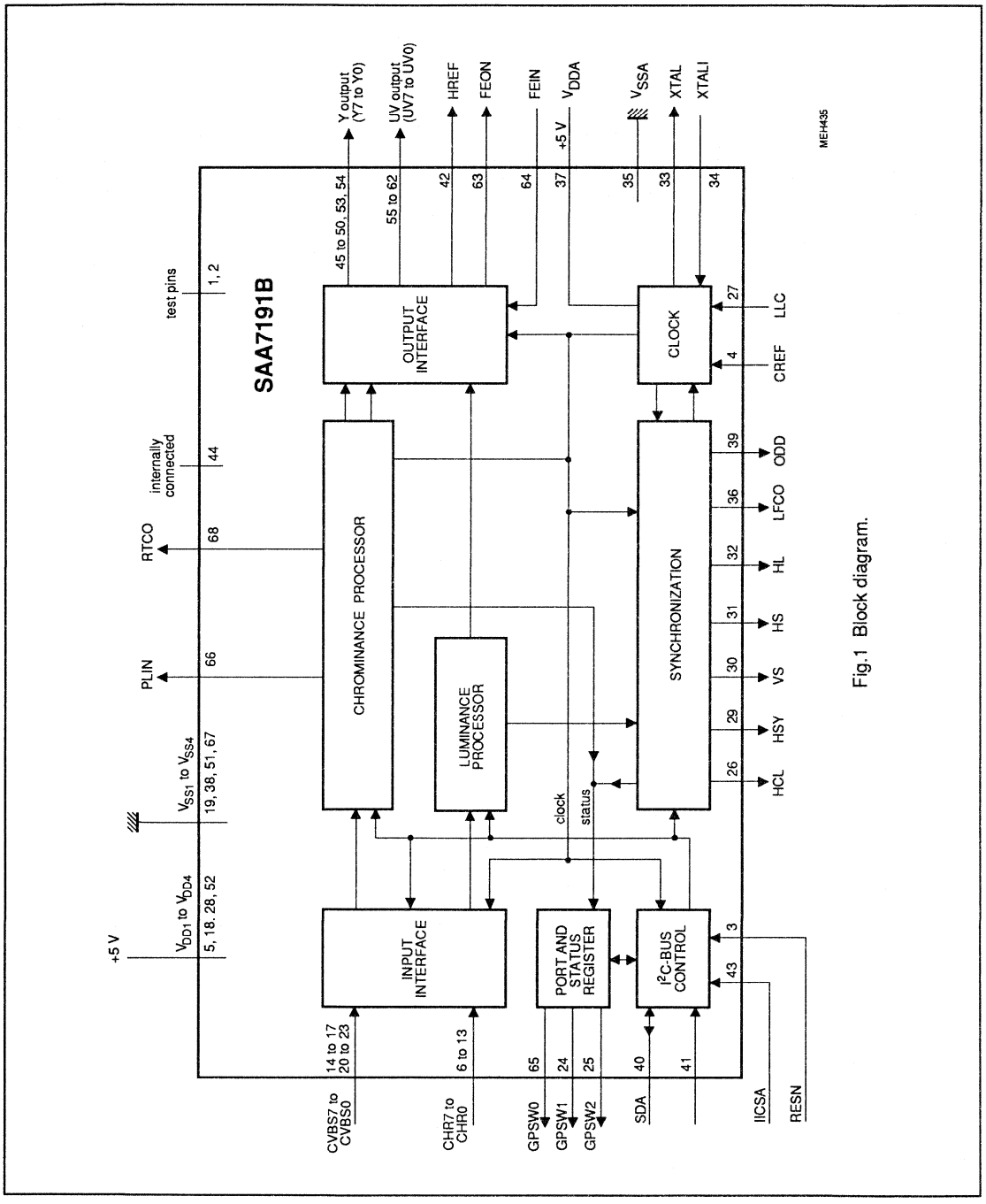


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SP	1	connected to ground (shift pin for testing)
AP	2	connected to ground (action pin for testing)
RESN	3	reset, active LOW
CREF	4	clock reference, sync from external to ensure in-phase signals on the YUV-bus
V_{DD1}	5	+5 V supply input 1
CHR0	6	chrominance input data bits CHR7 to CHR0 from a Y/C (VHS, Hi8) source in two's complement format
CHR1	7	
CHR2	8	
CHR3	9	
CHR4	10	
CHR5	11	
CHR6	12	
CHR7	13	
CVBS0	14	luminance respectively CVBS lower input data bits CVBS3 to CVBS0 (CVBS with luminance, chrominance and all sync information in two's complement format)
CVBS1	15	
CVBS2	16	
CVBS3	17	
V_{DD2}	18	+5 V supply input 2
V_{SS1}	19	ground 1 (0 V)
CVBS4	20	luminance respectively CVBS upper input data bits CVBS7 to CVBS4 (CVBS with luminance, chrominance and all sync information in two's complement format)
CVBS5	21	
CVBS6	22	
CVBS7	23	
GPSW1	24	Port 1 output for general purpose (programmable)
GPSW2	25	Port 2 output for general purpose (programmable)
HCL	26	black level clamp pulse (programmable), e.g. for TDA8708 (ADC)
LLC	27	line-locked clock input signal (29.5 MHz for 50 Hz system; 24.5454 MHz for 60 Hz system)
V_{DD3}	28	+5 V supply input 3
HSY	29	horizontal sync indicator output signal (programmable), e.g. for TDA8708 (ADC)
VS	30	vertical sync output signal
HS	31	horizontal sync output signal (programmable)
HL	32	horizontal lock flag, HIGH = PLL locked
XTAL	33	26.8 MHz clock output
XTALI	34	26.8 MHz connection for crystal or external oscillator (TTL compatible squarewave)

SYMBOL	PIN	DESCRIPTION
V_{SSA}	35	analog ground
LFCO	36	line frequency control output signal, multiple of horizontal frequency (7.375 MHz/6.136363 MHz)
V_{DDA}	37	+5 V supply input for analog part
V_{SS2}	38	ground 2 (0 V)
ODD	39	odd/even field identification output (odd = HIGH); active only at NFEN-bit = 1
SDA	40	I^2C-bus data line
SCL	41	I^2C-bus clock line
HREF	42	horizontal reference output for valid YUV data (for active line 768Y or 640Y samples long)
IICSA	43	set module address input (LOW = 1000 101X; HIGH = 1000 111X)
i.c.	44	internally connected
Y7	45	Y signal output bits Y7 to Y2 (luminance), part of the digital YUV-bus
Y6	46	
Y5	47	
Y4	48	
Y3	49	
Y2	50	
V_{SS3}	51	ground 3 (0 V)
V_{DD4}	52	+5 V supply input 4
Y1	53	Y signal output bits Y1 to Y0 (luminance), part of the digital YUV-bus
Y0	54	
UV7	55	UV signal output bits UV7 to UV0 (colour-difference), part of the digital YUV-bus
UV6	56	
UV5	57	
UV4	58	
UV3	59	
UV2	60	
UV1	61	
UV0	62	
FEON	63	output active flag (active LOW when Y and UV data in high-impedance state)
FEIN	64	fast enable input (active LOW to control fast switching due to YUV data)
GPSW0	65	Port 0 output for general purpose (programmable); active only at NFEN-bit = 1
PLIN	66	PAL flag (active LOW at inverted line); SECAM flag (LOW equals DR, HIGH equals DB line)
V_{SS4}	67	ground 4 (0 V)
RTCO	68	real-time control output active at NFEN-bit = 1; Fig.7

Digital multistandard colour decoder, square pixel (DMSD-SQP)

SAA7191B

PIN CONFIGURATION

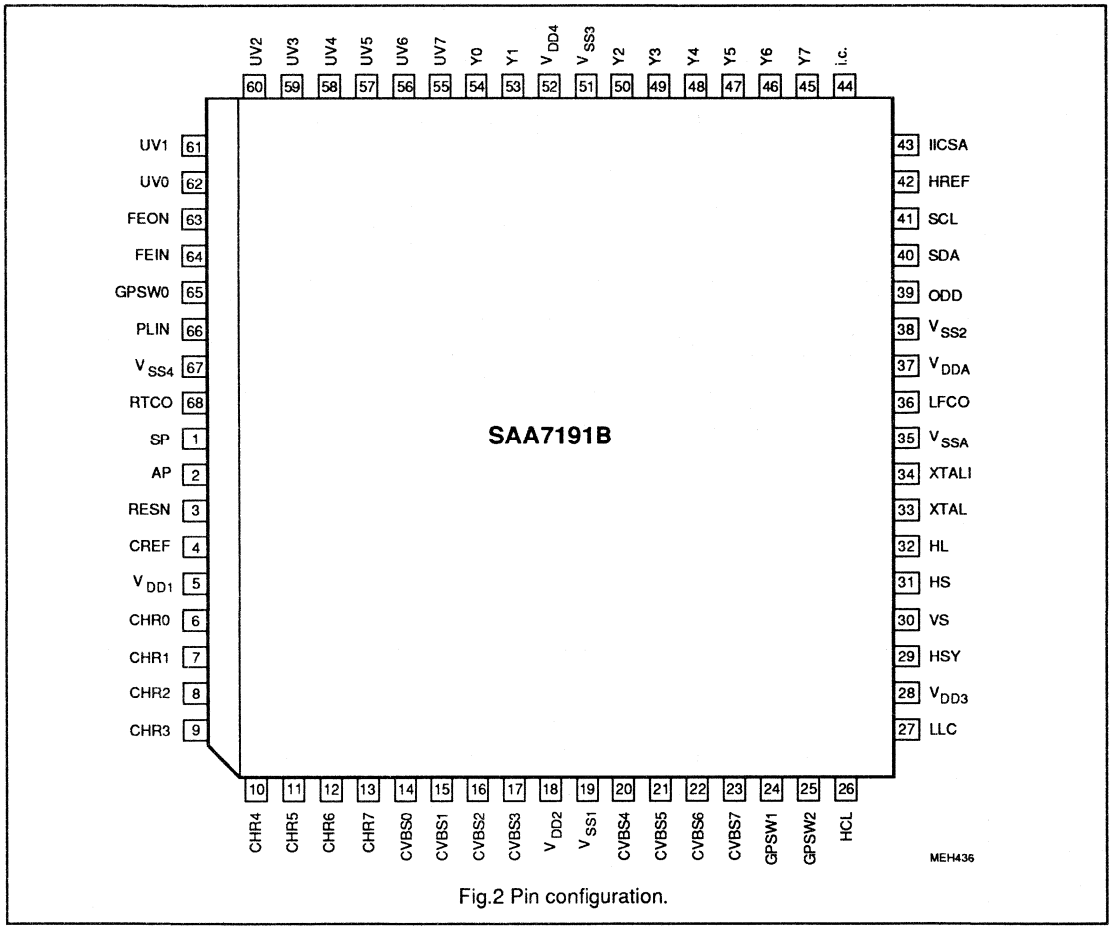


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Chrominance processor

The 8-bit chrominance input signal (CVBS or chrominance format). passes a bandpass filter to eliminate DC components and to decimate the sample rate before it is fed to the two multipliers (quadrature demodulator), Fig.3(a).
Two subcarrier signals from a local oscillator (0 and 90 degree) are fed to the multiplicator inputs of the multipliers. The multipliers operate as a quadrature demodulator for all PAL and NTSC signals; it operates as a frequency down-mixer for SECAM signals.
The two multiplier output signals are converted to a serial data stream and applied to three low-pass filter stages, then to a gain controlled amplifier. A final multiplexed low-pass filter achieves, together with the preceding stages, the required bandwidth performance.
The signals, originated from PAL and NTSC, are applied to a comb-filter.
The signals, originated from SECAM, are fed through a Cloche filter (0 Hz centre frequency), a phase demodulator and a differentiator to obtain frequency-demodulated colour-difference signals.
The SECAM signals are fed after de-emphasis to a cross-over switch, to provide the both serial-transmitted colour-difference signals. These signals are fed finally to the output formatter stages and to the output interface.

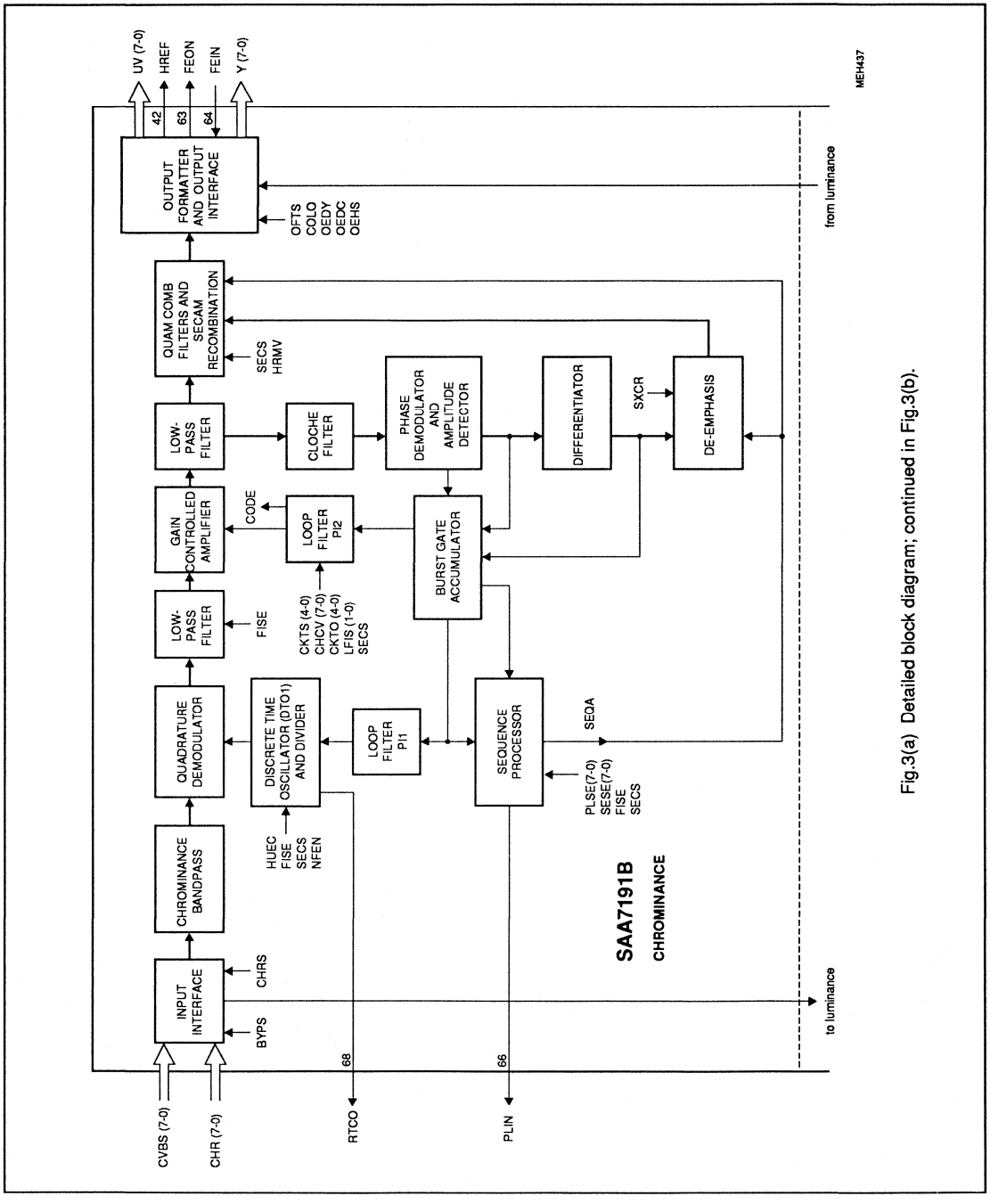


Fig.3(a) Detailed block diagram; continued in Fig.3(b).

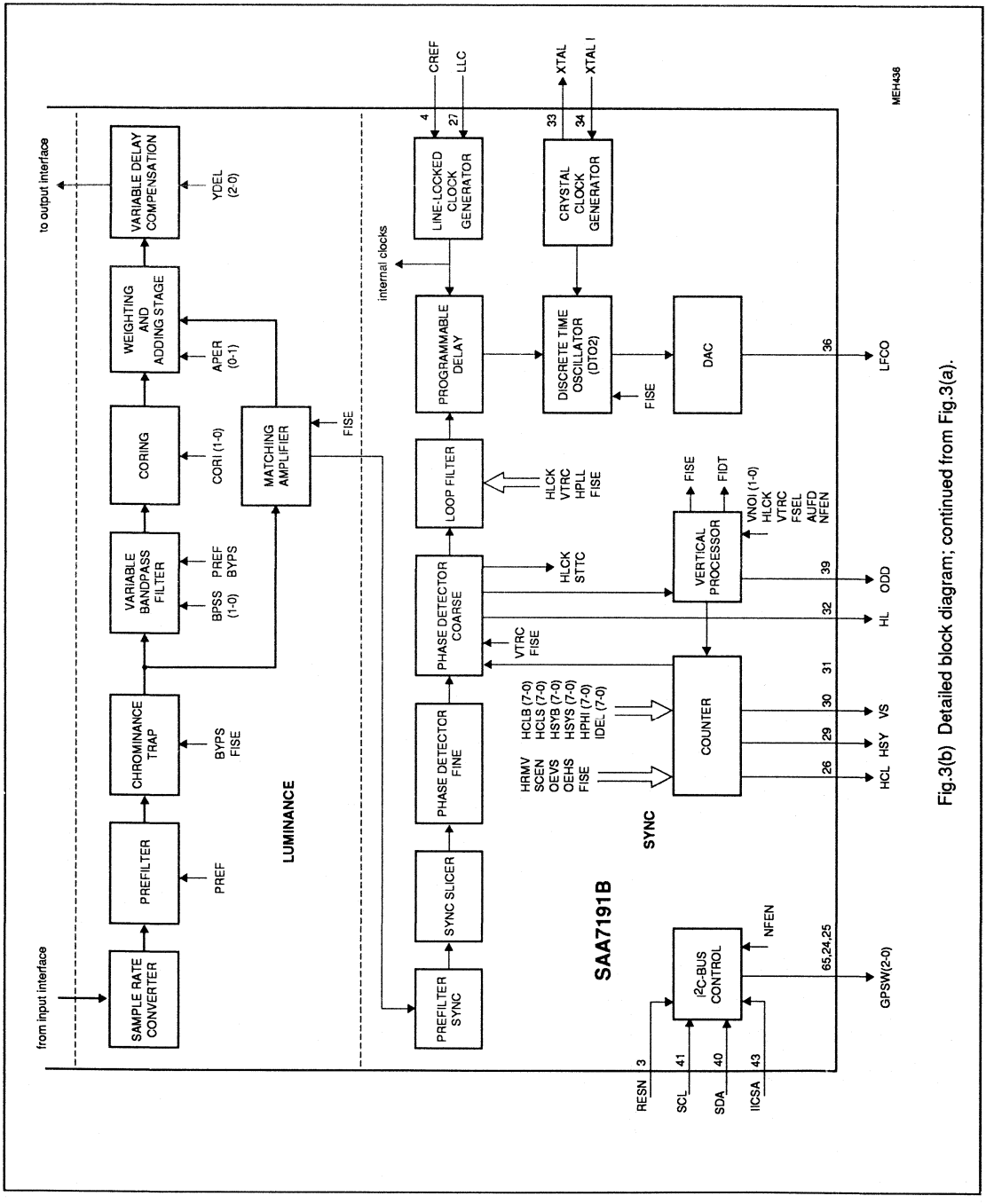


Fig.3(b) Detailed block diagram; continued from Fig.3(a).

Luminance processor

The luminance input signal, a digital CVBS format or an 8-bit luminance format (S-VHS, Hi8), is fed through a sample rate converter to reduce the data rate to 14.75 MHz for PAL and SECAM (12.2727 MHz for NTSC), Fig.3(b).

Sample rate is converted by means of a switchable pre-filter. High frequency components are emphasized to compensate for loss in the following chrominance trap filter. This chrominance trap filter (f_o = 4.43 MHz or f_o = 3.58 MHz centre frequency selectable) eliminates most of the colour carrier signal, therefore, it must be by-passed for S-Video (S-VHS and Hi8) signals.
The high frequency components of the luminance signal can be "peaked" (control for sharpness improvement via the I²C-bus) in two bandpass filters with selectable transfer characteristic.
A coring circuit with selectable characteristic improves the signal once more, this signal is then added to the original ("unpeaked") signal. A switchable amplifier achieves a common DC amplification, because the DC gains are different in both chrominance trap modes.

Processing delay stage

The improved luminance signal is fed to the variable delay compensation. The delay from input to output is 220 LLC cycles.The processing delay will be influenced in future enhancements.

Synchronization

The luminance output signal is fed to the synchronization stage. Its bandwidth is reduced to 1 MHz in a low-pass filter. The sync pulses are sliced and fed to the phase detectors to be compared with the sub-divided clock frequency.
The resulting output signal is applied to the loop filter to accumulate all phase deviations. Adjustable output signals (e. g. HCL and HSY) are generated according to peripheral requirements (TDA8708A, TDA8709A). The output signals HS, VS and PLIN are locked to the timing reference signal HREF (Figures 6 and 7).
There is no absolute timing reference guaranteed between the input signal and the HREF signal as further improvements to the circuit may change the total processing delay. It is therefore not recommended to use them for applications, which ask for absolute timing accuracy to the input signals.
The loop filter signal drives an oscillator to generate the line frequency control output signal LFCO.

Table 1 Clock frequencies in MHz for 50/60 Hz systems

CLOCK	50 Hz	60 Hz
LLC	29.5	24.545454
LLC2	14.75	12.272727
LLC4	7.375	6.136136
LLC8	3.6875	3.068181

Line locked clock frequency

LFCO is required in an external PLL (SAA7197) to generate the line locked clock frequency.

YUV-bus, digital outputs

The 16-bit YUV-bus transfers digital data from the output interfaces to a feature box, or to the digital-to-analog converter (DAC). Outputs are controlled via the I²C-bus in normal selections, or they are controlled by output enable chain (FEIN on pin 64, Fig.4).
The YUV-bus data rate equals LLC2 in Table 1. Timing is achieved by marking each second positive rising edge of the clock LLC in conjunction with CREF (clock reference).

YUV-bus formats 4:2:2 and 4:1:1

The output signals Y7 to Y0 are the bits of the digital luminance signal. The output signals UV7 to UV0 are the bits of the multiplexed colour-difference signals (B–Y) and (R–Y). The frame in the following tables is the time, required to transfer a full set of samples. In case of 4 : 2 : 2 format two luminance samples are transmitted in comparision to one U and one V sample within one frame.

Table 2 4 : 2 : 2 format (768 pixels per line for 50 Hz system; 640 pixels per line for 60 Hz system)

OUTPUT	PIXEL BYTE SEQUENCE					
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7(MSB)	U7	V7	U7	V7	U7	V7
Y frame	0	1	2	3	4	5
UV frame	0		2		4	

Notes to Table 2

1. Data rate: LLC2
2. Sample frequency:
   Y LLC2
   U LLC4
   V LLC4

The quoted frequencies are valid on the YUV-bus. The time frames are controlled by the HREF signal.

Table 3 4 : 1 : 1 format (768 pixels per line for 50 Hz system and 640 pixels per line for 60 Hz system)

OUTPUT	PIXEL BYTE SEQUENCE							
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	0	0	0	0	0	0	0	0
UV1	0	0	0	0	0	0	0	0
UV2	0	0	0	0	0	0	0	0
UV3	0	0	0	0	0	0	0	0
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7 (MSB)	U7	U5	U3	U1	U7	U5	U3	U1
Y frame	0	1	2	3	4	5	6	7
UV frame	0				4			

Fast enable is achieved by setting input FEIN to LOW. This signal is used to control fast switching on the digital YUV-bus. HIGH on this pin forces the Y and U/V outputs after 2 x LLC clock cycles to a high impedance state. The signal FEON is LOW when the Y and U/V outputs are in this high-impedance state.

FEIN and FEON provide a "daisy chain" structure for priority control of the YUV-bus (Figures 4 and 5).

Notes to Table 3

Data rate:		LLC2
sample frequency:	Y	LLC2
	U	LLC8
	V	LLC8

The quoted frequencies are valid on the YUV-bus. The time frames are controlled by the HREF signal.

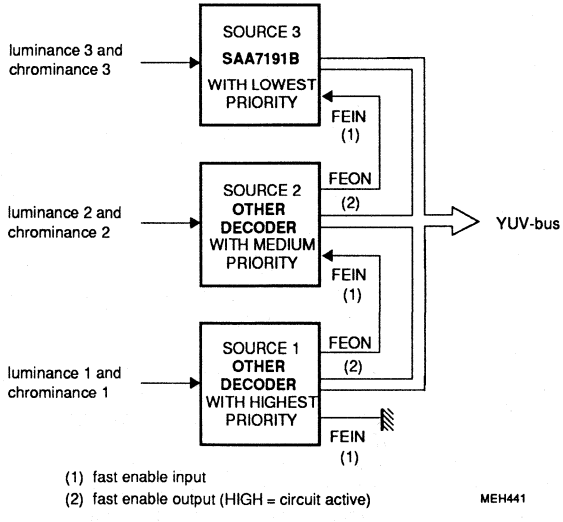
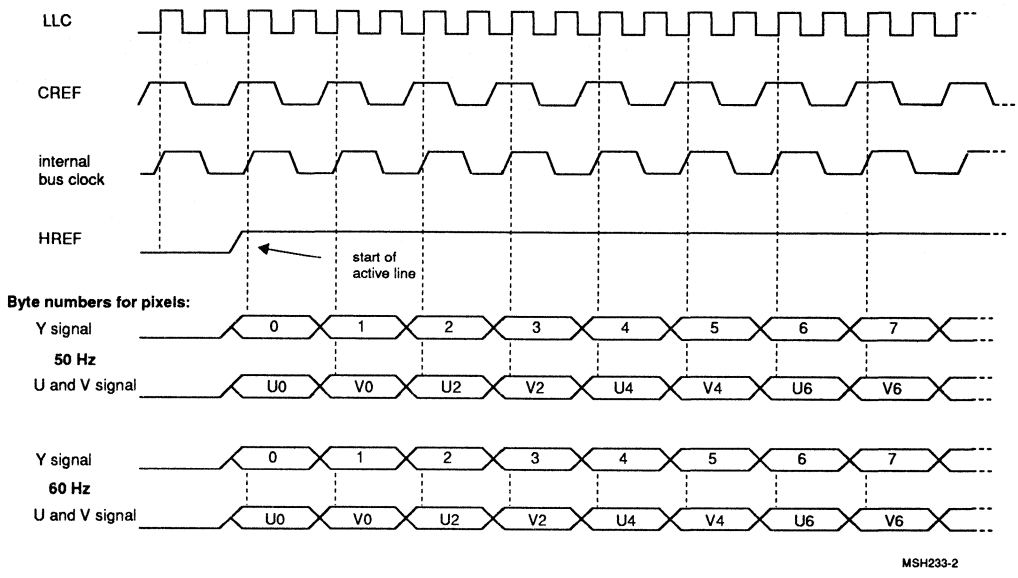


Fig.4 Fast output enable daisy chain.



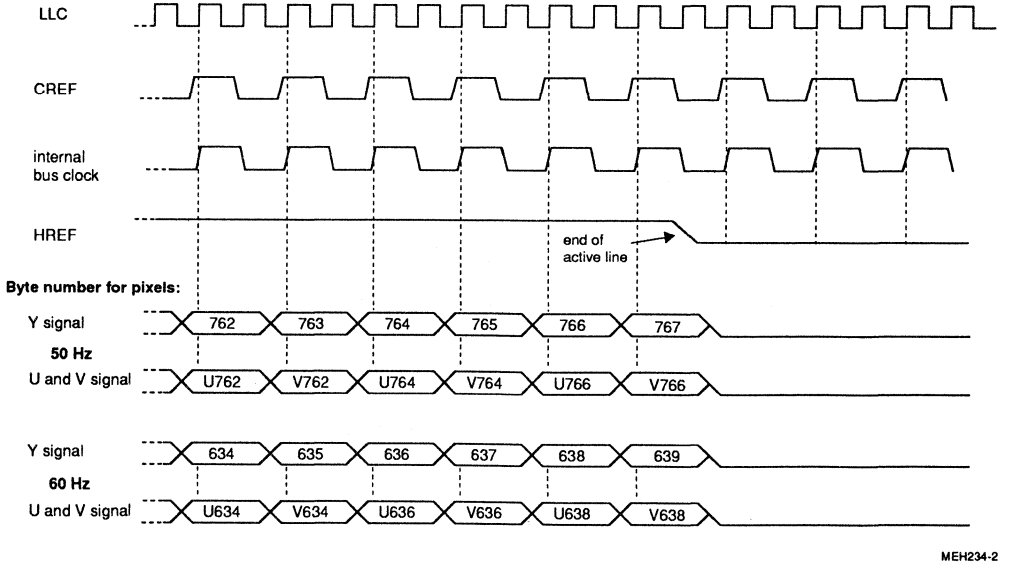


Fig.5 Line control by HREF in 4:2:2 format for 50 Hz and 60 Hz systems.

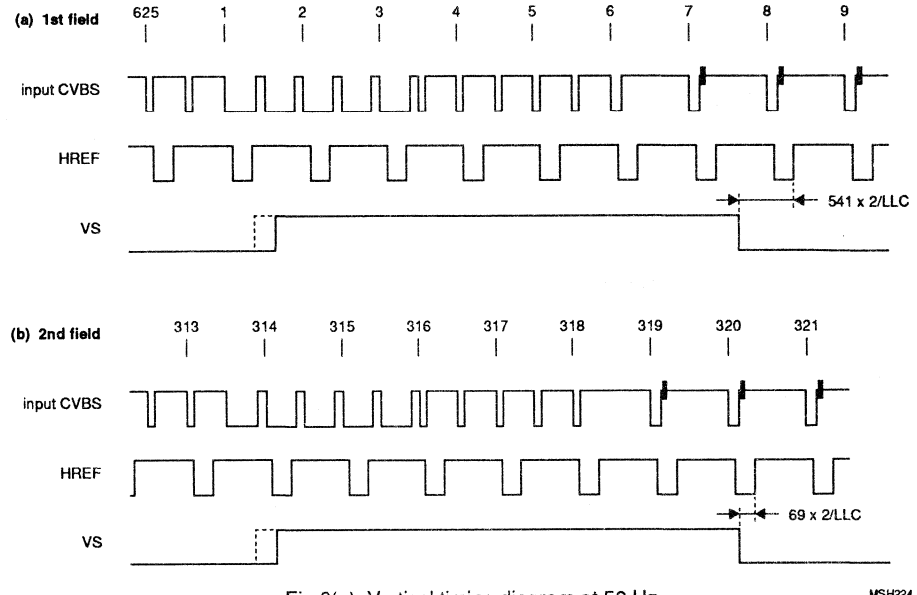


Fig.6(a) Vertical timing diagram at 50 Hz.

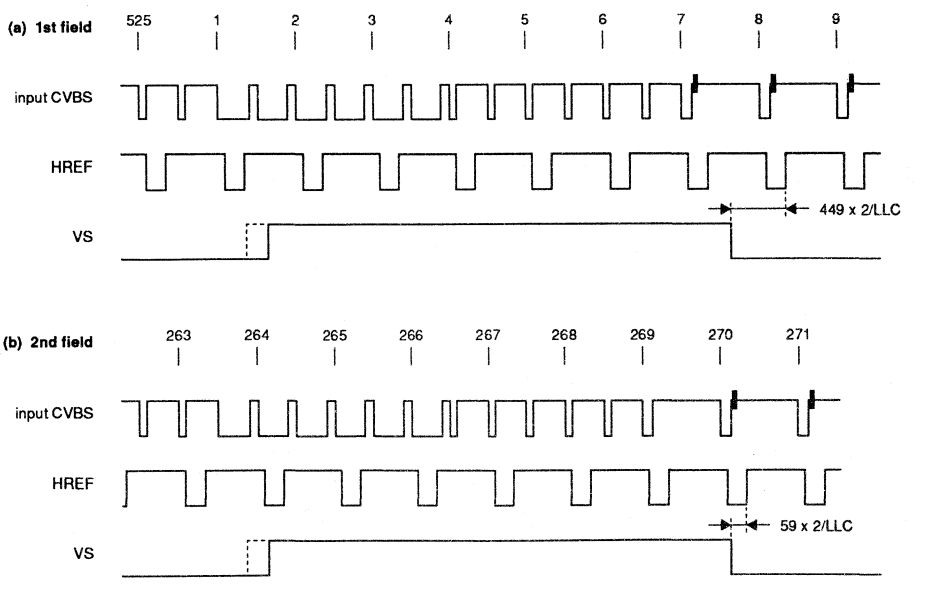


Fig.6(b) Vertical timing diagram at 60 Hz.

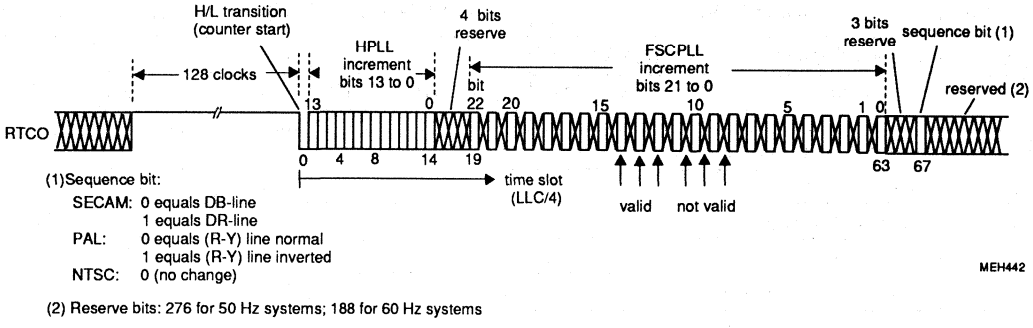


Fig.7 RTCO timing.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); ground pins 19, 35, 38, 51 and 67 as well as supply pins 5, 18, 28, 37 and 52 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pins 5, 18, 28, 37, 52)	−0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{SS\ A} - V_{SS\ (1\ to\ 4)}$	-	±100	mV
V_I	voltage on all inputs	−0.5	V_{DD}+0.5	V
V_O	voltage on all outputs ($I_{O\ max}$ = 20 mA)	−0.5	V_{DD}+0.5	V
P_{tot}	total power dissipation	-	2.5	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	±2000	-	V

* Equivalent to discharging a 100 pF capacitor through an 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range (pins 5, 18, 28, 37, 52)		4.5	5	5.5	V
I_{DD}	total supply current (pins 5, 18, 28, 37, 52)	V_{DD} = 5 V; inputs LOW; outputs not connected	-	100	250	mA
I²C-bus, SDA and SCL (pins 40 and 41)						
V_{IL}	input voltage LOW		−0.5	-	1.5	V
V_{IH}	input voltage HIGH		3	-	V_{DD}+0.5	V
$I_{40,41}$	input current		-	-	±10	μA
I_{ACK}	output current on pin 40	acknowledge	3	-	-	mA
V_{OL}	output voltage at acknowledge	I_{40} = 3 mA	-	-	0.4	V
Signal and control inputs (pins 3, 4, 6 to 17, 20 to 23, 27, 43 and 64), Fig.10						
V_{IL}	LLC input voltage LOW (pin 27)		−0.5	-	0.6	V
V_{IH}	LLC input voltage HIGH		2.4	-	V_{DD}+0.5	V
V_{IL}	other input voltage LOW		−0.5	-	0.8	V
V_{IH}	other input voltage HIGH		2.0	-	V_{DD}+0.5	V
I_{LI}	input leakage current		-	-	10	μA
C_I	input capacitance	data inputs; note 1	-	-	8	pF
		I/O high-ohmic	-	-	8	pF
		clock inputs	-	-	10	pF
$t_{SU.DAT}$	input data set-up time	Fig.8	11	-	-	ns
$t_{HD.DAT}$	input data hold time		3	-	-	ns
LFCO output (pin 36)						
V_o	output signal (peak-to-peak value)	note 2	1.4	-	2.6	V
YUV-bus outputs (pins 45 to 50 and pins 53 to 62)		Figures 11 and 15 to 25				
V_{OL}	output voltage LOW	notes 1 and 2	0	-	0.6	V
V_{OH}	output voltage HIGH		2.4	-	V_{DD}	V
C_L	load capacitance (HREF included)		15	-	50	pF
Control outputs (pins 24 to 26, 29 to 32, 39, 42 ,63, 65,66 and 68); Fig.12						
V_{OL}	output voltage LOW	notes 1 and 2	0	-	0.6	V
V_{OH}	output voltage HIGH		2.4	-	V_{DD}	V
C_L	load capacitance (HREF excluded)		7.5	-	25	pF
t_{SZ}	data output disable transition time	to 3-state condition	16	-	-	ns
t_{ZS}	data output enable transition time	from 3-state condition	14	-	-	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing of YUV-bus and control outputs		Fig.7				
t_{OH}	output signal hold time for	YUV, HREF, VS; C_L = 15 pF	13	-	-	ns
t_{OS}	output set-up time	others; C_L = 50 pF	14	-	-	ns
t_{SZ}	data output disable transition time	to 3-state condition	16	-	-	ns
t_{ZS}	data output enable transition time	from 3-state condition	14	-	-	ns
t_{RTCO}	RTCO timing			Fig.7		
Chrominance PLL						
f_C	catching range		±400	-	-	Hz
Crystal oscillator		Fig.9				
f_n	nominal frequency	3rd harmonic	-	26.8	-	MHz
$\Delta f / f_n$	permissible deviation f_n		-	-	±50	10^{-6}
	temperature deviation from f_n		-	-	±20	10^{-6}
X1	crystal specification:					
	temperature range T_{amb}		0	-	70	°C
	load capacitance C_L		8	-	-	pF
	series resonance resistance R_S		-	-	50	Ω
	motional capacitance C_1		-	1.1±20%	-	fF
	parallel capacitance C_0		-	3.5±20%	-	pF
	Philips catalogue number		9922 520 30004			
Line locked clock input LLC (pin 27)		Fig.8				
t_{LLC}	cycle time	note 3	31	-	45	ns
t_p	duty factor	t_{LLCH} / t_{LLC}	40	-	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns

Notes to the characteristics

1. Data output signals are Y7 to Y0 and UV7 to UV0. All others are control output signals.
2. Levels are measured with load circuit. YUV-bus outputs with 1.2 kΩ in parallel to 25 pF at 3 V (TTL load); LFCO output with 10 kΩ in parallel to 15 pF and other outputs with 1.2 kΩ in parallel to 25 pF at 3 V (TTL load).
3. t_{SU}, t_{HD}, t_{OH} and t_{OD} include t_r and t_f.

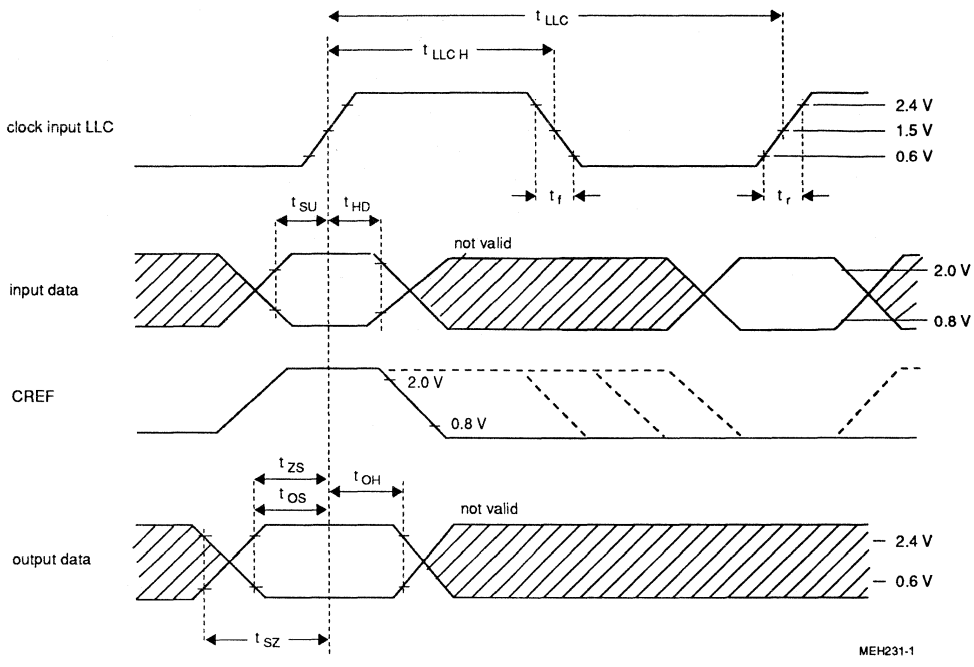


Fig.8 Data input and output timing diagram.

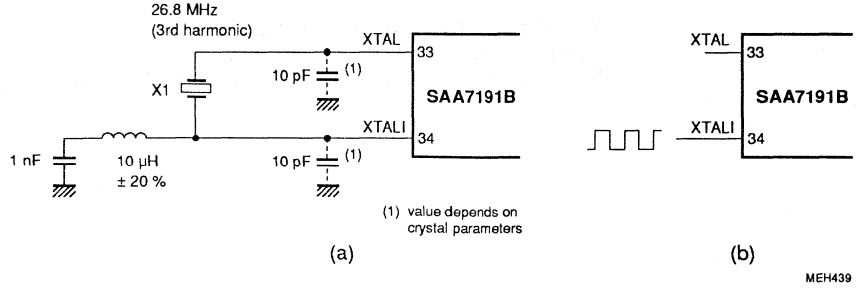
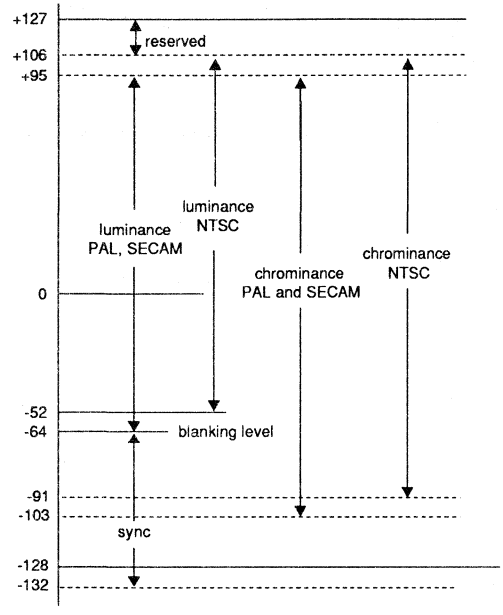
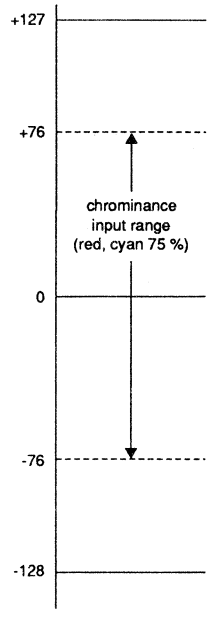


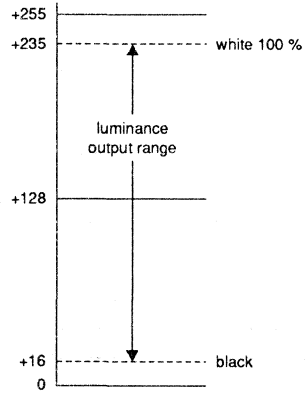
Fig.9 Oscillator application (a) and optional clock from external source (b).



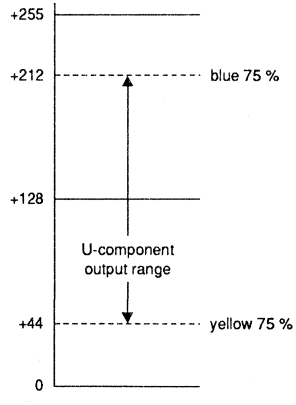
(a) CVBS7 to CVBS0 input signal range.



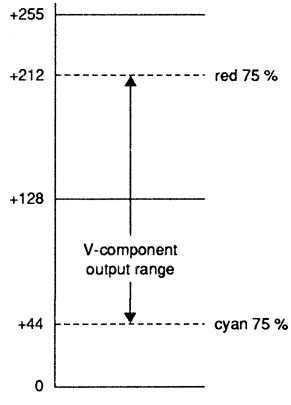
(b) CHR7 to CHR0 input signal range.



(c) Y output signal range.



(d) U output signal range (B-Y).



(e) V output signal range (R-Y).

Notes: 1. All levels are related to EBU colour bar.
2. Values in decimal at 100 % luminance and 75 % chrominance amplitude.

MSH254-1

Fig.10 Input and output signal ranges.

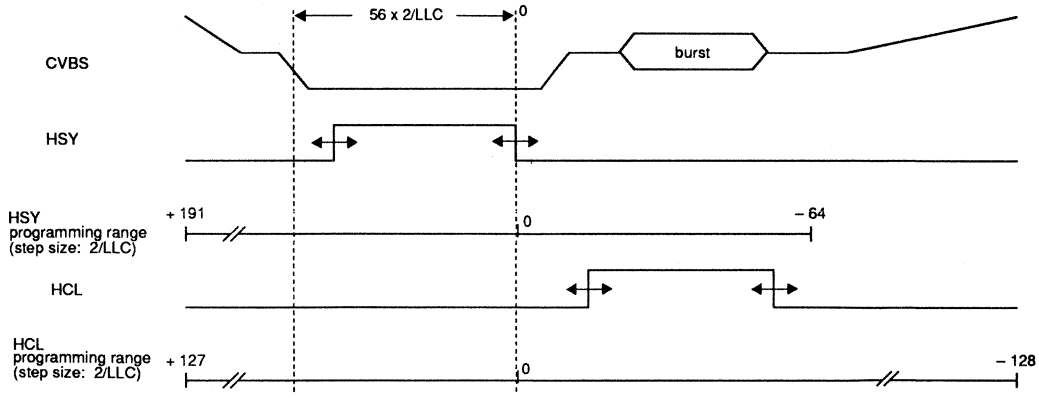


Fig.11 Horizontal sync indication HSY and clamping HCL.

MSH226-1

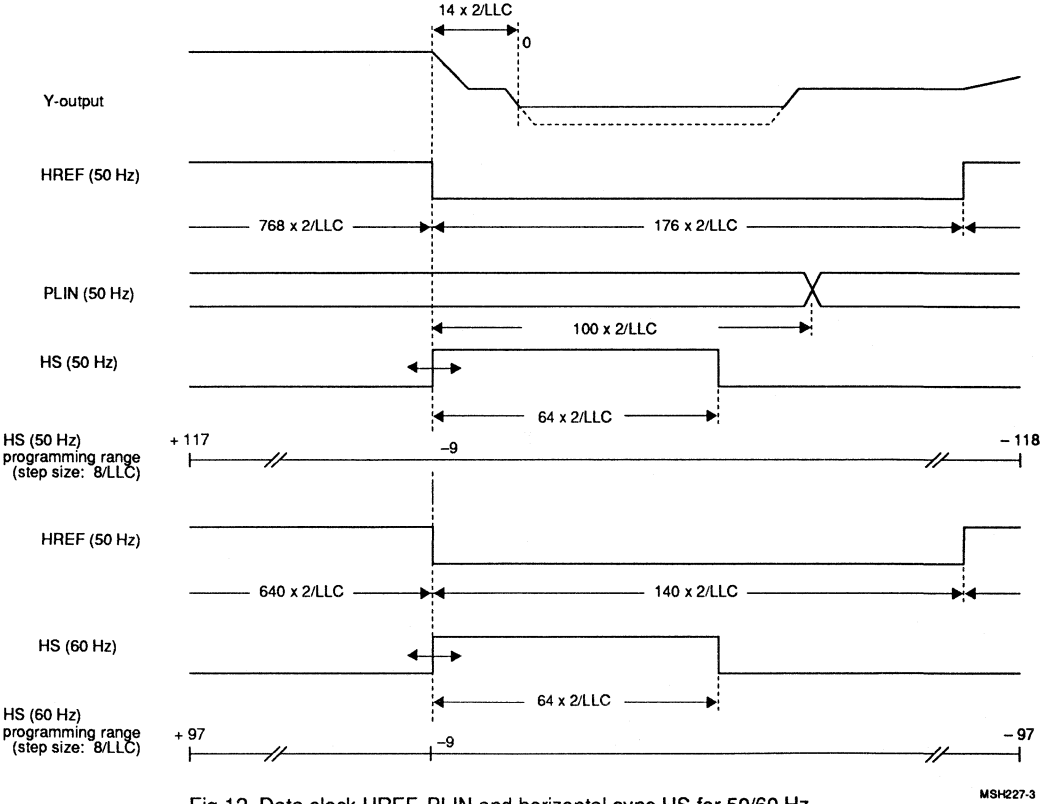


Fig.12 Data clock HREF, PLIN and horizontal sync HS for 50/60 Hz.

MSH227-3

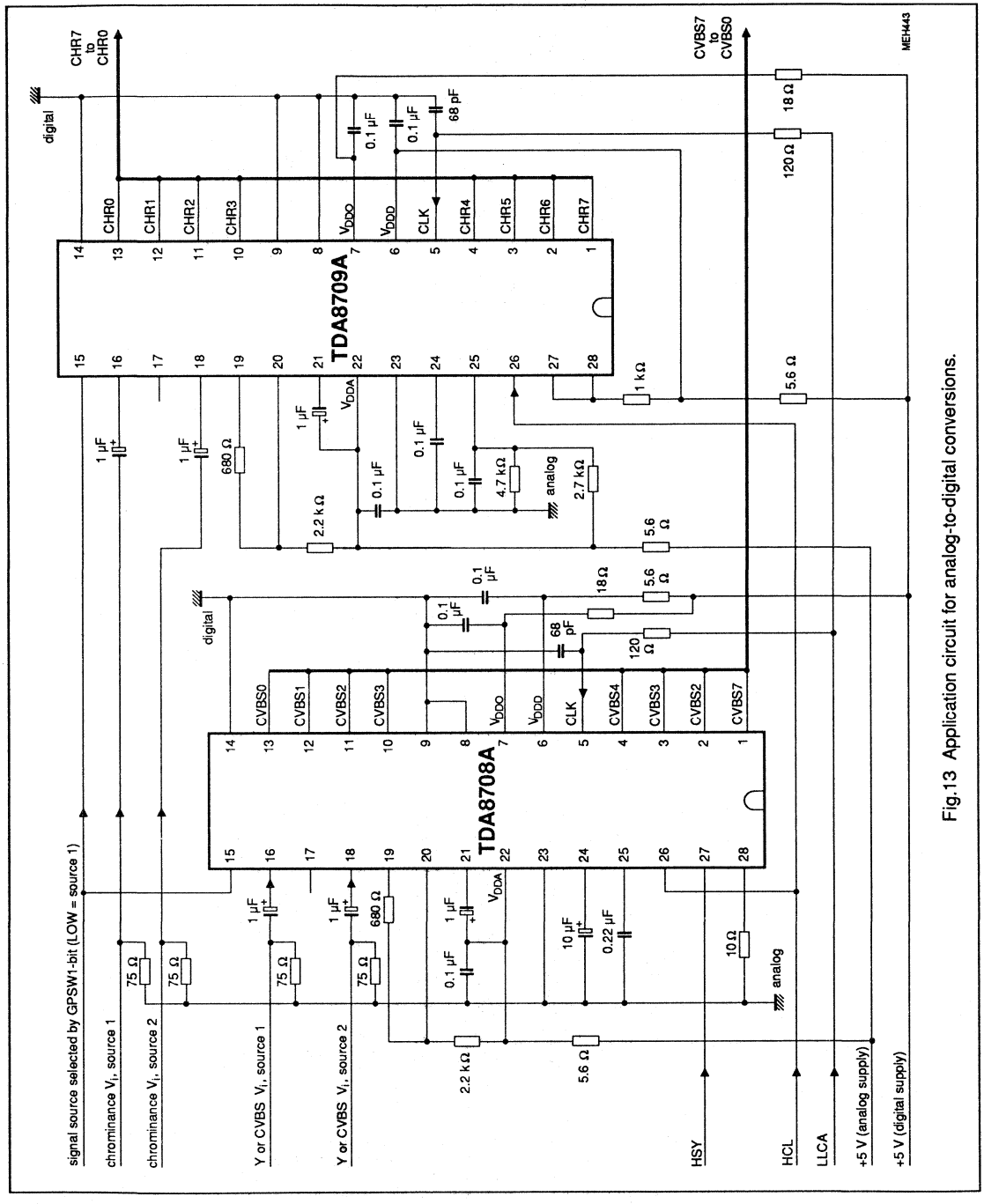


Fig.13 Application circuit for analog-to-digital conversions.

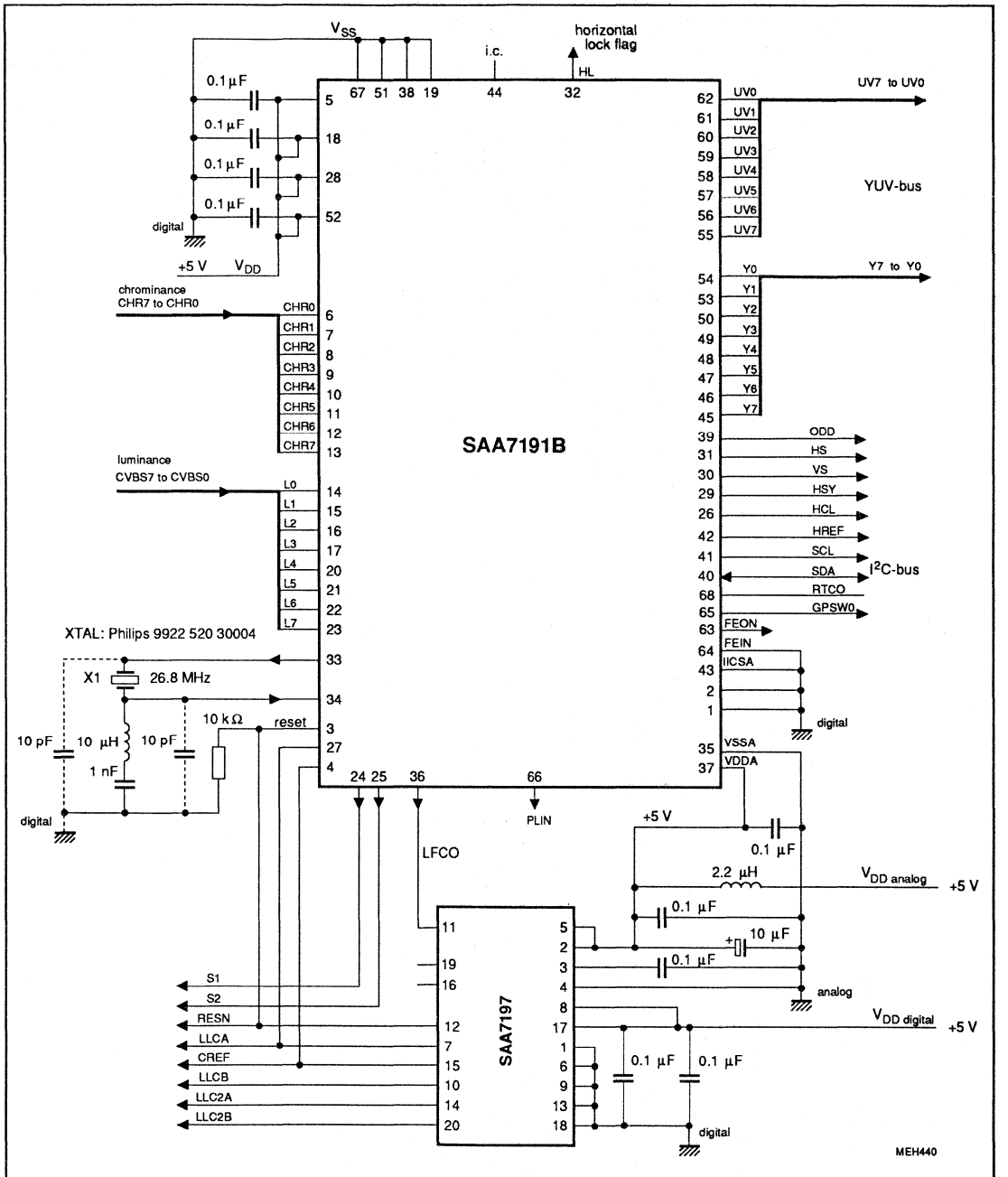


Fig.14 Application circuit for digital multistandard colour decoder.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A		DATAn	A	P

S = start condition
SLAVE ADDRESS = **1000 101X** (IICSA = LOW) **or 1000 111X** (IICSA = HIGH)
A = acknowledge, generated by the slave
SUBADDRESS* = subaddress byte (Table 4)
DATA = data byte (Table 4)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 4 I²C-bus; DATA for status byte (X = 1 in address byte).

FUNCTION		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
status byte		STTC	HLCK	FIDT	X	X	X	X	CODE

Function of the bits:

STTC — Horizontal time constant information: 0 = TV time constant (slow); 1 = VCR time constant (fast)
HLCK — Horizontal PLL information: 0 = HPLL locked; 1 = HPLL unlocked
FIDT — Field information: 0 = 50 Hz system detected; 1 = 60 Hz system detected
CODE — Colour information: 0 = no colour detected; 1 = colour detected

X — for future enhancements, do not evaluate

Table 5 I²C-bus; subaddress and data bytes for writing (X = 0 in address byte).

FUNCTION	SUBADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Increment delay	00	IDEL7	IDEL6	IDEL5	IDEL4	IDEL3	IDEL2	IDEL1	IDEL0
H sync begin, 50 Hz	01	HSYB7	HSYB6	HSYB5	HSYB4	HSYB3	HSYB2	HSYB1	HSYB0
H sync stop, 50 Hz	02	HSYS7	HSYS6	HSYS5	HSYS4	HSYS3	HSYS2	HSYS1	HSYS0
H clamp begin, 50 Hz	03	HCLB7	HCLB6	HCLB5	HCLB4	HCLB3	HCLB2	HCLB1	HCLB0
H clamp stop, 50 Hz	04	HCLS7	HCLS6	HCLS5	HCLS4	HCLS3	HCLS2	HCLS1	HCLS0
H sync after PHI1, 50 Hz	05	HPHI7	HPHI6	HPHI5	HPHI4	HPHI3	HPHI2	HPHI1	HPHI0
Luminance control	06	BYPS	PREF	BPSS1	BPSS0	CORI1	CORI0	APER1	APER0
Hue control	07	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
Colour killer threshold QAM	08	CKTQ4	CKTQ3	CKTQ2	CKTQ1	CKTQ0	0	0	0
Colour-killer threshold SECAM	09	CKTS4	CKTS3	CKTS2	CKTS1	CKTS0	0	0	0
PAL switch sensitivity	0A	PLSE7	PLSE6	PLSE5	PLSE4	PLSE3	PLSE2	PLSE1	PLSE0
SECAM switch sensitivity	0B	SESE7	SESE6	SESE5	SESE4	SESE3	SESE2	SESE1	SESE0
Gain control	0C	COLO	LFIS1	LFIS0	0	0	0	0	0
Standard/mode control	0D	VTRC	0	0	0	NFEN	HRMV	GPSW0	SECS
I/O and clock control	0E	HPLL	OEDC	OEHS	OEVS	OEDY	CHRS	GPSW2	GPSW1
Control #3	0F	AUFD	FSEL	SXCR	SCEN	OFTS	YDEL2	YDEL1	YDEL0
Control #4	10	0	0	0	0	0	HRFS	VNOI1	VNOI0
Colour control	11	CHCV7	CHCV6	CHCV5	CHCV4	CHCV3	CHCV2	CHCV1	CHCV0
Not used, is acknowledged	12	0	0	0	0	0	0	0	0
Not used, is acknowledged	13	0	0	0	0	0	0	0	0
H sync begin, 60 Hz	14	HS6B7	HS6B6	HS6B5	HS6B4	HS6B3	HS6B2	HS6B1	HS6B0
H sync stop, 60 Hz	15	HS6S7	HS6S6	HS6S5	HS6S4	HS6S3	HS6S2	HS6S1	HS6S0
H clamp begin, 60 Hz	16	HC6B7	HC6B6	HC6B5	HC6B4	HC6B3	HC6B2	HC6B1	HC6B0
H clamp stop, 60 Hz	17	HC6S7	HC6S6	HC6S5	HC6S4	HC6S3	HC6S2	HC6S1	HC6S0
H sync after PHI1, 60 Hz	18	HP6I7	HP6I6	HP6I5	HP6I4	HP6I3	HP6I2	HP6I1	HP6I0

Note to Table 5
- Default values of register contents to obtain a picture see Table 6.
- All unused control bits must be programmed with "0" (zero) as indicated in Table 5.

Function of the bits of Table 5

<table>
<tr><td>IDEL7 to IDEL0
"00"</td><td>Increment delay time (dependent on application), step size = 4 / LLC. The delay time is selectable from –4 / LLC (–1 decimal multiplier) to –1024 / LLC (–256 decimal multiplier) equals data FF to 00 (hex). Different processing times in the chrominance channel and the clock generation could result in phase errors in the chrominance processing by transients in clock frequency. An adjustable delay (IDEL) is necessary if the processing time in the clock generation is unknown.</td></tr>
<tr><td>HSYB7 to HSYB0
"01"</td><td>Horizontal sync begin for 50 Hz, step size = 2 / LLC. The delay time is selectable from +382/LLC (+191 decimal multiplier) to –128/LLC (–64 decimal multiplier) equals data BF to C0 (hex). Two's complement numbers with "hidden" sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB–1 bits.</td></tr>
<tr><td>HSYS7 to HSYS0
"02"</td><td>Horizontal sync stop for 50 Hz, step size = 2 / LLC. The delay time is selectable from +382/LLC (+191 decimal multiplier) to –128/LLC (–64 decimal multiplier) equals data BF to C0 (hex). Two's complement numbers with "hidden" sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB–1 bits.</td></tr>
<tr><td>HCLB7 to HCLB0
"03"</td><td>Horizontal clamp start for 50 Hz, step size = 2 / LLC. The delay time is selectable from +254/LLC (+127 decimal multiplier) to –256/LLC (–128 decimal multiplier) equals data 7F to 80 (hex).</td></tr>
<tr><td>HCLS7 to HCLS0
"04"</td><td>Horizontal clamp stop for 50 Hz, step size = 2 / LLC. The delay time is selectable from +254/LLC (+127 decimal multiplier) to –256/LLC (–128 decimal multiplier) equals data 7F to 80 (hex).</td></tr>
<tr><td>HPHI7 to HPHI0
"05"</td><td>Horizontal sync after PHI1 for 50 Hz, step size = 8 / LLC. The delay time is selectable from +936 /LLC (+117 decimal multiplier) to –944 /LLC (–118 decimal multiplier) equals data 7F to 80 (hex).</td></tr>
<tr><td>BYPS
"06"</td><td>input mode select bit: 0 = CVBS mode (chrominance trap active)
1 = S-Video mode (chrominance trap bypassed)</td></tr>
<tr><td>PREF</td><td>use of pre-filter: 0 = pre-filter off; 1 = pre-filter on;
PREF may be used if chrominance trap is active.</td></tr>
<tr><td>BPSS1 to BPSS0</td><td>Aperture bandpass to select different characteristics with maximums (0.2 to 0.3 x LLC / 2):
<table>
<tr><th>BPSS1</th><th>BPSS0</th><th>characteristics</th></tr>
<tr><td>0</td><td>0</td><td rowspan="4">Figures 16 to 25</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>CORI1 to CORI0
"06"</td><td>Coring range for high frequency components according to 8-bit luminance, Fig.15.
<table>
<tr><th>CORI1</th><th>CORI0</th><th>coring</th></tr>
<tr><td>0</td><td>0</td><td>coring off</td></tr>
<tr><td>0</td><td>1</td><td>±1 LSB</td></tr>
<tr><td>1</td><td>0</td><td>±2 LSB</td></tr>
<tr><td>1</td><td>1</td><td>±3 LSB</td></tr>
</table></td></tr>
</table>

<table>
<tr><td>APER1 to APER0
"06"</td><td>Aperture bandpass filter weights high frequency components of luminance signal:
<table><tr><th>APER1</th><th>APER0</th><th>factor</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0.25</td></tr><tr><td>1</td><td>0</td><td>0.5</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table></td></tr>
<tr><td>HUE7 to HUE0
"07"</td><td>Hue control from +178.6° to −180.0°, equals data bytes 7F to 80 (hex); 0° equals 00.</td></tr>
<tr><td>CKTQ4 to CKTQ0
"08"</td><td>Colour-killer threshold QAM from approximately −30 dB to −18 dB, equals data bytes F8 to 07 (hex); −24 dB equals 87</td></tr>
<tr><td>CKTS4 to CKTS0
"09"</td><td>Colour-killer threshold SECAM from approximately −30 dB to −18 dB, equals data bytes. F8 to 07 (hex); −24 dB equals 87</td></tr>
<tr><td>PLSE7 to PLSE0
"0A"</td><td>PAL switch sensitivity from LOW-to-HIGH (HIGH means immediate sequence correction), equals FF to 00 (hex), MEDIUM equals 80.</td></tr>
<tr><td>SESE7 to SESE0
"0B"</td><td>SECAM switch sensitivity from LOW-to-HIGH (HIGH means immediate sequence correction), equals FF to 00 (hex), MEDIUM equals 80.</td></tr>
<tr><td>COLO
"0C"</td><td>Colour on bit: 0 = on, dependent on colour-killer; 1 = forced colour on.</td></tr>
<tr><td>LFIS1 to LFIS0
"0C"</td><td>Gain control (AGC filter):
<table><tr><th>LFIS1</th><th>LFIS0</th><th></th><th>loop filter time constant</th></tr><tr><td>0</td><td>0</td><td>=</td><td>slow</td></tr><tr><td>0</td><td>1</td><td>=</td><td>medium</td></tr><tr><td>1</td><td>0</td><td>=</td><td>fast</td></tr><tr><td>1</td><td>1</td><td>=</td><td>actual gain, stored</td></tr></table></td></tr>
<tr><td>VTRC
"0D"</td><td>VTR/TV mode bit : 0 = TV mode; 1 = VTR mode.</td></tr>
<tr><td>NFEN</td><td>SAA7191B-specified functions enable (RTCO, ODD and GPSW0 outputs)
0 = outputs set to high-impedance (circuit equals SAA7191); 1 = outputs active</td></tr>
<tr><td>HRMV</td><td>HREF generation: 0 = like SAA7191; 1 = HREF is 8 x LLC2 clocks earlier</td></tr>
<tr><td>GPSWO</td><td>General purpose switch 0: 0 = output pin 65 LOW; 1 = output pin 65 HIGH</td></tr>
<tr><td>SECS</td><td>SECAM mode bit : 0 = other standards; 1 = SECAM</td></tr>
<tr><td>HPLL
"0E"</td><td>Horizontal clock PLL: 0 = PLL closed; 1 = PLL circuit open and horizontal frequency fixed.</td></tr>
<tr><td>OEDC</td><td>Colour-difference output enable: 0 = data outputs UV7 to UV0 high-impedance
1 = data outputs UV7 to UV0 active.</td></tr>
<tr><td>OEHS</td><td>H-sync output enable (pins 31 and 42): 0 = HS and HREF outputs high-impedance
1 = HS and HREF outputs active.</td></tr>
<tr><td>OEVS</td><td>V-sync output enable (pin 30): 0 = VS output high-impedance
1 = VS output active.</td></tr>
</table>

<table>
<tr><td>OEDY</td><td>Luminance output enable: 0 = data outputs Y7 to Y0 high-impedance
1 = data outputs Y7 to Y0 active.</td></tr>
<tr><td>CHRS</td><td>S-VHS bit (chrominance from CVBS or from chrominance input):
0 = controlled by BYPS-bit (subaddress 06)
1 = chrominance from chrominance input (CHR7 to CHR0)</td></tr>
<tr><td>GPSW2 to GPSW1
to "0E"</td><td>General purpose switches (port outputs dependent on application):
<table>
<tr><th>GPSW2</th><th>GPSW1</th><th>set port output pins 24 (GPSW2) and 25 (GPSW1)</th></tr>
<tr><td>0</td><td>0</td><td rowspan="4">use is dependent on application</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>AUFD
"0F"</td><td>Automatic field detection: 0 = field selection by microcomputer (FSEL-bit);
1 = automatic field detection by SAA7191.</td></tr>
<tr><td>FSEL</td><td>Field select (AUFD-bit = 0): 0 = 50 Hz (625 lines);
1 = 60 Hz (525 lines)</td></tr>
<tr><td>SXCR</td><td>SECAM cross-colour reduction: 0 = reduction off;
1 = reduction on.</td></tr>
<tr><td>SCEN</td><td>Sync enable, clamping pulse: 0 = HCL and HSY outputs HIGH (pins 26 and 29);
1 = HCL and HSY outputs active</td></tr>
<tr><td>OFTS</td><td>Select output format: 0 = 4 : 1 : 1 format;
1 = 4 : 2 : 2 format.</td></tr>
<tr><td>YDEL2 to YDEL0</td><td>Luminance delay compensation:
<table>
<tr><th>YDEL2</th><th>YDEL1</th><th>YDEL0</th><th>figure</th><th></th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0 x 2 / LLC</td><td rowspan="8">step size = 2 / LLC =
67.8 ns for 50 Hz
81.5 ns for 60 Hz</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>+1 x 2 / LLC</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>+2 x 2 / LLC</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>+3 x 2 / LLC</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>–4 x 2 / LLC</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>–3 x 2 / LLC</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>–2 x 2 / LLC</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>–1 x 2 / LLC</td></tr>
</table></td></tr>
<tr><td>HRFS
"10"</td><td>Select HREF: 0 = normal; 1 = for RGB input signal</td></tr>
<tr><td>VNOI1 to VNOI0</td><td>Vertical noise reduction
<table>
<tr><th>VNOI1</th><th>VNOI0</th><th>mode</th></tr>
<tr><td>0</td><td>0</td><td>normal</td></tr>
<tr><td>0</td><td>1</td><td>searching window</td></tr>
<tr><td>1</td><td>0</td><td>auto-deflection</td></tr>
<tr><td>1</td><td>1</td><td>vertical noise reduction bypassed</td></tr>
</table></td></tr>
</table>

<table>
<tr><td>CHCV7 to CHCV0
UV "11"</td><td>Chrominance gain control (nominal values) for QAM-modulated input signals, effects output amplitude (SECAM with fixed gain):
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>gain</th></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>maximum gain</td></tr>
<tr><td></td><td>:</td><td></td><td></td><td></td><td>:</td><td></td><td></td><td>to)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>CCIR level for PAL)) default programmed</td></tr>
<tr><td></td><td>:</td><td></td><td></td><td></td><td>:</td><td></td><td></td><td>to) values dependend</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>CCIR level for NTSC)) on application</td></tr>
<tr><td></td><td>:</td><td></td><td></td><td></td><td>:</td><td></td><td></td><td>to)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>minimum gain</td></tr>
</table></td></tr>
<tr><td>HS6B7 to HS6B0
"14"</td><td>Horizontal sync begin for 60 Hz, step size = 2 / LLC. The delay time is selectable from +382/LLC (+191 decimal multiplier) to −128/LLC (−64 decimal multiplier) equals data BF to C0 (hex). Two's complement numbers with "hidden" sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB−1 bits.</td></tr>
<tr><td>HS6S7 to HS6S0
"15"</td><td>Horizontal sync stop for 60 Hz, step size = 2 / LLC. The delay time is selectable from +382/LLC (+191 decimal multiplier) to −128/LLC (−64 decimal multiplier) equals data BF to C0 (hex). Two's complement numbers with "hidden" sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB−1 bits.</td></tr>
<tr><td>HC6B7 to HC6B0
"16"</td><td>Horizontal clamp begin for 60 Hz, step size = 2 / LLC. The delay time is selectable from +254/LLC (+127 decimal multiplier) to −256/LLC (−128 decimal multiplier) equals data 7F to 80 (hex).</td></tr>
<tr><td>HC6S7 to HC6S0
"17"</td><td>Horizontal clamp stop for 60 Hz, step size = 2 / LLC. The delay time is selectable from +254/LLC (+127 decimal multiplier) to −256/LLC (−128 decimal multiplier) equals data 7F to 80 (hex).</td></tr>
<tr><td>HP6I7 to HP6I0
"18"</td><td>Horizontal sync after PHI1 for 60 Hz, step size = 8 / LLC. The delay time is selectable from +776 /LLC (+97 decimal multiplier) to −776 /LLC (−97 decimal multiplier) equals data 7F to 80 (hex).</td></tr>
</table>

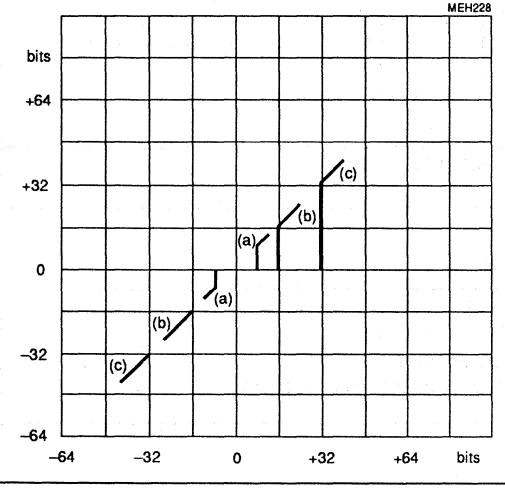


Fig.15 Coring function adjustment by subaddress 06 to affect the bandfilter output signal. The thresholds are related to the 13-bit word width in the luminance processing part and influence the 1LSB to 3LSB (Y0 to Y2) with respect to the 8-bit luminance output

(a) CORI1 = 0; CORI0 = 1

(b) CORI1 = 1; CORI0 = 0

(a) CORI1 = 1; CORI0 = 1

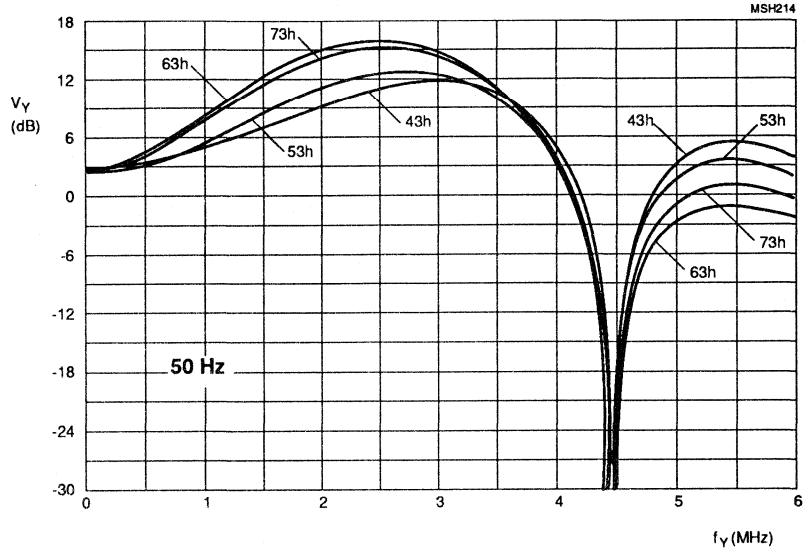


Fig.16 Luminance control in 50 Hz / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; maximum aperture bandpass filter characteristic.

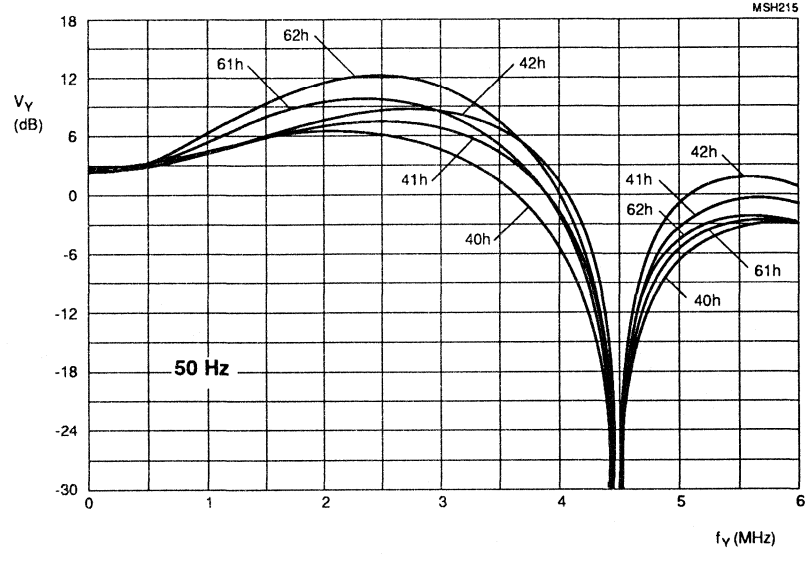


Fig.17 Luminance control in 50 Hz / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; other aperture bandpass filter characteristics.

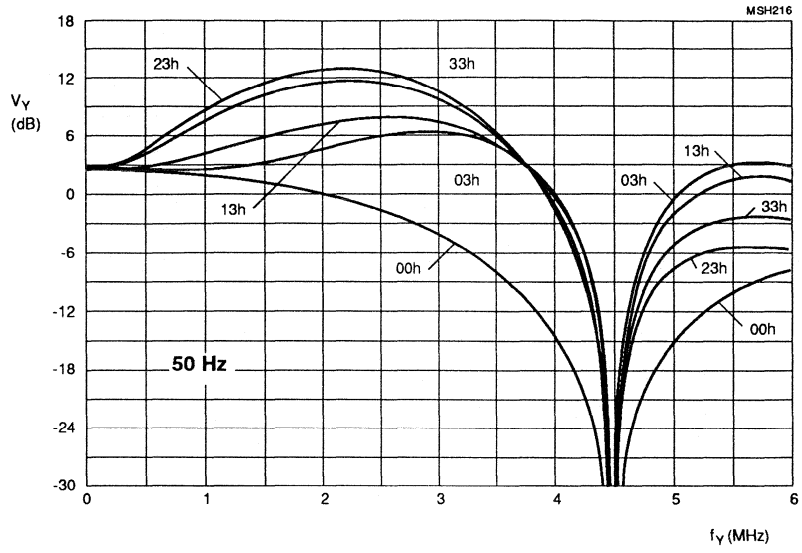


Fig.18 Luminance control in 50 Hz / CVBS mode controllable by subaddress byte 06; pre-filter off and coring off; maximum aperture bandpass filter characteristic.

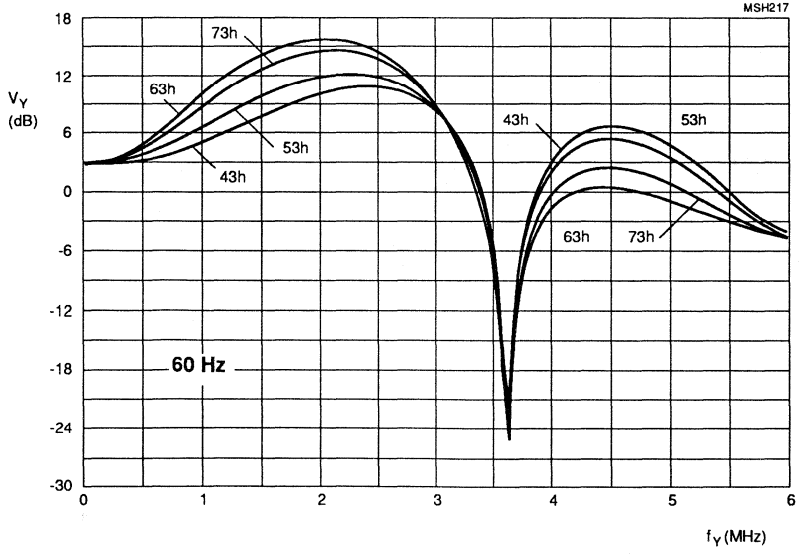


Fig.19 Luminance control in 60 Hz / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; maximum aperture bandpass filter characteristic.

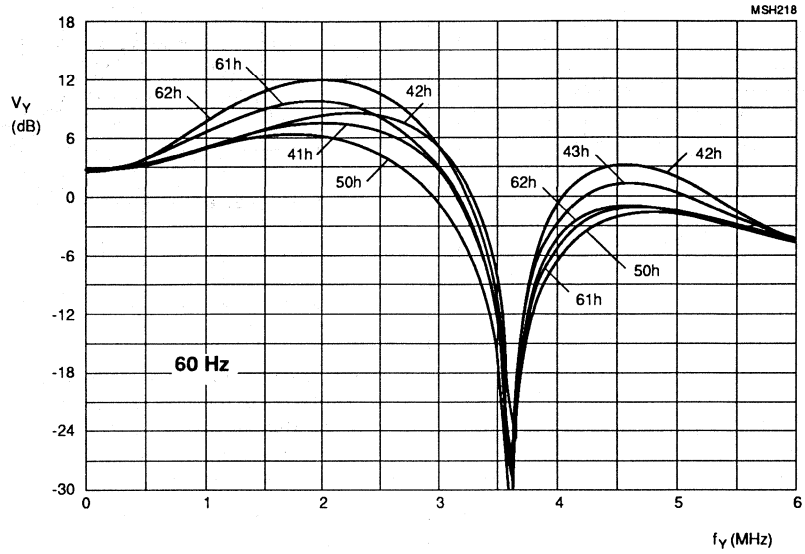


Fig.20 Luminance control in 60 Hz / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; other aperture bandpass filter characteristics.

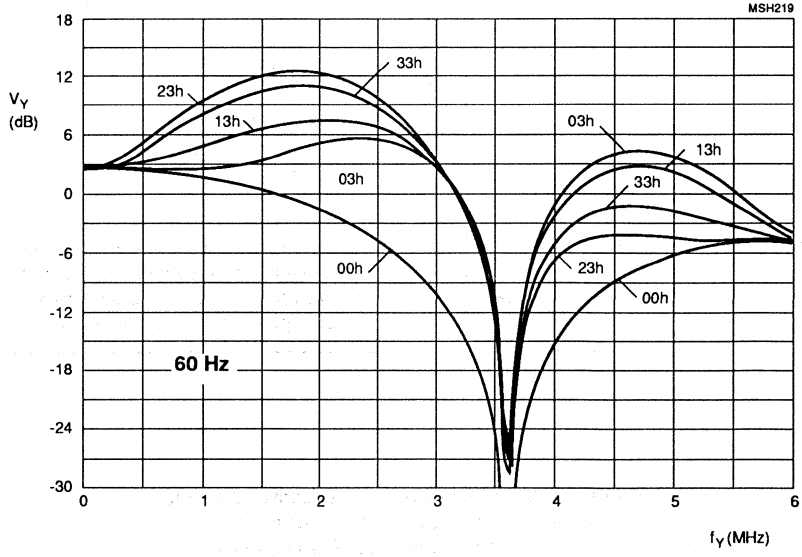


Fig.21 Luminance control in 60 Hz / CVBS mode controllable by subaddress byte 06; pre-filter off and coring off; maximum and minimum aperture bandpass filter characteristics.

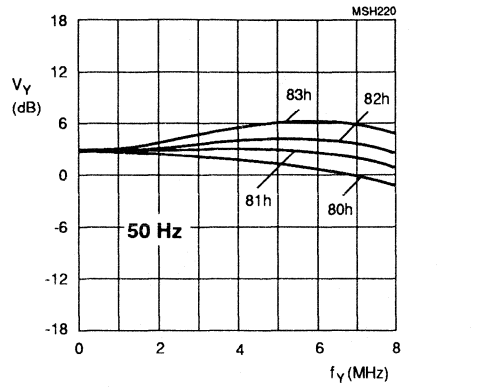


Fig.22 Luminance control in 50 Hz / S-VHS mode controllable by subaddress byte 06; pre-filter off and coring off; different aperture bandpass filter characteristics.

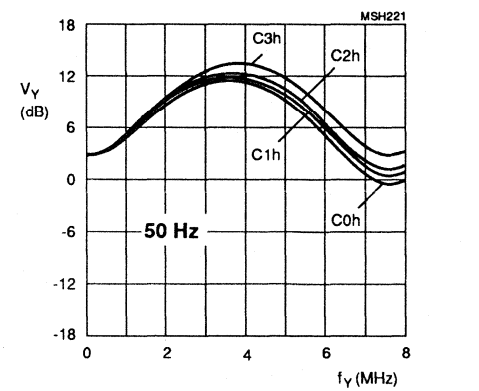


Fig.23 Luminance control in 50 Hz / S-VHS mode controllable by subaddress byte 06; pre-filter on and coring off; different aperture bandpass filter characteristics.

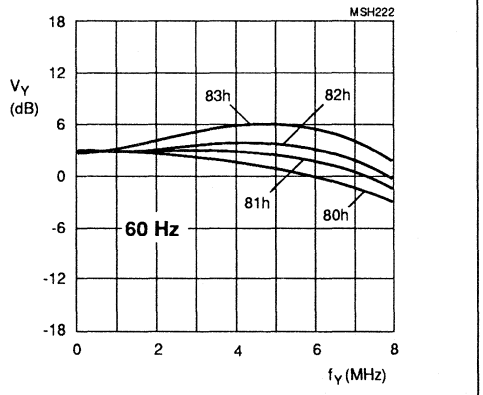


Fig.24 Luminance control in 60 Hz / S-VHS mode controllable by subaddress byte 06; pre-filter off and coring off; different aperture bandpass ffilter characteristics.

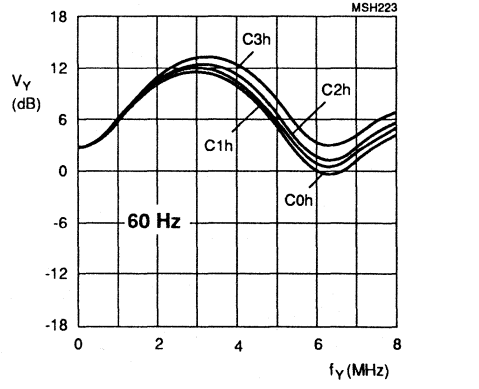
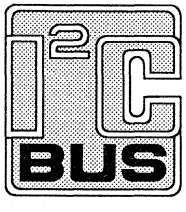


Fig.25 Luminance control in 60 Hz / S-VHS mode controllable by subaddress byte 06; pre-filter on and coring off; different aperture bandpass filter characteristics.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

PROGRAMMING EXAMPLE

Coefficients to set operation for application circuits Figures 13 and 14. (All numbers of the Table 6 are hex values). Slave address byte is 8A at pin 43 = 0 V (or subaddress 8E at pin 43 = 5 V).

Table 6 Recommended default values

SUBADDRESS	BIT NAME	FUNCTION	VALUE (HEX)
00	IDEL(7-0)	increment delay	50
01	HSYB(7-0)	H sync beginning for 50 Hz	30
02	HSYS(7-0)	H sync stop for 50 Hz	00
03	HCLB(7-0)	H clamping beginning for 50 Hz	E8
04	HCLS(7-0)	H clamping stop for 50 Hz	B6
05	HPHI(7-0)	H sync position for 50 Hz	F4
06	BYPS, PREF, BPSS(1-0)		
	CORI(1-0), APER(1-0)	luminance control:	01(1)
07	HUEC(7-0)	hue control (0 degree)	00
08	CKTQ(4-0)	colour-killer threshold QUAM	F8
09	CKTS(4-0)	colour-killer threshold SECAM	F8
0A	PLSE(7-0)	PAL switch sensitivity	90
0B	SESE(7-0)	SECAM switch sensitivity	90
0C	COLO, LFIS(1-0), CGFX	gain control	00
0D	VTRC, SECS	standards/mode control	00(2)(4), 01(3)(4)
0E	HPLL, OEDC, OEHS, OEVS		
	OEDY, CHRS, GPSW(2-1)	I/O and clock control	79, 7E(5)
0F	AUFD, FSEL, SXCR, SCEN,		
	OFTS, YDEL(2-0)	control #3	91(6), 99(7)
10	HRFS, VNOI(1-0)	control #4	00
11	CHCV(7-0)	chrominance control value	2C(8), 59(9)
12	-	set to zero	00
13	-	set to zero	00
14	HS6B(7-0)	H sync beginning for 60 Hz	34
15	HS6S(7-0)	H sync stop for 60 Hz	0A
16	HC6B(7-0)	H clamping beginning for 60 Hz	F4
17	HC6S(7-0)	H clamping stop for 60 Hz	CE
18	HP6I(7-0)	H sync position for 60 Hz	F4

Notes to Table 6

(1) dependent on application (Figures 16 to 25)
(2) for QUAM standards
(3) for SECAM
(4) HPLL is in TV mode; value for VCR mode is 80 (81 for SECAM VCR mode)
(5) for Y/C mode
(6) 4:1:1 format
(7) 4:2:2 format
(8) default value for NTSC-CCIR level
(9) default value for PAL-CCIR level

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	August 1990

SAA7192
Digital colour space converter

INTRODUCTION

The Digital Color Space Converter (DCSC) is a matrix which is used to transform 8-bit digital input signals, i.e. Y (luminance), Cr (colour, R-Y) and Cb (colour, B-Y), into an RGB 8-bit format in accordance with the CCIR-601 recommendations.
The system accepts the formats of the DMSD2 family of decoders at the input. The maximum data rate is 16 MHz. The propagation delay of the device is constant. A matched pipeline delay line is available to enable the HREF signal to be synchronized with the video data at the output.

SYSTEM FUNCTIONS

The DCSC consists of the following functional blocks, as illustrated in Fig.1:

- Input Formatter with;
  multiplexer
  Y-delay line
  Cr and Cb Interpolating filters
- Conversion matrix
- Video look up tables
- Pipeline delay line
- I²C-bus interface

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7192	68	PLCC	plastic	SOT188AA,AGA

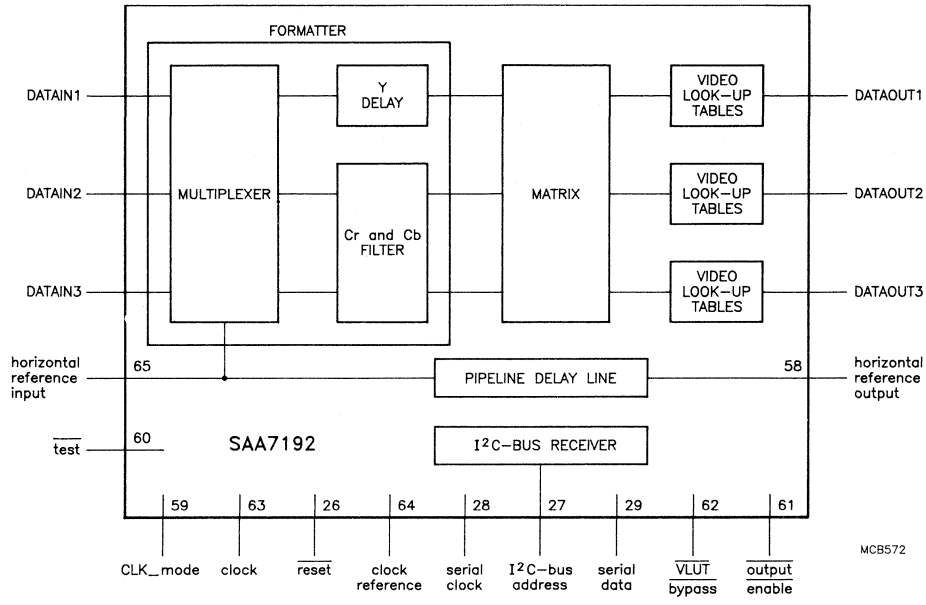


Fig.1 Block diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

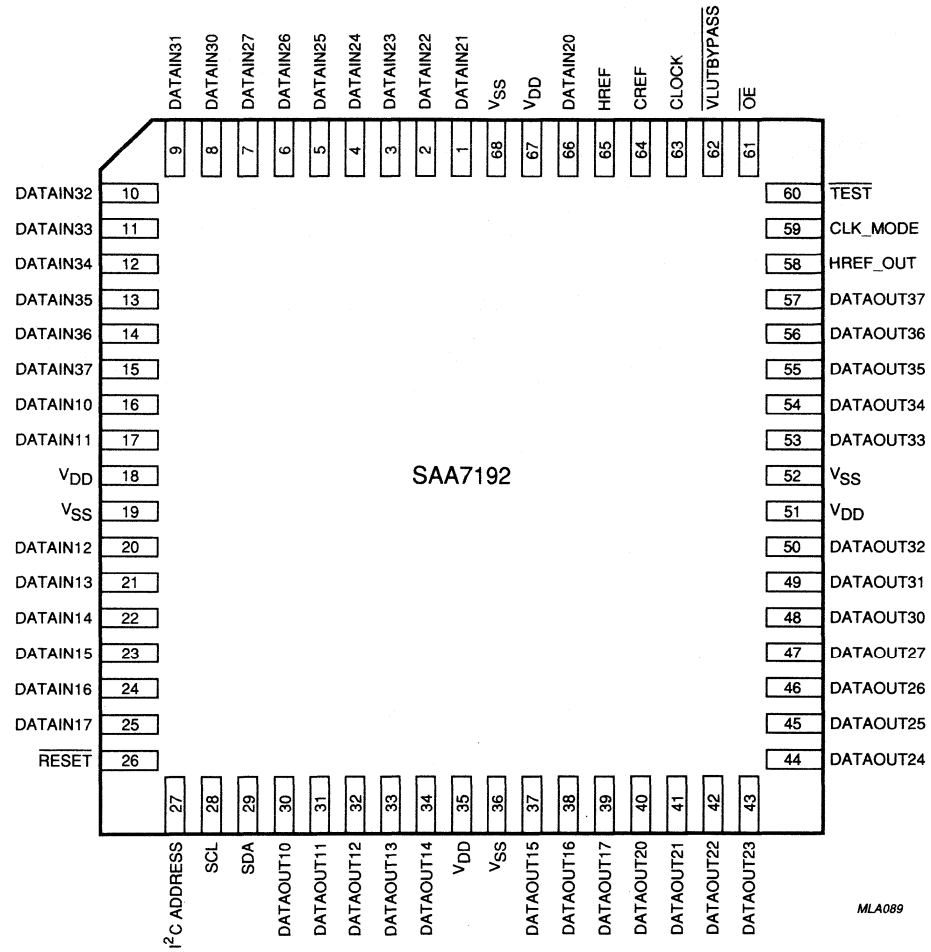


Fig.2 Pinning diagram.

Functional modes

Table 1 Functional Modes.

MODE	FUNCTION
1	4:1:1 filter, no matrix, no VLUT; DATAOUT = upsampled DATAIN
2	4:1:1 filter, matrix, no VLUT; DATAOUT = RGB
3	4:1:1 filter, no matrix, VLUT; DATAOUT = upsampled DATAIN multiplied by the factor loaded into the VLUT
4	4:1:1 filter, matrix, VLUT; DATAOUT = RGB multiplied by the factor loaded into the VLUT
5	4:2:2 filter, no matrix, no VLUT; DATAOUT = upsampled DATAIN
6	4:2:2 filter, matrix, no VLUT; DATAOUT = RGB
7	4:2:2 filter, no matrix, VLUT; DATAOUT = upsampled DATAIN multiplied by the factor loaded into the VLUT
8	4:2:2 filter, matrix, VLUT; DATAOUT = RGB multiplied by the factor loaded into the VLUT
9	no filter, no matrix, no VLUT; DATAOUT = DATAIN "Process Bypass"
10	no filter, matrix, no VLUT; DATAOUT = RGB
11	no filter, no matrix, VLUT; DATAOUT = DATAIN multiplied by the factor loaded into the VLUT.
12	no filter, matrix, VLUT; DATAOUT = RGB multiplied by the factor loaded into the VLUT

Figures 3 to 9b illustrate the various functional modes.

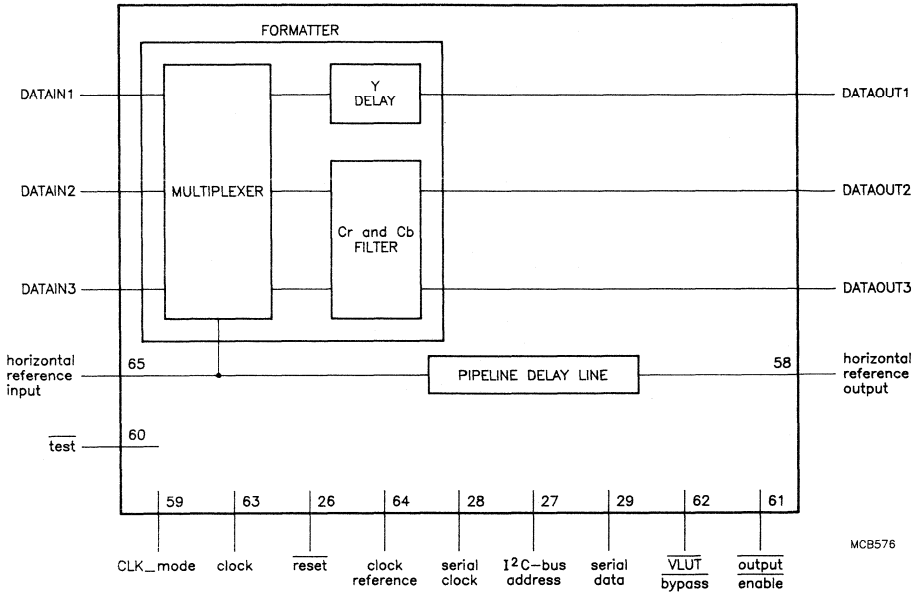


Fig.3 Functional mode 1 and 5.

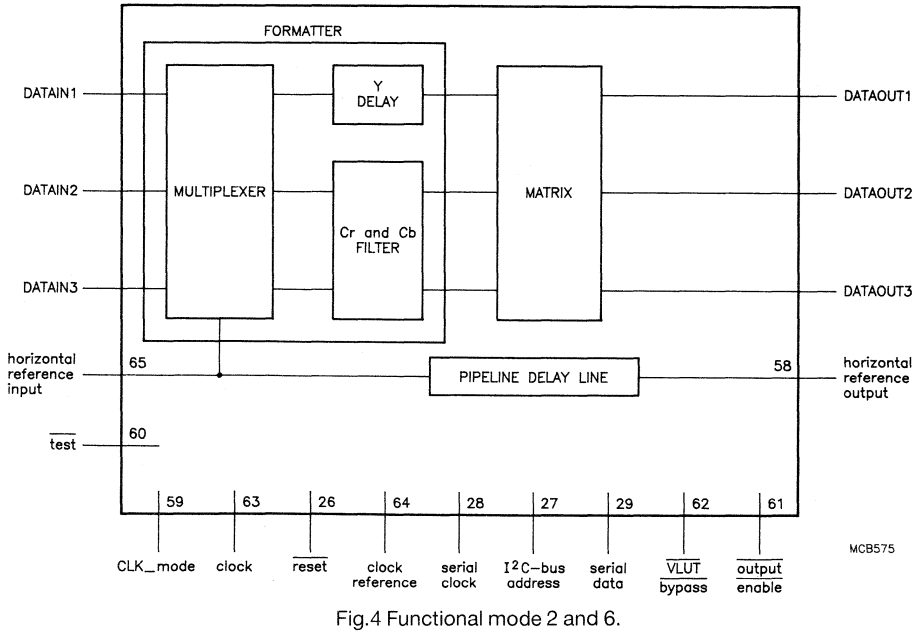


Fig.4 Functional mode 2 and 6.

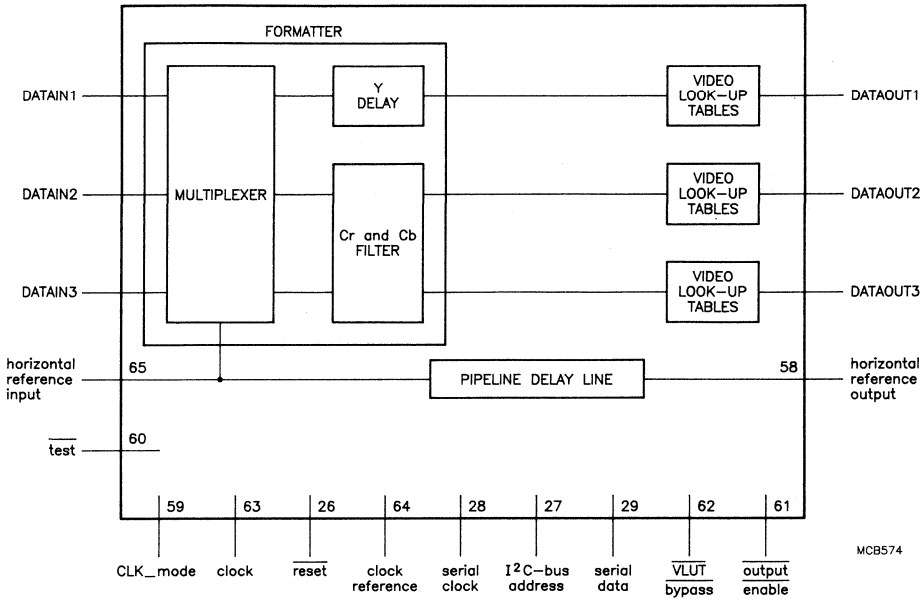


Fig.5 Functional mode 3 and 7.

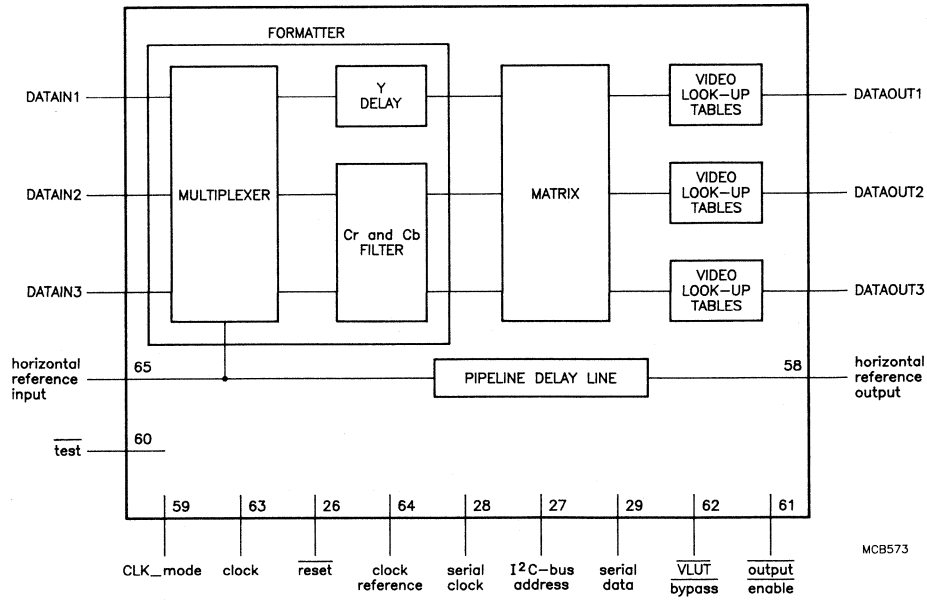


Fig.6 Functional mode 4 and 8.

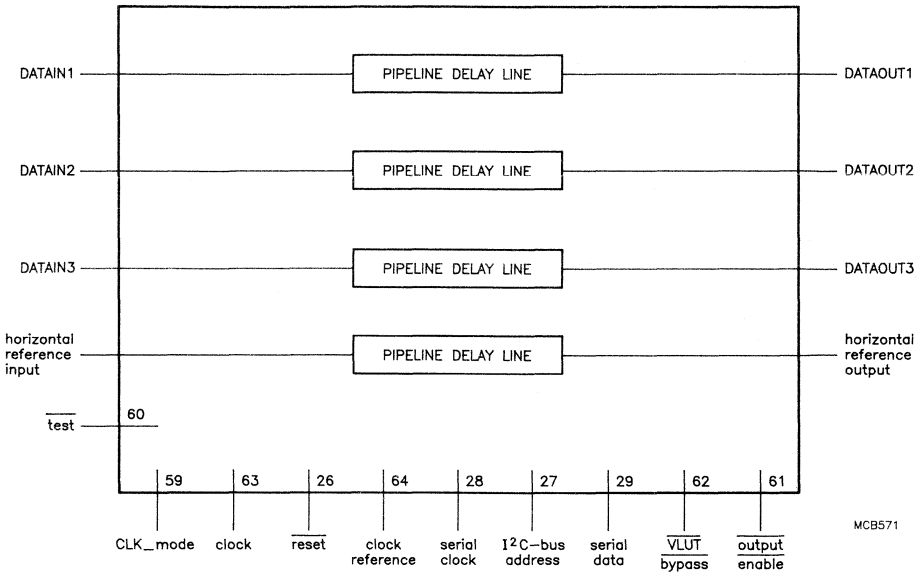


Fig.7 Functional mode 9.

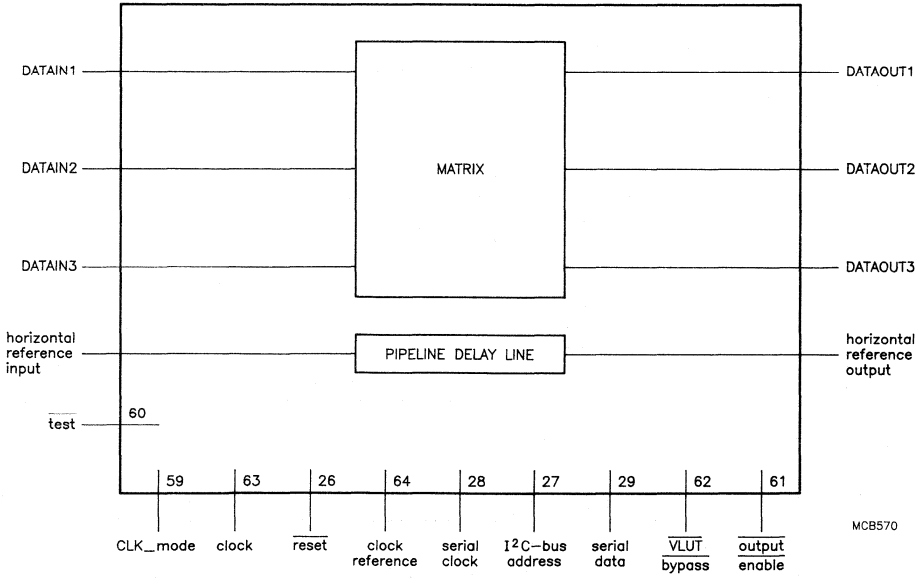


Fig.8 Functional mode 10.

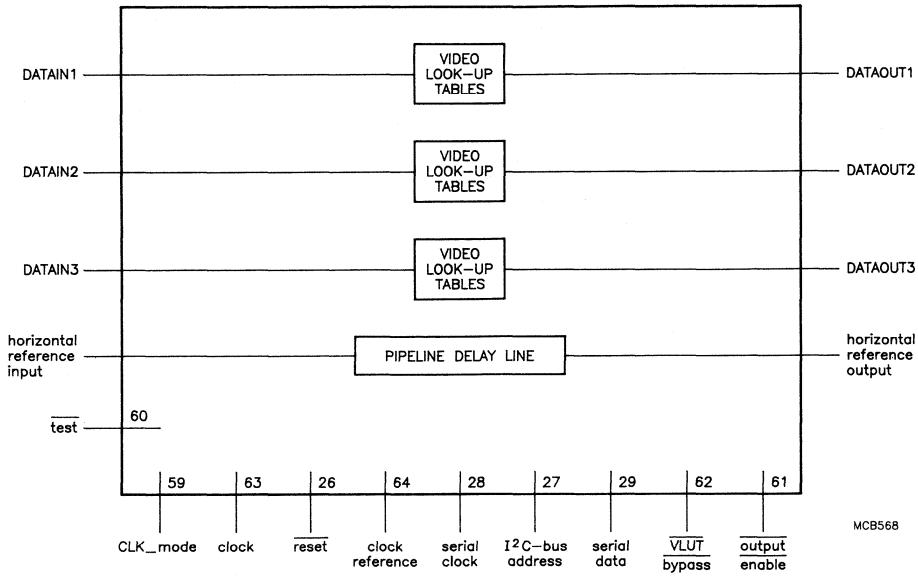


Fig.9a Functional mode 11.

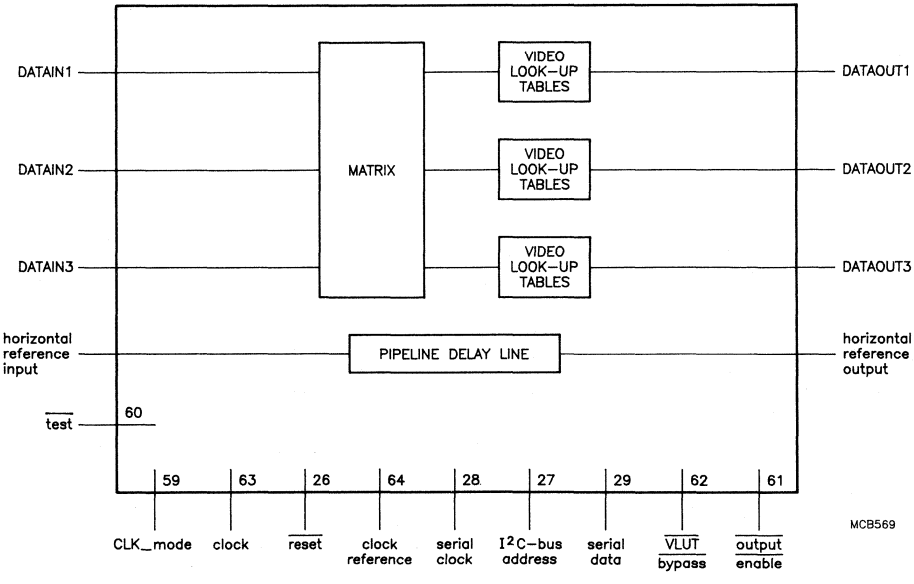


Fig.9b Functional mode 12.

Control facilities

After power-up all internal control signals of the device are at undefined values. The I²C-bus receiver must, therefore, be reset by using the external RESET signal. The control signals are then set to:

IICOE = 1
output in 3-state

FMTCNTRL = 4
format 4:4:4

$\overline{\text{MATBYPASS}}$ = 0
matrix bypassed

$\overline{\text{VLUTLOAD}}$ = 1
VLUT at READ operation

$\overline{\text{INRESET}}$ = 0
input data set to fixed values

Table 2 Input formats and functional modes

FMTCNTRL	$\overline{\text{MATBYPASS}}$	$\overline{\text{VLUTBYPASS}}$	FUNCTIONS
0	0	0	mode 1, input format 1 (DMSD2 format)
0	1	0	mode 2, input format 1 (DMSD2 format)
1	0	0	mode 1, input format 2
1	1	0	mode 2, input format 2
2	0	0	mode 5, input format 3 (DMSD2 format)
2	1	0	mode 6, input format 3 (DMSD2 format)
3	0	0	mode 5, input format 4 (parallel IN)
3	1	0	mode 6, input format 4 (parallel IN)
4	0	0	mode 9, input format 5 (parallel IN)
4	1	0	mode 10, input format 5 (parallel IN)
x	x	1	each of the above described modes will be multiplied by the factor loaded into the VLUT.

Note

The modes are given in Table 1.

The other control signals are:

$\overline{\text{VLUTLOAD}}$ = logic 1: VLOAD inactive
= logic 0: VLOAD datalines active to load VLUT

$\overline{\text{INRESET}}$ = logic 1: input latches at the formatter are always transparent
= logic 0: at the end of each active video line the input latches have to be set to fixed values (Y to 16; Cr and Cb to 128; if HREF = 0)

CLK_MODE = logic 1: DMSD mode (LL27 clock of DMSD feeds the DCSC)
= logic 0: DCSC is fed by a maximum 16 MHz clock without CREF signal.

Table 3 Output enable control

IICOE	$\overline{OE}$	CONTROL LINE TO DRIVER STAGES
0	X	1 = DATAOUT in high impedance mode
1	1	1 = DATAOUT in high impedance mode
1	0	0 = DATAOUT working

Note

IICOE: output enable control of I^2C-bus (enables $\overline{OE}$)
$\overline{OE}$: output enable (fast switch)

SYSTEM I/O INTERFACES

Input signals

VIDEO DATA (DATAIN)

Table 4 Format 1 (4:1:1, semi-parallel, DMSD2 format)

DATAIN1 - Y	luminance signal, 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black, quantization level 16 100 IRE; white, quantization level 235
DATAIN3 - U, V	multiplexed colour difference signals 4-bit; corresponds to UV7 to UV4 of DMSD2
Sampling frequency	1/4 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128
DATAIN2	not used

Table 5 Timing of Format 1; pin (DATAIN) and bit (U,V) numbers are indicated except clock

Y; 7 to 0	Y	Y	Y	Y	Y	Y	Y
DATAIN2, 7	U7	U5	U3	U1	U7	U5	U3
DATAIN2, 6	U6	U4	U2	U0	U6	U4	U2
DATAIN2, 5	V7	V5	V3	V1	V7	V5	V3
DATAIN2, 4	V6	V4	V2	V0	V6	V4	V2
Clock A	1	2	3	4	5	6	7

Table 6 Format 2 (4:1:1, semi-parallel, customized format)

DATAIN1 - Y	luminance signal; 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235
DATAIN3 - Cr, Cb	multiplexed colour difference signals,8-bit
Sampling frequency	1/4 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128
DATAIN2	not used

Table 7 Timing of Format 2; the indexes show the clock (sample) number

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cr, Cb	Cb0		Cr0		Cb4		Cr4
Clock A	0	1	2	3	4	5	6

Table 8 Format 3 (4:2:2, semi-parallel, DMSD2 format)

DATAIN1 - Y	luminance signal; 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235
DATAIN3 - Cr, Cb	multiplexed colour difference signals corresponds to UV7 to UV0 of DMSD2
Sampling frequency	1/2 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128
DATAIN2	not used

Table 9 Timing of Format 3

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cr, Cb	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4	Cb6
Clock A	0	1	2	3	4	5	6

Table 10 Format 4 (4:2:2, Y-Cr-Cb, parallel)

DATAIN1 - Y	luminance signal; 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235
DATAIN3 - Cb	colour difference signal B-Y, 8-bit
Sampling frequency	1/2 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128b
DATAIN2 - Cr	colour difference signal R-Y, 8-bit
Sampling frequency	1/2 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128

Table 11 Timing of Format 4

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cb	Cb0		Cb2		Cb4		Cb6
Cr	Cr0		Cr2		Cr4		Cr6
Clock A	0	1	2	3	4	5	6

Table 12 Format 5 (4:4:4, Y-Cr-Cb, parallel)

DATAIN1 - Y	luminance signal; 8-bit
Sampling frequency	maximum 16.0 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235
DATAIN2 - Cr	colour difference signal R-Y, 8-bit
Sampling frequency	maximum 16.0 MHz
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless, binary 128
DATAIN3 - Cb	colour difference signal B-Y, 8-bit
Sampling frequency	maximum 16.0 MHz
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128

Table 13 Timing of Format 5

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cb	Cb0	Cb1	Cb2	Cb3	Cb4	Cb5	Cb6
Cr	Cr0	Cr1	Cr2	Cr3	Cr4	Cr5	Cr6
Clock A	0	1	2	3	4	5	6

CONTROL DATA

Clock

The line locked clock LL27 (denoted as CLOCK at the DCSC input) is twice the data rate of that specified for the DMSD2 family of decoders. The data rate is denoted as CLOCK_A in Tables 5, 7, 9, 11 and 13.

The data rate on the input (DATAIN) is as follows;

12.2727 MHz; 60 Hz signals (from SAA7191)
13.5 MHz; CCIR signals (from SAA7151)
14.75 MHz; 50 Hz signals (from SAA7191)
16.0 MHz; maximum frequency

Timing reference (Fig.10)

The timing reference signal from the SAA7151/7191 is used to synchronize the multiplexer and refers to the LL27 clock. Each alternative positive slope, marked by a CREF signal, is used to obtain data. The horizontal reference signal, HREF, indicates the active part of a line and also synchronizes the multiplexer.

CREF The clock reference signal is a clock qualifier signal distributed by the clock generator of the DMSD system. The frequency is identical to the sample rates denoted in the input and the output formats (see Video data and Operating conditions).

HREF Horizontal reference signal is the line reference signal of the YUV-bus. A positive slope marks the beginning of the active part of a line. The length of the active part corresponds to the number of samples (see Operating conditions).

Table 14 Real-time control signals

$\overline{OE}$	= 1 : = 0 :	switches the output to high-z mode output enable, output stage in use
$\overline{VLUTBYPASS}$	= 1 : = 0 :	VLUT's in use VLUT's bypassed
$\overline{RESET}$	= 1 : = 0 :	device in use general reset
CLK_MODE	= 1 : = 0 :	DMSD mode (LL27 clock of DMSD feeds the DCSC) DCSC is feed by a clock signal with a maximum data rate of 16 MHz (without CREF signal).

Table 15 I²C-bus controls

FMTCNTRL	= 0 : = 1 : = 2 : = 3 : = 4 : = 5 : = 6 : = 7 :	4:1:1 format, DMSD2 format 4:1:1 format, customized format 4:2:2 format, from DMSD2 4:2:2 format, parallel 4:4:4 format, parallel not used not used not used
$\overline{MATBYPASS}$	= 1 : = 0 :	matrix in use matrix bypassed
$\overline{VLUTLOAD}$	= 1 : = 0 :	VLOAD inactive VLOAD data lines active to load VLUT
VLUTDATA	:	load VLUT's via I²C-bus (256 x 8-bit)
$\overline{INRESET}$	= 1 : = 0 :	input latches at the formatter are always transparent at the end of each active video line the input latches have to be set to fixed values (Y to 16; Cr, Cb to 128; if HREF = 0)
IICOE	= 1 : = 0 :	$\overline{OE}$ enabled switches the output to high impedance mode

Output signals

VIDEO DATA

$\overline{OE}$ (output enable, fast switch, active LOW) and IICOE (I^2C output enable, active HIGH) switchs the DATAOUT lines when in the high-impedance mode (see Control facilities).

Table 16 Format of DATAOUT (RGB if matrix in use)

DATAOUT1 (0 to 7)	Red
DATAOUT2 (0 to 7)	Green
DATAOUT3 (0 to 7)	Blue
To all three DATAOUT lines:	
Sampling frequency	12 to 16 MHz
Level	0 IRE; quantization level 16 100 IRE; quantization level 235

AUXILIARY DATA

Pipelined external reference signal HREF_OUT (delayed HREF).

The delay line (wordlength 1-bit) has the same duration as the signal processing of the video data lines.

OPERATING CONDITIONS

Electrical Conditions

Start-up condition

No particular function except the external power-on-reset e.g. for I^2C-bus interface (RESET) is intended.

Operating time

As this device will be used in computers, it has been designed to operate continuously.

Temperature range

Refer to the characteristics.

Backup

No backup capability (standby) is provided internally.

Power down mode

No power-down capability is provided internally.

CHARACTERISTICS

SYMBOL	PARAMETERS	CONDITIONS	MIN.	MAX.	UNIT
Supply					
V_{DD}	supply voltage range		4.5	5.5	V
Inputs					
V_{IL}	input voltage LOW (SDA, SCL)		−0.5	1.5	V
V_{IH}	input voltage HIGH (SDA, SCL)		3.0	V_{DD} +0.5	V
V_{IL}	input voltage LOW (any other)		−0.5	0.8	V
V_{IH}	input voltage HIGH (any other)		2.0	V_{DD} +0.5	V
I_{LI}	input leakage current		-	10	µA
C_I	input capacitance (clocks)		-	10	pF
C_I	input capacitance (data)		-	8	pF
Outputs					
V_{OH}	output voltage HIGH	note 1	2.4	V_{DD}	V
V_{OL}	output voltage LOW	note 1	0	0.6	V
C_L	output load capacitance (data and HREF)		15	40	pF
Timing					
t_{LL27}	cycle time	note 2	31	45	ns
k_{LL27}	duty factor		40	60	%
t_r	rise time		-	5	ns
t_f	fall time		-	6	ns
t_{CDL}	duty time LOW	note 3	26	-	ns
t_{CDH}	duty time HIGH		18	-	ns
t_{CS}	CREF set-up time		*	11	ns
t_{CH}	CREF hold time		*	3	ns
t_{HS}	HREF set-up time		*	11	ns
t_{HH}	HREF hold time		*	3	ns
$t_{SU;DAT}$	input data set-up time		11	-	ns
$t_{HD;DAT}$	input data hold time		3	-	ns
t_{OH}	ouput hold time		13	-	ns
$t_{OS;DAT}$	output data set-up time		14	-	ns
t_{SZ}	output disable time to 3-state		*	-	ns
t_{ZS}	output enable time from 3-state		*	-	ns

Note to the characteristics

1. The levels must be measured with the following load circuits; 0.6 kΩ to 3.0 V (2 TTL load); C_L = 40 pF.

2. DMSD-mode means that the DCSC will work in a DMSD environment. The CLOCK and the clock reference signal CREF is fed by the SCGC (SAA7157).

3. 16 MHz-mode means that the DCSC will work in any other environment. The CREF signal will be set to HIGH, the CLOCK signal can be any clock up to 16 MHZ.

* Value to be fixed

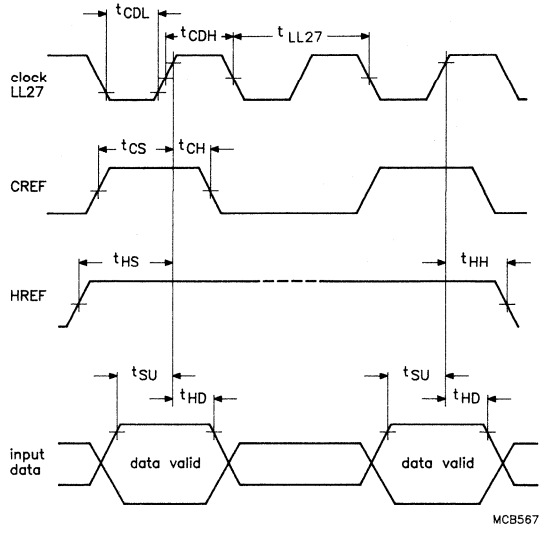


Fig.10 Input timing diagram.

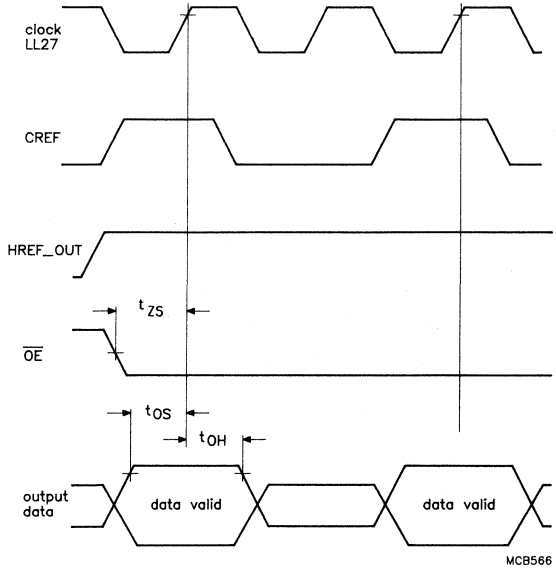


Fig.11 Output timing diagram.

Error condition

So as to inhibit unwanted operations, no information signal is available to the peripheral circuits. In the advent of an error the system has to be started again by applying the $\overline{\text{RESET}}$ signal.

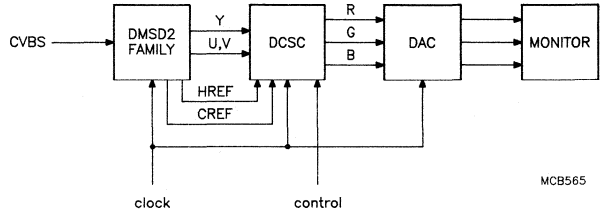


Fig.12 Application example.

SYSTEM BLOCK DESCRIPTION

INPUT FORMATTER

The formatter consist of five functional blocks;

- the multiplexer, which decodes the luminance and chrominance input signals
- the filter, which interpolates the samples of the incoming signal to get an upsampled data rate as at DATAIN1
- the luminance delay line;
- the timing control which creates the internal reference signals from the various inputs
- the bypass output multiplexer

Multiplexer

The data applied at DATAIN1 to DATAIN3 is converted as follows;

FIL1 : Y Luminance
FIL2 : Cb colour-difference signal B-Y
FIL3 : Cr colour-difference signal R-Y

The formats and data rates of DATAIN are described in 'Video data' (see tables 4 to 13).

The sampling frequency of the FIL data lines is 16 MHz maximum. The levels of the FIL data lines are the same as characterized for the DATAIN signals.

The timing reference signals CLOCK, HREF and CREF, for distinguishing the incoming data signals, are described in 'Control data'.

The signal FMTCNTRL is used to control the multiplexer and the filter.

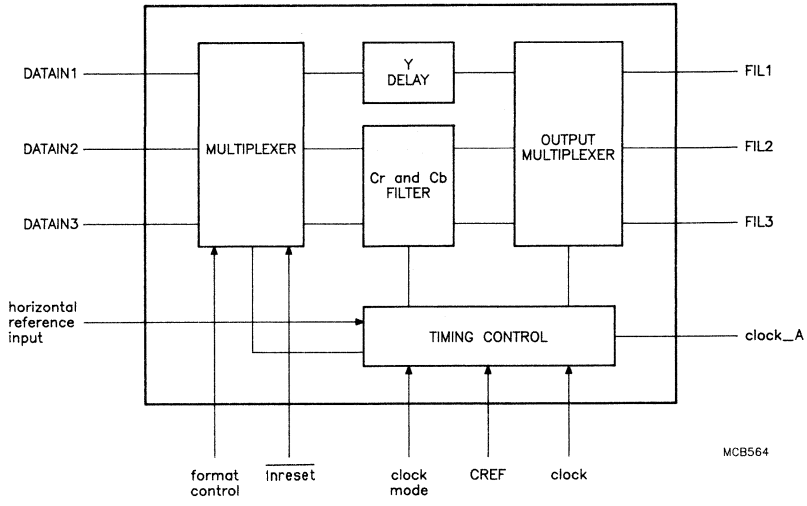


Fig.13 Input formatter.

FMTCNTRL = 0 : 4:1:1 format; DMSD2 format
= 1 : 4:1:1 format; customized format
= 2 : 4:2:2 format; from DMSD2
= 3 : 4:2:2 format; parallel
= 4 : 4:4:4 format; parallel
= 5 : not used
= 6 : not used
= 7 : not used

$\overline{\text{INRESET}}$ = 1 : input latches transparent
= 0 : input latches has to be set to fixed values (Y to 16, Cr, Cb to 128) if HREF = 0

CLK_MODE = 1 : DMSD mode (LL27 clock of DMSD feeds the DCSC)
= 0 : DCSC is feed by a clock of maximum 16 MHz without CREF signal.

Timing control

The timing control unit generates the required control signals from the incoming reference signals and the internally used CLOCK_A.

Filter and delay line

In the various functional modes the signal FMTCNTRL switches in the required filters (FMTCNTRL is described in 'Control data'). In all modes the same propagation delay will be realized, (the reference is Cb0).

DELAY LINE (LUMINANCE-DELAY)

At all frequencies and in all formats, there is a delay line to compensate for the delay of the signal processing time needed in the chrominance section.

CHROMINANCE FILTER

The filter for the Cr and Cb signal is realized in one filter design.

Format 1, 2 4:1:1

An interpolating filter is inserted to convert the original sampling frequency to the sampling frequency of the luminance signal i.e. four times the colour signal. Figure 14 illustrates the frequency response of the chrominance section.

Format 3, 4 4:2:2

An interpolating filter is inserted to convert the original sampling frequency to the sampling frequency of the luminance signal i.e. twice the colour signal. Figure 15 illustrates the frequency response of the chrominance section.

Format 5 4:4:4

A bypass with a specified delay is inserted.

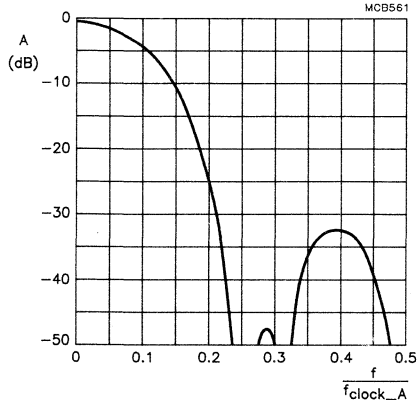


Fig.14 Frequency response of 4:1:1 filter.

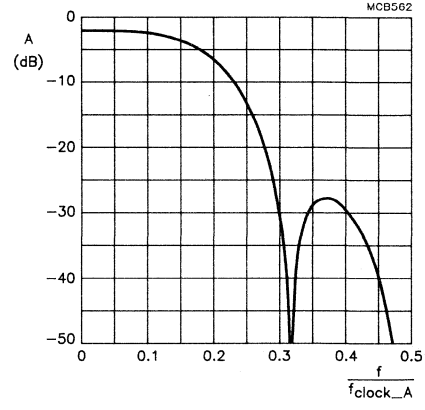


Fig.15 Frequency response of 4:2:2 filter

CONVERSIONAL MATRIX

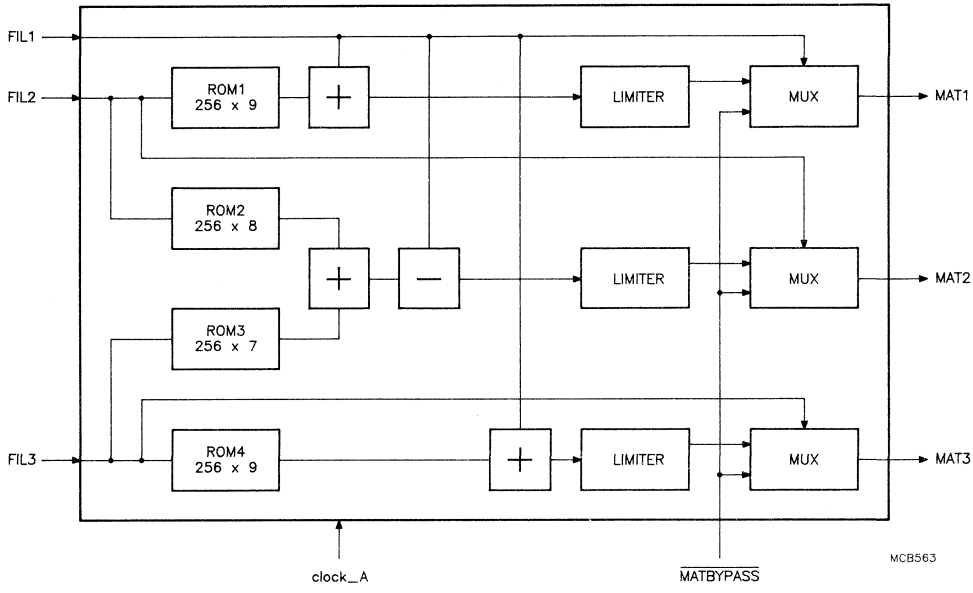


Fig.16 Block diagram MATRIX.

The properties of the conversion matrix are as follows:

- the conversion equations are (according to CCIR 601, with respect to the different quantisation on Y, Cb and Cr);

  Red = Y + 1.371 (Cr - 0.5)
  Green = Y - 0.698 (Cr - 0.5)
  - 0.336 (Cb - 0.5)
  Blue = Y + 1.732 (Cb - 0.5)

- the accuracy of the signal processing is within ± 0.5% of the accuracy of a theoretical conversion.

- the input and output data lines are 8-bit.

- $\overline{\text{MATBYPASS}}$ switches the matrix in bypass. The bypass has the same propagation delay as the matrix itself.

Input/Output Data

The levels are as follows:

FIL1 : luminance signal Y
: 0 IRE; black, quantization level 16
100 IRE; white, quantization level 235

FIL2 : multiplexed colour difference signals Cr
: bottom peak; quantization level 16
: top peak; quantization level 240
: colourless; quantization level 128

FIL3 : multiplexed colour difference signals Cb
: bottom peak; quantization level 16
: top peak; quantization level 240
: colourless; quantization level 128

The data rate on the input is maximum 16 MHz

The levels at the input and output, for some specific colour patterns, are given in Table 17.

CONTROL SIGNALS

$\overline{\text{MATBYPASS}}$ = 1 : matrix in use
= 0 : matrix bypassed

Functional description

Four ROMs are used to obtain the coefficients with the required accuracy.

In the advent of non-standard input levels the limiter reduces the possible data values at the output (red, green, blue channel) to values between 0 and 255. Consequently, all negative values are set to 0 and all values higher than 255 are set to 255.

Table 17 Levels at the functional blocks

test number	Y FIL1	CR FIL2	CB FIL3	MAT1 R	MAT2 G	MAT3 B
1 (white)	235	128	128	235	235	235
2 (black)	16	128	128	16	16	16
3 (red)	82	240	90	235	16	16
4 (green)	145	34	54	16	236	16
5 (blue)	41	110	240	16	16	235

VIDEO LOOK-UP TABLE AND OUTPUT STAGE

Functional description

The $\overline{\text{VLUTLOAD}}$ signal enables the memories to obtain data from the VLUTDATA signal via the I²C-bus (auto-increment mode). The three RAMs will also obtain the same data.

$\overline{\text{VLUTBYPASS}}$ will bypass the VLUT's in clock period time (real time switch).

In computer applications the VLUT is also known as Colour Look-Up Table (CLUT).

In the DCSC this table might be used to invert the Gamma-correction of a camera. This correction is applied to compensate for the non-linear relationship between the video voltage applied to the cathode and the light output of the phosphor of a CRT.
The Gamma-correction function (also known as Gradation) is given as;

$$Y = X^{\gamma}$$

The VLUT's are realized by 256 x 8-bit RAMs.

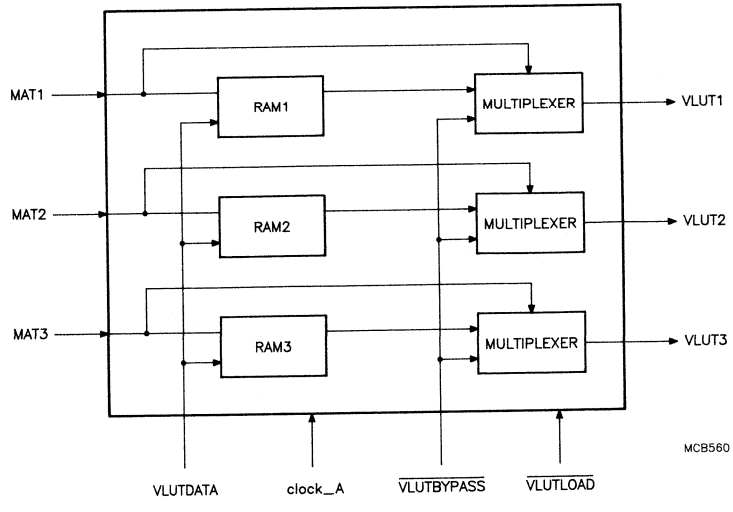


Fig.17 Block diagram video look up table.

I²C-bus receiver

Functional description

At switch-on all internal control signals are at undefined values and the I²C-bus receiver must, therefore, be reset by the external $\overline{\text{RESET}}$ signal. After reset the control signals will be set as follows:

IICOE	= logic 1	$\overline{\text{OE}}$ enabled
FMTCNTRL	= 4	format 4:4:4
$\overline{\text{MATBYPASS}}$	= logic 0	matrix bypassed
$\overline{\text{VLUTLOAD}}$	= logic 1	VLUT at read operation
$\overline{\text{INRESET}}$	= logic 0	input data set to fixed values

Receiver organisation

The address for the DCSC is as follows:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	1	0	0	0	X	0

write only

hardware programmable address bit

S	DCSC ADDRESS	A	SUB-ADDRESS	A	DATA BYTE	A	P

where S = start
A = acknowledge
P = stop

Table 18 Sub-address and data byte formats

HEX SUBADD	BINARY - DATA								FUNCTION
	D7	D6	D5	D4	D3	D2	D1	D0	
00	X	X	X	X	X	0	0	0	input formatter to Format 1
00	X	X	X	X	X	0	0	1	input formatter to Format 2
00	X	X	X	X	X	0	1	0	input formatter to Format 3
00	X	X	X	X	X	0	1	1	input formatter to Format 4
00	X	X	X	X	X	1	0	0	input formatter to Format 5
00	X	X	X	X	0	X	X	X	matrix bypassed
00	X	X	X	X	1	X	X	X	matrix in use
00	X	X	X	0	X	X	X	X	input data at fixed values
00	X	X	X	1	X	X	X	X	input data to formatter
00	X	X	1	X	X	X	X	X	$\overline{OE}$ enabled
00	X	X	0	X	X	X	X	X	output stages 3-state
00	X	0	X	X	X	X	X	X	VLUT write enabled
00	X	1	X	X	X	X	X	X	VLUT read enabled
01	X	X	X	X	X	X	X	X	VLUTDATA

where;

D0 to D2 = FMTCONTROL
D3 = $\overline{MATBYPASS}$
D4 = $\overline{INRESET}$
D5 = IICOE
D6 = $\overline{VLUTLOAD}$
D7 = not used

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	May 1992

SAA7197

Clock signal generator circuit for Desktop Video systems (SCGC)

FEATURES

- Suitable for Desktop Video systems
- Two different sync sources selectable
- PLL frequency multiplier to generate 4 times of input frequency
- Dividers to generate clocks LLCA, LLCB, LLC2A and LLC2B (2nd and 4th multiples of input frequency)
- PLL mode or VCO mode selectable
- Reset control and power fail detection

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8, 17)	4.5	5.0	5.5	V
I_{DDA}	analog supply current	3	-	9	mA
I_{DDD}	digital supply current	10	-	60	mA
V_{LFCO}	LFCO input voltage (peak-to-peak value)	1	-	V_{DDA}	V
f_i	input frequency range	5.5	-	8.0	MHz
V_I	input voltage LOW input voltage HIGH	0 2.0	- -	0.8 V_{DDD}	V V
V_O	output voltage LOW output voltage HIGH	0 2.6	- -	0.6 V_{DDD}	V V
T_{amb}	operating ambient temperature range	0	-	70	°C

GENERAL DESCRIPTION

The SAA7197 generates all clock signals required for a digital TV system suitable for the SAA719x family. The circuit operates in either the phase-locked loop mode (PLL) or voltage controlled oscillator mode (VCO).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7197	20	DIL	plastic	SOT146
SAA7197T	20	mini-pack (SO20)	plastic	SOT163A

Clock signal generator circuit for Desktop Video systems (SCGC)

SAA7197

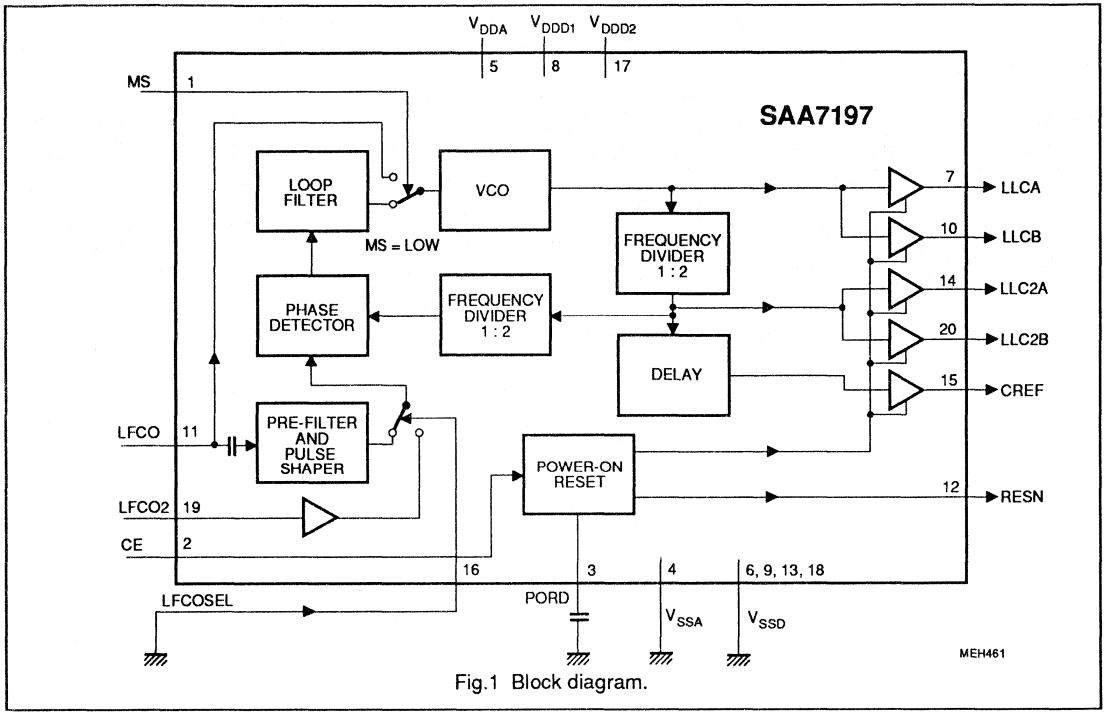


Fig.1 Block diagram.

FUNCTION DESCRIPTION

The SAA7197 generates all clock signals required for a digital TV system suitable for the SAA719x family consisting of an 8-bit analog-to-digital converter (ADC8), digital video multistandard decoder, square pixel (DMSD-SQP), digital video colour space converter (DCSC) and optional extentions. The SAA7197 completes a system for Desktop Video applications in conjunction with memory controllers.

The input signal LFCO is a digital-to-analog converted signal provided by the DMDS-SQPs horizontal PLL. It is the multiple of the line frequency:

7.38 MHz = 472 x f_H in 50 Hz systems
6.14 MHz = 360 x f_H in 60 Hz systems

LFCO2 (TTL-compatible signal from an external reference source) can be applied to pin 19 (LFCOSEL = HIGH).

The input signal LFCO or LFCO2 is multiplied by factors 2 or 4 in the PLL (including phase detector, loop filter, VCO and frequency divider) and output on LLCA (pin7), LLCB (pin 10), LLC2A (pin 14) and LLC2B (pin 20). The rectangular output signals have 50 % duty factor. Outputs with equal frequency may be connected together externally. The clock outputs go HIGH during power-on reset (and chip enable) to ensure that no output clock signals are available the PLL has locked-on.

Mode select MS

The LFCO input signal is directly connected to the VCO at MS = HIGH. The circuit operates as an oscillator and frequency divider. This function is not tested.

Source select LFCOSEL

Line frequency control signal LFCO (pin 11) is selected by LFCOSEL = LOW. LFCOSEL = HIGH selects LFCO2 input signal (pin 19). This function is not tested.

Chip enable CE

The buffer outputs are enabled and RESN set HIGH by CE = HIGH (Fig.4). CE = LOW sets the clock outputs HIGH and RESN output LOW.

CREF output

2 f_{LFCO} output to control the clock dividers of the DMSD-SQP chip family.

Power-on reset

Power-on reset is activated at power-on, when the supply voltage decreases below 3.5 V (Fig.4) or when chip enable is done. The indicator output RESN is LOW for a time determined by capacitor on pin 3. The RESN signal can be applied to reset other circuits of this digital TV system.
The LFCO or LFCO2 input signals have to be applied before RESN becomes HIGH.

Clock signal generator circuit for Desktop Video systems (SCGC)

SAA7197

PINNING

SYMBOL	PIN	DESCRIPTION
MS	1	mode select input (LOW = PLL mode)*
CE	2	chip enable /reset (HIGH = outputs enabled)
PORD	3	power-on reset delay, dependent on external capacitor
V_{SSA}	4	analog ground (0 V)
V_{DDA}	5	analog supply voltage (+5 V)
V_{SSD1}	6	digital ground 1 (0 V)
LLCA	7	line-locked clock output signal (4 times f_{LFCO})
V_{DDD1}	8	digital supply voltage 1 (+5 V)
V_{SSD2}	9	digital ground 2 (0 V)
LLCB	10	line-locked clock output signal (4 times f_{LFCO})
LFCO	11	line-locked frequency control input signal 1
RESN	12	reset output (active-LOW, Fig.4)
V_{SSD3}	13	digital ground 3 (0 V)
LLC2A	14	line-locked clock output signal 2A (2 times f_{LFCO})
CREF	15	clock reference output, qualifier signal (2 times f_{LFCO})
LFCOSEL	16	LFCO source select (LOW = LFCO selected)*
V_{DDD2}	17	digital supply voltage 2 (+5 V)
V_{SSD4}	18	digital ground 4 (0 V)
LFCO2	19	line-locked frequency control input signal 2*
LLC2B	20	line-locked clock output signal 2B (2 times f_{LFCO})

PIN CONFIGURATION

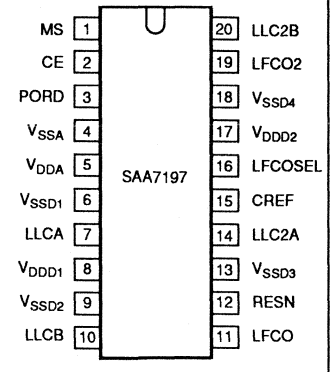


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); ground pins as well as supply pins together connected.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	–0.5	7.0	V
V_{DDD}	digital supply voltage (pins 8 and 17)	–0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{DDA} - V_{DDD}$	-	±100	mV
V_O	output voltage (I_{OM} = 20 mA)	–0.5	V_{DDD}	V
P_{tot}	total power dissipation (DIL20)	0	1.1	W
T_{stg}	storage temperature range	–65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling** for all pins	-	tbf	V

* MS and LFCO2 functions are not tested. LFCO2 is a multiple of horizontal frequency.

** Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take normal handling precautions appropriate to "Handling MOS devices ".

CHARACTERISTICS

V_{DDA} = V_{DDD} = 4.5 to 5.5 V; f_{LFCO} = 5.5 to 8.0 MHz and T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8 and 17)		4.5	5.0	5.5	V
I_{DDA}	analog supply current (pin 5)		3	-	9	mA
I_{DDD}	digital supply current ($I_8 + I_{17}$)	note 1	10	-	60	mA
V_{reset}	power-on reset threshold voltage	Fig.4	-	3.5	-	V
Input LFCO (pin 11)						
V_{11}	DC input voltage		0	-	V_{DDA}	V
V_i	input signal (peak-to-peak value)		1	-	V_{DDA}	V
f_{LFCO}	input frequency range		5.5	-	8.0	MHz
C_{11}	input capacitance		-	-	10	pF
Inputs MS, CE, LFCOSEL and LFCO2 (pins 1, 2, 16 and 19); note 3						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}	V
f_{LFCO2}	input frequency range for LFCO2		5.5	-	8.0	MHz
I_{LI}	input leakage current	LFCOSEL	50	-	150	µA
		others	-	-	10	µA
C_I	input capacitance		-	-	5	pF
Output RESN (pin 12)						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −0.5 mA	2.4	-	V_{DDD}	V
t_d	RESN delay time	C_3 = 0.1µF; Fig.4	20	-	200	ms
Output CREF (pin 15)						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	-	0.6	V
V_{OH}	output voltage HIGH	I_{OH} = −0.5 mA	2.4	-	V_{DDD}	V
f_{CREF}	output frequency CREF	Fig.3	-	2 $f_{LFCO(2)}$		MHz
C_L	output load capacitance		15	-	40	pF
t_{SU}	set-up time	Fig.3; note 1	12	-	-	ns
t_{HD}	hold time	Fig.3; note 1	4	-	-	ns
Output signals LLCA, LLCB, LLC2A and LLC2B (pins 7, 10, 14, and 20); note 3						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	-	0.6	V
V_{OH}	output voltage HIGH	I_{OH} = −0.5 mA	2.6	-	V_{DDD}	V
t_{comp}	composite rise time	Fig.3; notes 1 and 2	-	-	8	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{LL}	output frequency LLCA	Fig.3	-	4 $f_{LFCO(2)}$		MHz
	output frequency LLCB		-	4 $f_{LFCO(2)}$		MHz
	output frequency LLC2A		-	2 $f_{LFCO(2)}$		MHz
	output frequency LLC2B		-	2 $f_{LFCO(2)}$		MHz
t_r, t_f	rise and fall times	Fig.3	-	-	5	ns
t_{LL}	duty factor LLCA, LLCB, LLC2A and LLC2B (mean values)	note 1; Fig.3; at 1.5 V level	40	50	60	%

Notes to the characteristics

1. f_{LFCO} = 7.0 MHz and output load 40 pF (Fig.3). V_{SSA} and V_{SSD} connected together.
2. t_{comp} is the rise time from LOW of all clocks to HIGH of all clocks (Fig.3) including rise time, skew and jitter components. Measurements taken between 0.6 V and 2.6 V. Skew between two LLx clocks will not deviate more than ±2 ns if output loads are matched within 20 %.
3. MS and LFCO2 functions not tested.

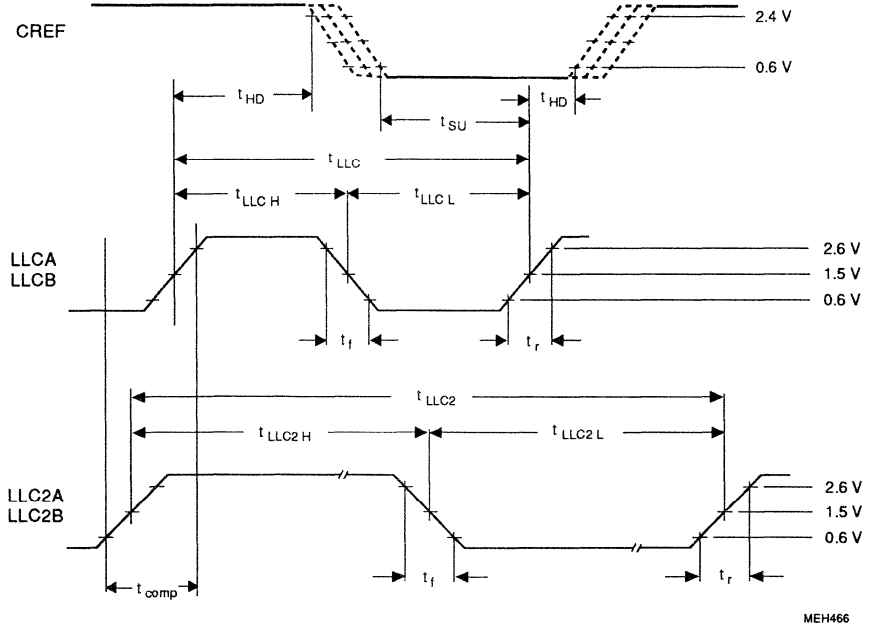


Fig.3 Output timing.

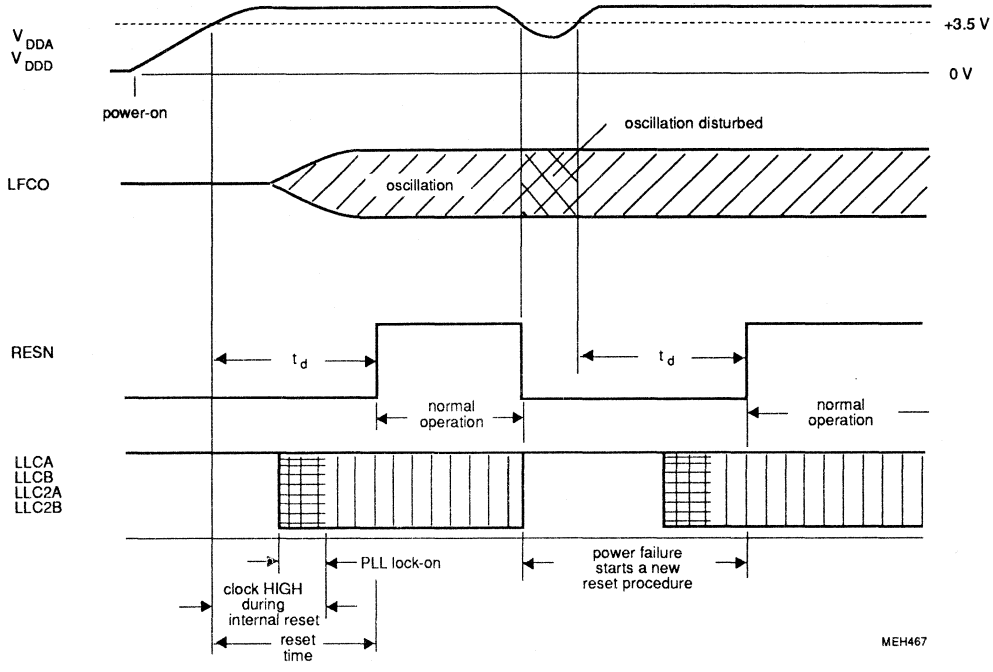


Fig.4 Reset procedure.

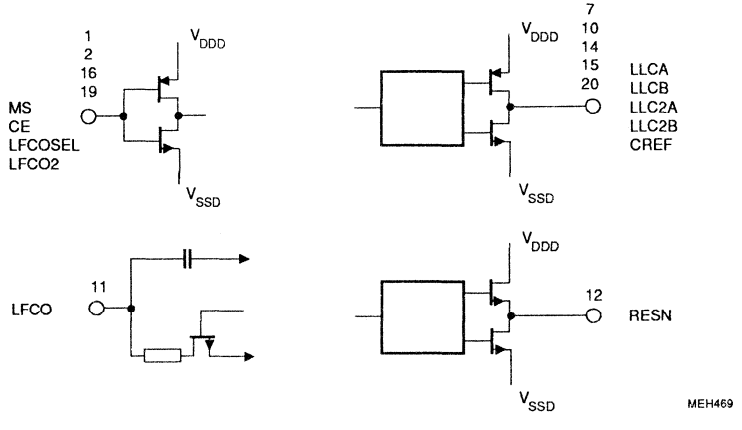


Fig.5 Internal circuit.

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